TRANSISTOR CIRCUIT ANALYSIS

ALFRED D. GRONNER

theory and
step-by-step
solutions to
235 problems

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ALFRED D. GRONNER
Singer-General Precision, Inc.

REVISED EDITION
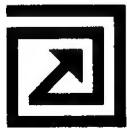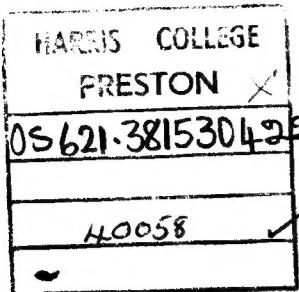
PREFACE

This book combines the advantages of both the textbook and the so-called review book. As a textbook it can stand alone, because it contains enough descriptive material to make additional references unnecessary. And in the direct manner characteristic of the review book, it has hundreds of completely solved problems that amplify and distill basic theory and methods. It is my intention that this book serve equally well as a basic text for an introductory course, and as a collateral problem-solving manual for the electrical engineering student at the junior- or senior-level, who has had a course in circuit theory. It is also a useful supplement for the student taking advanced courses in related areas that require a knowledge of transistors. The analysis and design problems should benefit professional engineers encountering transistors for the first time.

Although the principles of transistor circuit design and analysis are developed in an academic manner, a practical emphasis is maintained throughout; i.e., the student is shown how to "size up" a problem physically, and to estimate the approximate magnitudes of such parameters as quiescent operating point, impedances, gain, etc. Moreover, a scrupulous effort is made in the solved problems to keep sight of underlying analytical and physical principles, thereby establishing a strong background for the practical problems that arise in the analysis and design of circuits.

New concepts, definitions, and important results are tinted in grey throughout the text. The solved problems are generally comprehensive, and incorporate numerous applications. Supplementary problems are included not only for exercise but also to strengthen the skill and insight necessary for the analysis and design of circuits.

After a preliminary discussion of semiconductor principles in Chap. 1, a complete chapter is devoted to graphical analysis of semiconductor circuits. Thus the foundation is laid for succeeding chapters on small- and large-signal parameters. Nonlinearities, in particular, are easily investigated by means of the graphical methods described.

Chapter 3 provides a thorough coverage of the small-signal equivalent circuit, with emphasis on the tee-equivalent and hybrid configurations. The hybrid-π circuit is introduced in connection with the high-frequency limitations of transistor behavior.

Chapter 4 presents a variety of bias circuit configurations, including leakage effects, stability factors, temperature errors, and methods of bias stabilization.

Chapter 5 establishes the basic formulae for the small-signal amplifier. Multistage amplifiers, together with various feedback circuits, are considered in Chap. 6. Power amplifiers, both single-ended and push-pull, are covered in Chap. 7.

Chapter 8 rounds out much of the material on feedback developed in earlier chapters, and investigates the operational amplifier and the stability of high-gain feedback amplifiers by Nyquist and Bode techniques.

The appendices provide a convenient reference to transistor characteristics, important formulae, asymptotic plotting, and distortion calculations.

I am deeply grateful to Mr. Sidney Davis, who made important contributions to both the first and second editions in organizing the problems, unifying the notation, and commenting on the contents as a whole. I also wish to acknowledge the editorial efforts of Raj Mehra of Simon & Schuster, Inc., towards the revision of the first edition.

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TABLE OF CONTENTS

SEMICONDUCTOR PHYSICS AND DEVICES

1.1 Basic Semiconductor Theory

Solid-state devices such as the *junction diode* and *transistor* are fabricated from *semiconductor materials*. These materials have electrical resistivities which lie between *conductors* and *insulators*. The principal semiconductors used are the elements *germanium* and *silicon*, which in a pure state occur in *crystalline form*; namely, where the atoms are arranged uniformly in a periodic pattern.

To fully appreciate the operation of solid-state devices, a familiarity with atomic physics is needed. Refer to Fig. 1.1, which shows the atomic models of germanium and silicon. The *nuclei* of the atoms have 32 and 14 units of positive charge or *protons*, respectively, while around the nuclei orbit an *identical number* of units of negative charge or *electrons*. This equalization of charges results in the atoms possessing a total effective charge which is *neutral*.

The electron orbits are arranged in *shells* designated by the letters *K, L, M, N, . . .* . According to quantum mechanics, the maximum allowable number of electrons in shell *K* is 2, in *L*, 8, in *M*, 18, and in *N*, 32. A *filled* shell has very little influence on chemical processes involving a particular atom.

The electrons in their individual orbits around the nucleus exhibit specific energy values, called *discrete energy levels*. These are determined by the momentum of the electrons and their distance from the nucleus. The bond between the electron and the nucleus is inversely proportional to the distance between them. The closer they are, the greater the energy required to free the electron from the atom. Subsequently, electrons which are remote from the nucleus require less energy to free themselves from the atom.
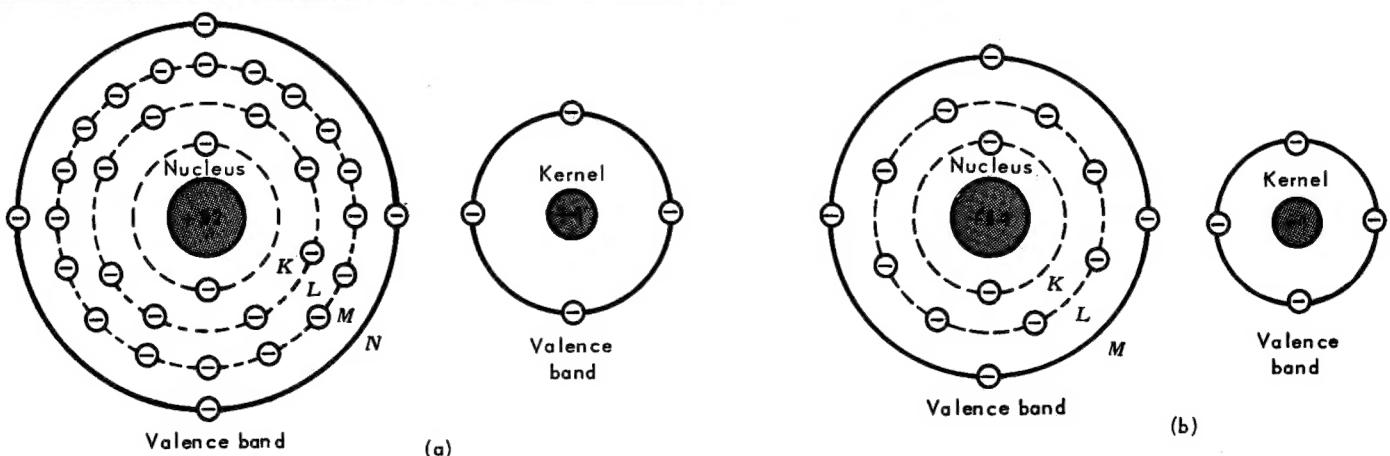

Fig. 1.1 Models of (a) germanium and (b) silicon atoms, and their simplified representations.

Conduction band

Valence band

(a)

Conduction band

Energy gap

Valence band

(b)

Conduction band

Energy gap

Valence band

(c)
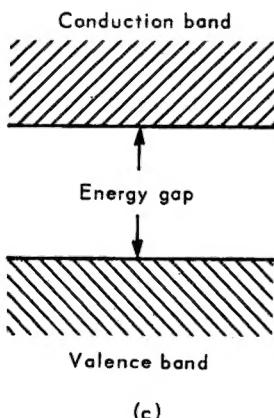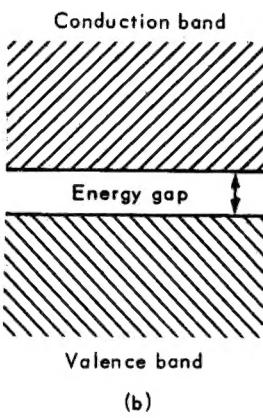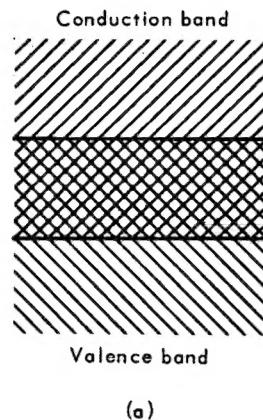
Fig. 1.2 Comparison of energy gaps between valence and conduction bands for (a) conductors, (b) semiconductors, and (c) insulators.

Valence electrons are those in the outer orbit which can break away more freely from the atom. The inner orbit electrons can be combined with the nucleus; in effect, simplified to a *central core* or *kernel* (Fig. 1.1), which may then be considered a modified nucleus. The *valence band* electrons or outer orbit electrons determine the chemical and crystalline properties of the elements.

Valence electrons exist at *excitation levels* if energy is supplied from some external source. When the energy source is removed, the electrons normally fall back into the valence band. The most common source of energy that moves valence electrons into excitation levels is *heat*. At absolute zero, electrons do not exist at excitation levels.

Valence electrons at excitation levels are called *free electrons*. They are so loosely held by the nucleus that they will move relatively freely through a semiconductor in response to *applied electrical fields* as well as other forces.

Now consider a *semiconductor crystal* wherein the atoms are arranged uniformly in a periodic pattern. The proximity of neighboring atoms leads to modifications in the energies of the valence electrons. The energies are distributed in an *energy band* that represents the *range* of energies of the valence electrons in the crystal. Although the energies of the specific electrons have *discrete values*, the energy bands corresponding to the valence electrons in the crystal appear almost as a continuous band of energy distribution.

There is also a corresponding energy band for every shell within each atom of the crystal. The bands are separated by *energy gaps*, which represent the energy required to move electrons between bands. Energy is generally expressed in *electron volts* ($1 \text{ ev} = 1.6 \times 10^{-19}$ joules). Quantum mechanics demonstrates that electrons can only exist at energy levels *within the bands* and not at levels *within the forbidden gaps*.

Electron motion within an energy band can only occur if the band is not filled, such as in the case of the valence band. If sufficient energy is applied to an electron, it can move from its band to a higher band. Heat or energy supplied by an external electric field can move an electron from the valence band to the *conduction band*, where it may travel with relative ease through the crystal. If all valence bands in a crystal are filled, conduction can only occur if electrons are first moved to the conduction band. The vacant sites left in the valence band are called *holes*.

PROBLEM 1.1 What distinguishes conductors, semiconductors, and insulators in terms of the forbidden energy gap?

Solution: In a conductor, the forbidden gap between conduction and valence bands is zero (they actually overlap in most conductors.) Therefore, no energy is needed to move electrons into the conduction band and electron flow is large for small applied voltage.

In a semiconductor, the forbidden gap is on the order of 1 v. Temperature will excite some electrons across it, but the number so excited is small.

In an insulator, the forbidden gap is very wide and almost no electrons are available for conduction. Therefore a large amount of energy is required to cause conduction.

Figure 1.2 shows the above energy levels in a convenient, diagrammatic form.

The valence bands of both germanium and silicon atoms have 4 electrons each (Fig. 1.1), and in crystals form *covalent bonds*; i.e., adjacent atoms share pairs of valence electrons. At absolute zero temperature the valence band is filled, and there are no electrons available for conduction. The semiconductor is then said to have *infinite resistivity*. As temperature increases, the valence electrons absorb energy and a certain number break their covalent bonds
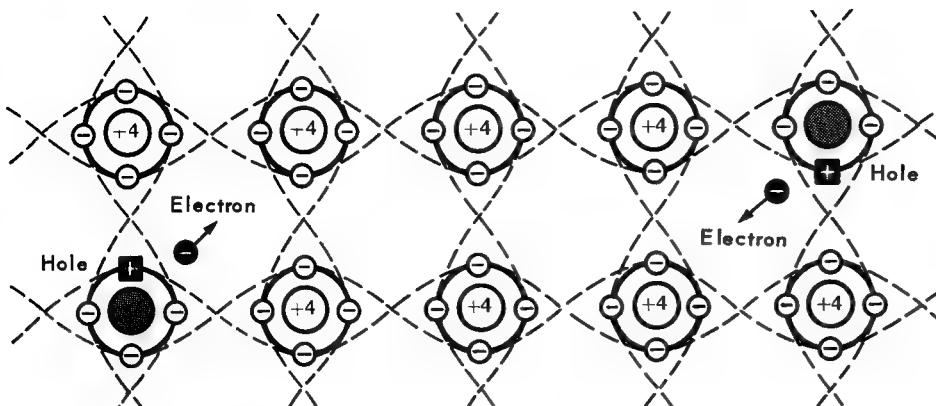
Fig. 1.3 The generation of mobile electron-hole pairs due to thermal agitation in a germanium crystal shown two-dimensionally.

(Fig. 1.3). The broken bonds move electrons into the conduction band, leaving holes in the valence band. This makes conduction possible *in both bands*. In the conduction band, the free electrons move in response to an applied electric field, while in the valence band, electrons move by shifting from one hole to the next. The latter process is most easily visualized by regarding the *holes* as *positive particles*, moving under the influence of an electric field. When the holes reach an electrode, they neutralize electrons at the electrode, so that the resultant current cannot be distinguished outside the semiconductor from the more familiar conduction band current (Fig. 1.4).

The valence electrons of common semiconductors require relatively large amounts of energy to break their covalent bonds, and thus exhibit a characteristic poor conductivity. The valence electrons of silicon and germanium need, respectively, 1.1 ev and 0.72 ev to excite them out of their covalent bonds. The greater energy needed for the silicon electrons indicates that pure silicon has higher ohmic resistance than pure germanium. The resistivity of the pure semiconductor is its *intrinsic resistivity*.

PROBLEM 1.2 Why does the conductivity of a semiconductor *increase*, rather than *decrease* with temperature, as does the conductivity of a metal?

Solution: As temperature increases in a semiconductor, the number of *electron-hole pairs* generated by thermal agitation increases. The liberated electrons and holes are current carriers, and thus provide increasing conductivity.

But at very high temperatures, when sufficiently large numbers of free electrons and holes are generated, collisions tend to increase resistance by reducing the average speed of the current carriers.
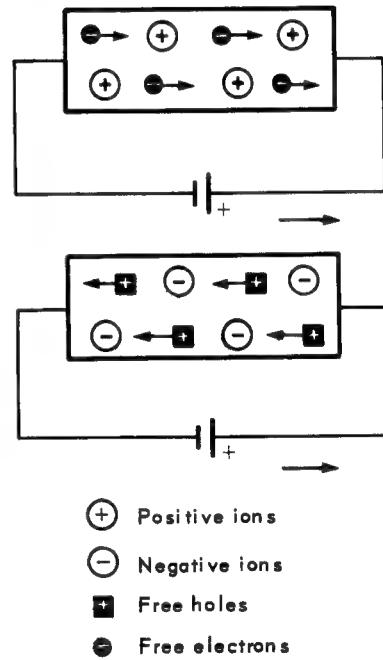
Fig. 1.4 Movement of electrons and holes in two types of semi-conductors.

1.2 Effects of Impurities

When an electron moving through a semiconductor crystal encounters a hole, *recombination* occurs. We may think of the electron as "entering" the hole, and the electron-hole pair thereby ceasing to exist. At any given temperature, equilibrium exists where the rate of thermal generation of electron-hole pairs equals the recombination rate.

It may thus be inferred that in a pure semiconductor crystal, the number of electrons *equals* the number of holes. The crystal is, of course, electrically neutral.

To create a useful semiconductor device, a small amount of a specific impurity element is added to the pure semiconductor crystal. The technique is called *doping*. The most common impurity elements are atoms of approximately the same volume as the atoms of the crystal or *host*, in order to minimize dislocation of the crystal structure. However, the impurity atoms have either one electron more (*pentavalent*) or one electron less (*trivalent*) in their valence bands than the host.

When the impurity atoms are introduced into the crystal structure to form covalent bonds with the host atoms, there will be – depending on the type of impurity – either an extra electron or extra hole in the vicinity of each impurity atom. Impurities that contribute extra electrons are called *donor* or *n-type* (n for negative) *impurities*, and the crystal thus treated becomes an *n-type semiconductor*. Analogously, impurities that contribute extra holes are called *acceptor* or *p-type* (p for positive) *impurities*, and the crystal thus treated becomes a *p-type semiconductor*. Figure 1.5 shows how the type of impurity determines whether a semiconductor becomes either an *n*-type or *p*-type.
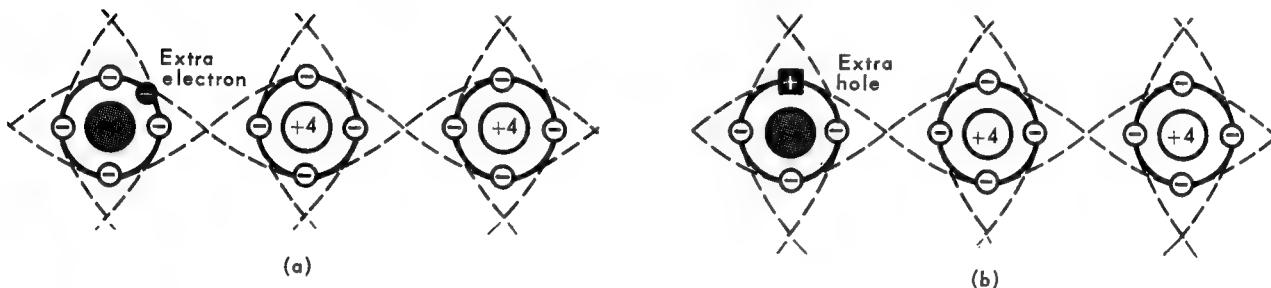
Fig. 1.5 Effect of impurities on pure germanium crystals. (a) Donor impurity provides mobile electrons. The positively-charged atoms are not free to move. (b) Acceptor impurity provides mobile holes. The negatively-charged atoms are not free to move.

Typical numbers showing impurity effects are of interest. Pure silicon, for example, has approximately 10^{10} charge carriers (electrons and holes) per cubic centimeter at room temperature, and an intrinsic resistivity of 240,000 Ω-cm. Typically, a crystal of silicon might be doped by one donor atom per 10^8 host atoms with a corresponding reduction in resistivity.

PROBLEM 1.3 What effect do added impurities have on semiconductor conductivity?

Solution: Added impurities contribute electrons or holes which are not rigidly held in covalent bonds. Thus electrons may move freely through *n*-type material, thereby creating an electric current. Similarly, the principal current in *p*-type material is that of *holes moving through the crystal in the opposite direction to the movement of electrons.*

Electron and hole motion constitute components of *current flow*. The charge carriers contributed by the impurity atoms lead to substantially increased conductivity.

In *n*-type material, electrons are called *majority carriers* and holes are called *minority carriers*. In *p*-type material, the holes are majority carriers and the electrons minority carriers. Both *p*-type and *n*-type materials are normally electrically neutral even though free holes and electrons are present.

PROBLEM 1.4 Would you expect minority carrier current flow in response to an applied voltage?

Solution: Minority carrier flow occurs in response to an applied voltage since it is a current carrier. Majority carrier flow, however, is predominant, except at high temperatures where thermally-generated electron-hole pairs lead to a higher proportion of minority carriers.

1.3 The *p-n* Junction

If p-type and n-type materials are mechanically joined together to form a single crystal, and they thereby create a junction in which the continuity of the crystalline structure is preserved – such a junction is called a *p-n junction* or *junction diode.*

Since both the p-type and n-type materials exist at different charge levels because of natural and impurity differences, they seek equilibrium between one another and an energy exchange occurs. Thus electrons and holes migrate across the p-n junction by the fundamental process of *diffusion*; i.e., the spread of charge carriers from regions of high concentration to regions of low concentration, ultimately tending toward uniform distribution. By diffusion, the holes migrate from p-type to n-type material, while the electrons move in the opposite direction.

Figure 1.6a shows the p-n junction. During diffusion, the *excited* or *ionized areas* on either side of the junction become relatively free of charge carriers due to the *annihilation* of electrons and holes by recombination, and are called the *depletion layer* or *region.* An electric field also builds up, generated by the newly created positive and negative ions located in the opposing materials, and conduction decreases. A *potential difference* or *barrier* is thus created in the depletion region (Fig. 1.6b) which inhibits further electron and hole migration. This potential difference is called the *potential barrier voltage* or *contact potential,* and is about 0.3 v for germanium and 0.7 v for silicon at room temperature.

An equilibrium condition or *barrier balance* in which conduction is limited by the potential difference exists between the p-type and n-type materials. However, if electron-hole pairs are formed by thermal agitation in the p-type material, electrons will flow across the p-n junction *aided* by the electric field. Similarly, holes in the n-type material will also migrate. Therefore minority carriers continue to flow despite the *barrier balance,* assisted by the potential difference established by the diffusion of majority carriers. Of course any net movement of minority carriers due to increasing temperature will be balanced by further diffusion of majority carriers, and a resultant widening of the depletion region.

Now suppose an external potential is applied to the p-n junction of Fig. 1.7a. With the polarity shown in Fig. 1.7b, the junction is *forward-biased* and the field of the applied potential difference opposes the internal field across the depletion layer. Majority carriers therefore will flow freely across the barrier. When the polarity of the externally applied voltage is *reverse-* or *back-biased* (Fig. 1.7c), the internal field across the junction is increased, and majority carriers *cannot* flow. However, minority carriers generated by thermal agitation continue to flow freely. This property of conducting essentially in one direction makes the p-n junction a *rectifier.*

Note that the depletion region gets wider as applied reverse voltage is increased. Since the depletion layer does not contain many current carriers, it acts as an insulator, and the depletion region can be regarded as a *capacitor* whose plate distance varies with the reverse voltage.

⊕ Donor atoms

⊖ Acceptor atoms

+ Holes

− Electrons

■ Imperfections, etc.
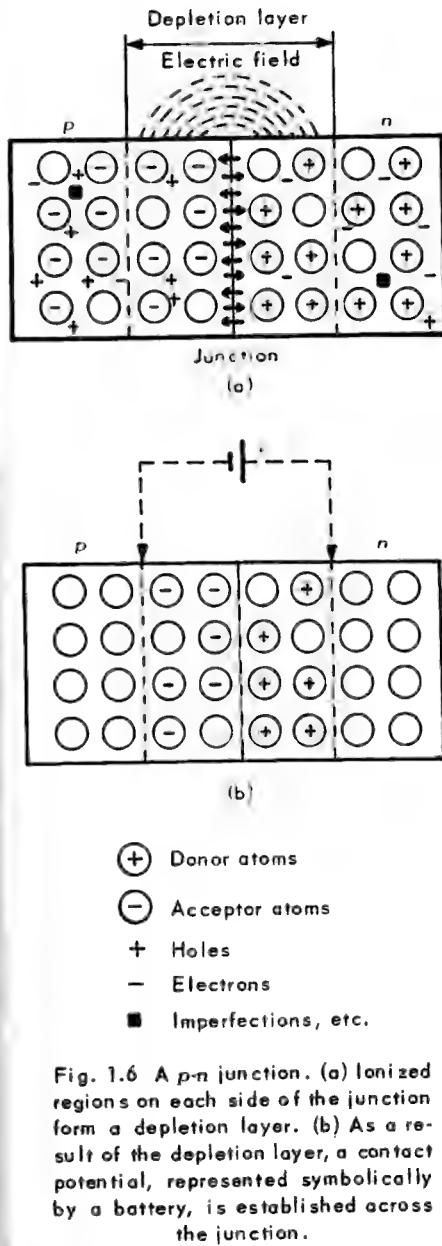
Fig. 1.6 A *p-n* junction. (a) Ionized regions on each side of the junction form a depletion layer. (b) As a result of the depletion layer, a contact potential, represented symbolically by a battery, is established across the junction.

(a)

(b)

(c)
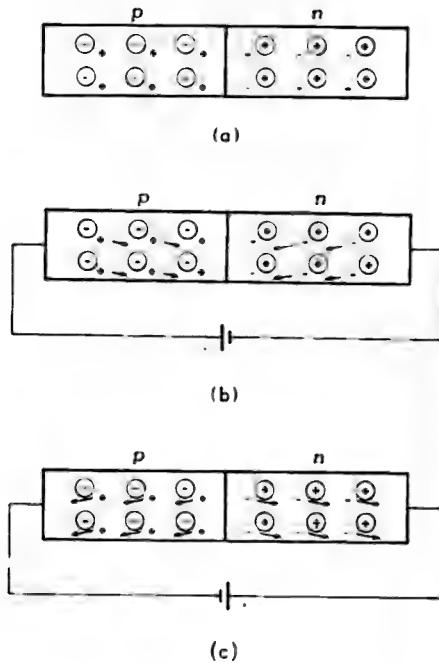
Fig. 1.7 (a) Unenergized *p-n* junc-
tion. (b) The effect on the *p-n* junc-
tion of application of forward bias.
(c) When the battery connections
are reversed, the electrons and
holes are drawn away from the
p-n junction.

A plausible expression for current flow across a *p-n* junction as a function of applied voltage may be developed by using relationships from semiconductor physics. Referring to Figs. 1.7a–c, consider first the case where no external bias is applied. There are four current components flowing simultaneously across the junction:

1. A *diffusion current* I_{dn} due to *electron flow* from the *n*-type material with its relatively high concentration of mobile electrons.
2. A *diffusion current* I_{dp} due to *hole flow* from the *p*-type material with its relatively high concentration of mobile holes.

These two current components are *majority carrier* currents since they are due to electrons in the *n*-region and holes in the *p*-region. As a result of the flow of these current components, at the junction the *n*-type material develops a net positive charge and the *p*-type material a net negative charge, which leads to a potential barrier across it. This barrier limits further diffusion except for the effect of thermally-generated electron-hole pairs on both sides of the junction. Consequently the remaining two current components are:

3. A current I_{gn} due to thermally-generated free electrons in the *p*-region, which are accelerated across the junction by the barrier voltage.
4. A current I_{gp} due to thermally-generated free holes in the *n*-region, which are accelerated across the junction by the barrier voltage.

These last current components are *minority carrier* currents, since they are due to electrons in the *p*-region and holes in the *n*-region.

Since holes flowing in one direction across the junction, and electrons flowing in the opposite direction correspond to the same current direction:

$$\text{Total diffusion current } I_d = I_{dp} + I_{dn}. \tag{1.1}$$

$$\text{Total thermally-generated current } I_s = I_{gp} + I_{gn}. \tag{1.2}$$

This latter current component, I_s, is called the *saturation current*, and is discussed later.

In the absence of applied voltage, under open-circuit or short-circuit conditions, the net current flow must be zero. Therefore,

$$I_d = I_s.$$

The barrier potential adjusts itself until an *equilibrium* exists between the diffusion and thermally-generated current components.

An externally applied voltage modifies this equilibrium, and leads to a condition of net current flow across the junction. Depending on the polarity of the applied voltage, the potential barrier is either raised or reduced.

To arrive at a quantitative picture of current flow with applied voltage, it is necessary to relate I_d to barrier potential. Although the detailed background physics is beyond the scope of this book, it is intuitively clear that the rates of diffusion of electrons or holes depend on the concentrations, *n* and *p*, of electrons and holes, respectively, in the regions from which they diffuse. In the typical materials used in making common semiconductor devices, the concentrations of majority carriers are affected to only a slight extent by the relatively low concentrations of thermally-generated electron-hole pairs.

From semiconductor physics,

$$I_{dp} = p e^{\frac{-q}{kT}(V_B - V)} \tag{1.3}$$

and

$$I_{dn} = n e^{\frac{-q}{kT}(V_B - V)}, \tag{1.4}$$

where

V_B = barrier potential at equilibrium, volts.
k = Boltzmann's constant = 1.38×10^{-23} joules/°K.
T = absolute temperature, °K.
q = electron charge = 1.6×10^{-19} coulomb.

In consistent units, for $T = 300$ °K (approximately room temperature),

$$\frac{kT}{q} = 0.026. \tag{1.5}$$

Note that I_{dp} and I_{dn} are proportional to the p and n concentrations, respectively, as noted earlier. Note further that diffusion currents decrease exponentially as V_B increases, which is intuitively plausible, and consistent with previous reasoning.

The total diffusion current is, therefore,

$$I_d = I_{dp} + I_{dn}.$$

or, substituting and simplifying,

$$I_d = A e^{\frac{q}{kT} V}, \tag{1.6}$$

where A is a constant.

Since the total junction current is the difference between diffusion current and saturation current (I_s),

$$I = I_d - I_s, \qquad \text{or} \qquad I = A e^{\frac{q}{kT} V} - I_s.$$

Now, at $V = 0$ and $I = 0$,

$$I_s = A.$$

Hence,

$$I = I_s (e^{\frac{q}{kT} V} - 1). \tag{1.7}$$

This is the expression for the diode current, and is often referred to as the *rectifier equation*. Since $kT/q = 0.026$ v at room temperature, the expression for I simplifies for $V \gg 0.026$ v, that is,

$$I \cong I_s e^{\frac{q}{kT} V} \qquad \text{for} \quad V \gg 0.026 \text{ v}. \tag{1.8}$$

Similarly, for V negative by more than about 0.1 v,

$$I \cong -I_s.$$

The diode characteristic in the forward and reverse regions are plotted in Fig. 1.8. The rapid increase in reverse current at a large reverse voltage is discussed later.

PROBLEM 1.5 Explain the flat character of the saturation current of the p-n junction.

Solution: The reverse current is dependent on the number of minority carriers in the semiconductor crystal. When a few tenths of a volt reverse voltage is applied, all the thermally-generated minority carriers are swept across the junction. Reverse current is limited by the number of available minority carriers.

The saturation or *reverse leakage* current increases sharply with temperature (Fig. 1.9). As a very approximate rule of thumb, this leakage component doubles for every 10 °C increase in temperature.
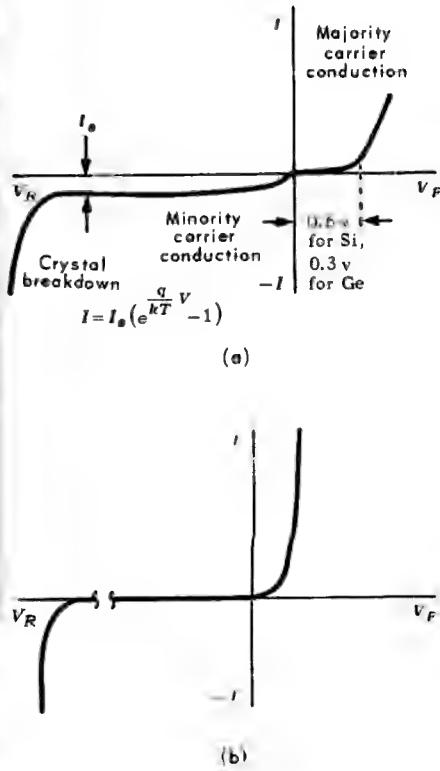
Fig. 1.8 Current vs. voltage across a p-n junction. (a) The magnitudes of the leakage current I_s and forward voltage V_F are greatly exaggerated. (b) A scaled drawing of a diode characteristic.
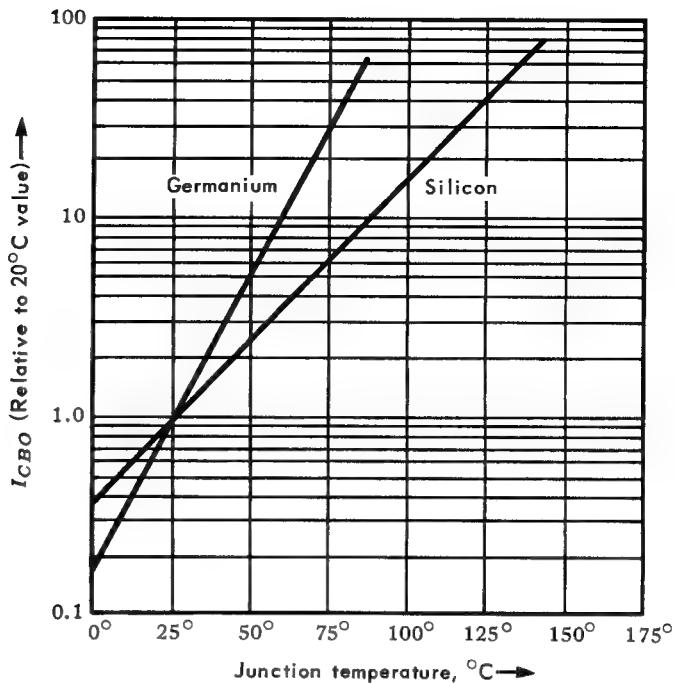
Fig. 1.9 Typical variation of I_s with temperature for germanium and silicon diodes.

PROBLEM 1.6   Would you expect germanium or silicon to have the greater value of reverse leakage? Why?

Solution: Since reverse leakage is predominantly due to minority carriers generated by thermal agitation, it is evident that germanium, with its lower energy gap (0.72 ev for Ge compared to 1.1 ev for Si) between valence and excited electron states, would have the greater leakage. The greater energy gap of silicon allows it to be used at much higher temperatures (to 150 °C approximately) than germanium, whose maximum junction temperature is slightly above 100 °C.

PROBLEM 1.7   Sketch a curve similar to Fig. 1.8a, roughly comparing a silicon and a germanium diode. How does the width of the energy gap affect diode characteristics?

Solution: Figure 1.10 provides the required sketch. In the forward direction, more voltage is required to overcome the barrier potential (related to the energy gap) for silicon. In the reverse direction, the tighter covalent bonds mean greater crystal breakdown voltages. The saturation current, as previously discussed, is higher for germanium. Note the different scales in the forward and reverse directions.

Fig. 1.10 Comparing silicon and germanium diode characteristics. Note the modified scales for plus and minus ordinates. Voltages V_{FG} and V_{FS} are forward voltages caused primarily by the potential barriers.

PROBLEM 1.8   Derive a formula for the diode incremental forward resistance or *dynamic resistance* where $r_f = dV/dI$ for currents in the forward direction. Note that this is the resistance to small changes in current and voltage about a particular operating current, I.

Solution: The rectifier equation for the diode current is

$$I = I_s (e^{\frac{q}{kT} V} - 1) .$$ [1.7]

Differentiating (1.7) with respect to V,

$$\frac{dI}{dV} = \frac{q}{kT} I_s e^{\frac{q}{kT} V} .$$ (1.9)

For large positive voltage, $e^{(q/kT)V} \gg 1$, and $I \cong I_s e^{(q/kT)V}$ from (1.7). Substitute this in the expression (1.9) for dI/dV:

$$\frac{dI}{dV} = \left(\frac{q}{kT}\right) I,$$

and

$$r_f = \frac{dV}{dI} = \frac{kT}{qI}. \tag{1.10}$$

Note that the incremental diode forward resistance r_f varies *inversely* with the diode forward current.

PROBLEM 1.9 At room temperature, find the incremental resistance r_f as a function of I. Introduce numerical values for k, T, and q.

Solution: Room temperature, 25°C, corresponds to $273 + 25°C = 298°K$. Substitute in (1.10) using numerical values for k and q:

$$r_f \cong \frac{26}{I}\,\Omega, \tag{1.11}$$

where I is in milliamperes.

PROBLEM 1.10 What is the incremental resistance of a forward conducting *p-n* junction with 2 ma current?

Solution: Substitute in (1.11):

$$r_f \cong \frac{26}{I} = \frac{26}{2} = 13\,\Omega.$$

PROBLEM 1.11 If forward diode resistance r_f is 13 Ω at 25°C and 2 ma, what is the resistance at 125°C and 2 ma?

Solution: Refer to (1.10) in which r_f is directly proportional to absolute temperature:

$$r_{f\,125°C} = \frac{273 + 125}{273 + 25}(13) = \frac{398}{298}(13) = 17.4\,\Omega.$$

The effect of temperature on the diode forward characteristics may now be estimated. From (1.10), the incremental diode forward resistance r_f is inversely proportional to current and directly proportional to temperature, °K. Since °K = 273 + °C, relatively small changes in °C about a room temperature ambient lead to much smaller *percentage* changes in °K. Consequently r_f is relatively independent of temperature. However, diode *ohmic* resistance decreases with increasing temperature due to increased thermal agitation.

A family of diode forward characteristics as a function of temperature has the general appearance of Fig. 1.11. Points at the same current level have the same incremental resistance (except, of course, at very low voltages where $e^{Vq/kT}$ is not much greater than unity), so that the curves are essentially parallel. It turns out that for a fixed forward current, the forward voltage drop decreases by about 1.5 to 3 mv/°C. As a rule of thumb, a good average figure for temperature sensitivity is −2.5 mv/°C. This determines the separation of the individual curves of the family shown in Fig. 1.11.


Fig. 1.11 Family of forward diode characteristics for different temperatures. At $I = I_{F_1}$, a constant forward current, the curves are approximately uniformly spaced for equal temperature increments.

PROBLEM 1.12 A diode has a forward drop of 0.6 v at 10 ma where the temperature is 25°C. If current is held constant, what is the forward drop at 125°C?

Approximately what additional voltage is required at 125°C to increase current to 12 ma?

Solution: At 125°C and constant current, the diode forward drop decreases by $(2.5 \text{ mv/°C}) \times 100 = 250$ mv.   The forward drop at high temperature is now only 0.350 v.

Using the method of Prob. 1.11, $r_f = 3.5\ \Omega$.   The additional voltage corresponding to a current increment of 2 ma is

$$\Delta V = r_f \Delta I = 3.5 \times 2 \times 10^{-3} = 0.007 \text{ v}.$$

There is a 7 mv increase in voltage.

An additional component of leakage current not previously described corresponds to *surface leakage* along the semiconductor surface between terminals. Humidity and surface impurities contribute to this leakage component. The magnitude of the leakage is proportional to the reverse voltage applied across the junction, in contrast to the constant I_s component. At low reverse voltages, the surface leakage component is negligible.

Figure 1.12 shows the effect of reverse leakage on the diode characteristic curve. At low temperatures, the surface leakage components usually predominate. At high temperatures, leakage resulting from thermal agitation becomes increasingly important. Because silicon requires more thermal agitation to generate electron-hole pairs than does germanium, the saturation leakage of silicon is much less than for germanium. Surface leakage is therefore more important in silicon p-n junctions.
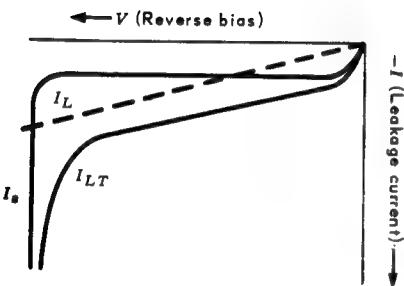
Fig. 1.12 Leakage components in a semiconductor: I_s = saturation component due to minority carriers, I_L = surface leakage component, I_{LT} = total leakage.

PROBLEM 1.13   A germanium diode has a saturation leakage of 200 μa at 25°C. Find the corresponding leakage component at 75°C.

Solution: From Fig. 1.9, it is estimated that the leakage increases over the temperature range by a ratio of 20 : 1.   The high temperature leakage is therefore 4 ma.

PROBLEM 1.14   A silicon diode has a saturation leakage of 10 μa at 25°C. Find the corresponding leakage components at 75°C and 125°C.

Solution: Again refer to Fig. 1.9.   The leakage increase ratio is about 6 : 1, leading to a 60 μa leakage at 75°C.   At 125°C, leakage becomes $40 \times 10 = 400\ \mu$a.

PROBLEM 1.15   A silicon diode operates at a reverse voltage of 10 v and has a total leakage of 50 μa.   At 40 v, the leakage is 80 μa.   Find the leakage resistance R_L and the leakage currents.

Solution: The total leakage consists of a voltage-independent component I_s, and a surface leakage component I_L :

$$I_{LT} = I_s + I_L,$$

$$50\ \mu\text{a} = I_s + \frac{10}{R_L}, \tag{1.12a}$$

$$80\ \mu\text{a} = I_s + \frac{40}{R_L}, \tag{1.12b}$$

where R_L equals the equivalent resistance corresponding to surface leakage. Now subtract (1.12a) from (1.12b) and solve for R_L:

$$30\ \mu\text{a} = \frac{30}{R_L}, \qquad R_L = \frac{30}{30}\ \mu\text{a} = 1\ \text{M}\Omega.$$

Thus $I_{LT} = I_s + V/1$ MΩ where V is the applied reverse voltage. We then solve for I_s as follows:

$$50\ \mu a = I_s + \frac{10}{1}, \qquad I_s = 40\ \mu a.$$

The final expression is

$$I_{LT} = (40 + V)\ \mu a.$$

The 40 μa component varies sharply with temperature, as previously discussed.

When sufficiently large reverse voltages are applied, the potential gradient (electric field) across the *p-n* junction may measure in the hundreds of thousands of volts per inch. Such a gradient will impart a very high kinetic energy to the minority carriers normally flowing across the junction. Thus the minority carriers, as a result of increased momenta, will collide with the atoms of the crystal with such a force as to release additional carriers, which in turn, are accelerated by the gradient. An *avalanche breakdown* therefore occurs, and there is a very rapid increase in current for slight increases in reverse voltage (Fig. 1.8). But as long as the allowable junction power dissipation is not exceeded, the diode can operate in the avalanche breakdown mode without damage. This characteristic makes the *avalanche* or *Zener diode* suitable for voltage regulating circuits.

True Zener breakdown refers to the disruption of covalent bonds because of the presence of a high electric field. In practice, however, the diode generally breaks down because of the avalanche effect.

PROBLEM 1.16 A diode breaks down under a reverse voltage of 40 v. A 60 v battery is applied to the diode through a 1000 Ω resistor. Find the power dissipation at the junction.

Solution: The diode drop is 40 v, leaving a 20 v drop across the resistor. The current, by Ohm's law, is $20/1000 = 20$ ma. The *p-n* junction dissipation is 40 v $\times$ 20 ma = 0.8 w.

PROBLEM 1.17 A diode is in series with a 100 Ω resistor and a 2 v battery (Fig. 1.13a). Find the circuit current and show, qualitatively, the effect of increased temperature.*

Solution: The problem is easily solved by superimposing a *load line* corresponding to the 100 Ω resistor on the diode forward characteristic. The graphical solution of Fig. 1.13a, as shown in Fig. 1.13b, is much easier to obtain than an analytical solution based on (1.7). The load line is drawn with a slope of magnitude 2 v/20 ma = 100 Ω. The load line intersects the diode characteristic at point P, which is the operating point. From the curve it is estimated that the diode voltage = 0.6 v and diode current = 14 ma. At higher temperatures, the characteristic curve shifts to the left and the operating point is located at P'.

The diode may be conveniently represented for analytical purposes by the straight-line *piecewise linear* approximation of Fig. 1.14. The slope of the straight-line approximation corresponds to r_f, the average forward resistance in the vicinity of the operating current. This straight line intersects the horizontal axis at E, the voltage corresponding to the battery of the equivalent model. For various temperatures, the straight line portions are parallel.
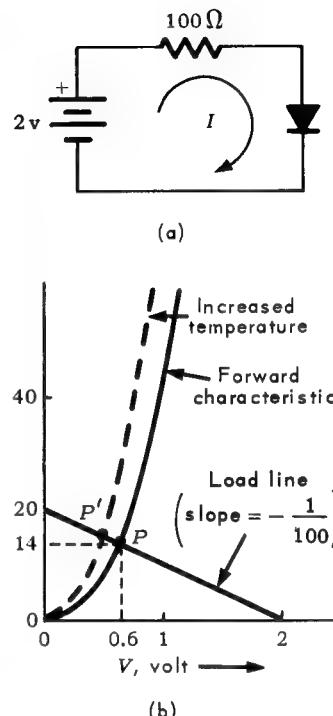
Fig. 1.13 Graphical solution of Prob. 1.17.
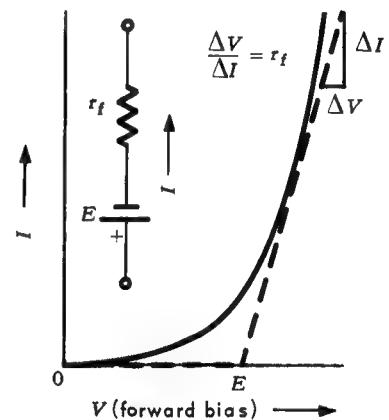
Fig. 1.14 Forward characteristic of diode approximated by two-line segments (piecewise linear approximation). The equivalent model is a battery in series with V_F, as long as there is substantial forward conduction.

*In this and the following problems, the diode is operated as a forward-biased device.
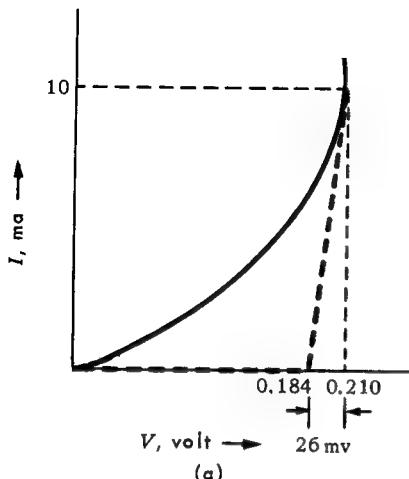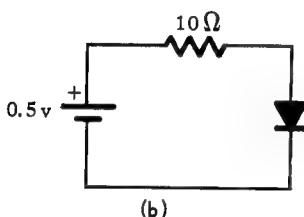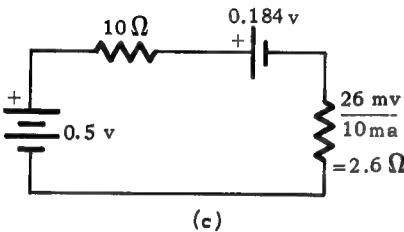
Fig. 1.15 Solution to Prob. 1.18. (a) Diode characteristics, (b) circuit, and (c) equivalent model.
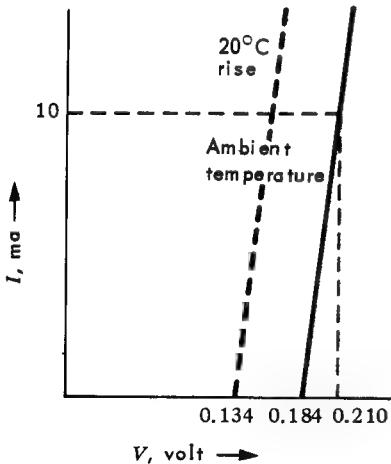
Fig. 1.16 Idealized diode characteristic showing effect of 20°C rise in temperature.

PROBLEM 1.18 A diode having the characteristics of Fig. 1.15a is energized as shown in Fig. 1.15b. Calculate the forward current.

Solution: The diode equivalent circuit used to calculate the current is given in Fig. 1.15c. Current is (0.5 − 0.184)/(10 + 2.6) = 25 ma. This analysis may be compared with the graphical method of Fig. 1.13.

PROBLEM 1.19 In Prob. 1.18, show the effect of a 20 °C rise in temperature.

Solution: A 20 °C rise in temperature means a 50 mv (20 °C × 2.5 mv/°C) shift to the left in the diode forward characteristic. This is shown in Fig. 1.16 as a shift in the idealized characteristic. The high temperature current is

$$\frac{0.5 - 0.134}{10 + 2.6} = 29 \text{ ma.}$$

Actually, r_f is somewhat reduced at this higher current, but the error in neglecting this is small.

PROBLEM 1.20 A germanium diode, for which saturation current $I_s = 10 \ \mu a$, is conducting 2 ma at room temperature. What is the forward voltage drop?

Solution: Use the diode equation (1.7) and solve for voltage drop. We have

$$I = I_s (e^{\frac{q}{kT} V} - 1). \qquad [1.7]$$

Substituting numerical values,

$$2 \times 10^{-3} = 10^{-5} [e^{\frac{V}{0.026}} - 1] \qquad \text{or} \qquad 199 \times 10^{-5} = e^{\frac{V}{0.026}}.$$

Taking the natural logarithm of both sides,

$$\frac{V}{0.026} = 5.31, \quad V = 5.31 \times 0.026 = 0.14 \text{ v.}$$

PROBLEM 1.21 A diode with 10 μa saturation current is in series with a 100 Ω resistor. What current is developed with an applied voltage of 0.220 v?

Solution: The problem is solved by trial and error. Assume a series of values for V, the voltage across the diode itself, typically between 0.1 v and 0.2 v. Let $kT/q = 0.026$ v. Compute I using (1.7). To the IR drop across the 100 Ω resistor, add the assumed V to establish a figure for applied voltage. Interpolate (perhaps graphically) to find where the calculated applied voltage equals the actual applied 220 mv. This occurs for $I = 1$ ma, with a 120 mv drop across the diode. (Problems of this kind are very well suited for solution on a digital computer.)

PROBLEM 1.22 In the preceding problem, what is the applied voltage for a 22 ma current?

Solution: The solution to this problem is direct. The IR drop is 2.2 v. Since I and I_s are known, the diode equation is readily solved for diode voltage, 0.2 v, corresponding to a total applied voltage of 2.4 v.

1.4 The Transistor

The previous section describes the behavior of the *p-n* junction diode as a rectifying device. Consider now two *p-n* junctions, J_1 and J_2, as in Fig. 1.17. Junction J_1 is forward-biased so that majority carriers (in this case, electrons) flow from *n-* to *p-*material. Junction J_2 is reverse-biased, so that only I_s is flowing. If we now combine these junctions and make the *p-*region very

thin, so that majority carriers do not recombine with holes to any appreciable extent, then these majority carriers are almost all accelerated to the right by the barrier potential of J_2. If we call α the ratio of current going through J_2 to the current going through J_1,

$$I_C = \alpha \, I_E. \qquad (1.13)$$

The holes that do recombine with the few electrons in the p-region are supplied by I_B. Since α is close to but less than unity, I_E is almost entirely transferred to the right-hand junction. Because these carriers are accelerated by the J_2 barrier potential, which can be high, this current can flow through a high external resistor to produce voltage amplification.

The three-layer device described is called a *junction transistor*. The equilibrium conditions previously mentioned occur automatically at each junction. Figure 1.18 shows the two junctions biased so as to produce transistor behavior for both the n-p-n and p-n-p cases. The emitter-base junction is forward-biased and the base-collector junction is reverse-biased for ordinary amplifier operation. For p-n-p transistors, holes flow from emitter to base, and electrons from base to emitter. This is the typical flow of majority carriers characteristic of forward-biased diodes.

In all cases, the emitter current I_E is equal to the sum of base and collector currents; i.e.,

$$I_E = I_B + I_C. \qquad (1.14)$$

In practical junction transistor design, very few impurities are introduced into the base, so that the base has relatively few electron charge carriers compared to the large number of hole charge carriers of the emitter (p-n-p device). In addition, the base is made quite thin. Both of these factors tend to minimize recombination in the base. Because the current flow from base to collector occurs across a relatively high reverse bias, the power obtained in the collector-base circuit is considerably higher than the power in the base-emitter circuit. This power gain, properly exploited, is the basis for the amplifying properties of the transistor.

Figure 1.19 shows a p-n-p transistor in the so-called *common-base* connection; i.e., the base is common to both the emitter and collector circuits.

Fig. 1.17 Juxtaposition of two p-n junctions to make a transistor. (a) Junction J_1 is forward-biased, (b) junction J_2 is reverse-biased, and (c) an n-p-n junction transistor.
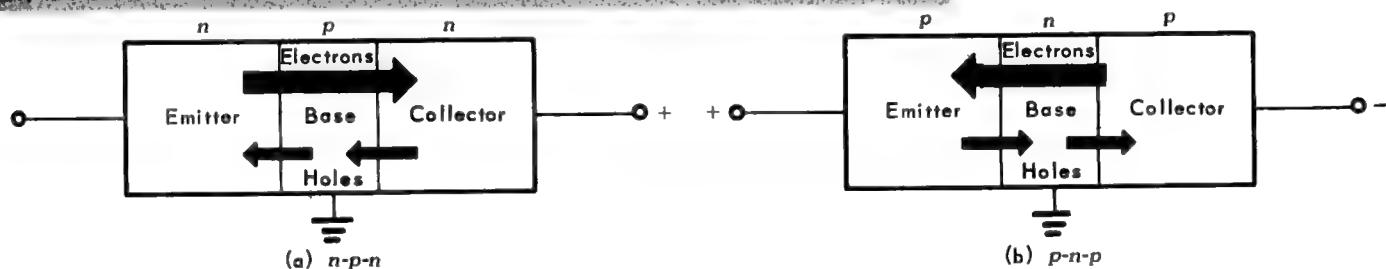
Fig. 1.18 A junction transistor showing flow of currents in normal amplifier operation.
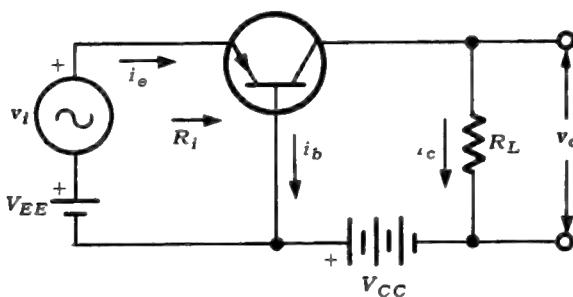
Fig. 1.19 Common-base connection of a p-n-p transistor. Lower case letters represent small-signal components of voltage and current superimposed on steady d-c bias components.

PROBLEM 1.23 The transistor in the common-base circuit of Fig. 1.19 has a current gain of α. Determine voltage gain and power gain with respect to small signal input variations.

Solution: The transistor input resistance R_i is related to the low forward resistance from emitter to base. The load resistance R_L in the reverse-biased collector circuit can be quite high. Thus,

$$\text{Input voltage} = v_i = i_e R_i ,$$

$$\text{Output voltage} = v_o = i_c R_L ,$$

$$\text{Voltage gain} = \frac{v_o}{v_i} = \frac{i_c R_L}{i_e R_i} = \alpha \frac{R_L}{R_i} ,$$

$$\text{Power gain} = \text{current gain} \times \text{voltage gain} = \alpha^2 \frac{R_L}{R_i}.$$

While the common-base circuit offers a less than unity current gain, it can provide high voltage and power gain. Other transistor connections, discussed later, can also provide large current gains.

The current gain β may be defined as the ratio of collector current to base current:

$$\beta = \frac{I_C}{I_B}. \tag{1.15}$$

PROBLEM 1.24 Derive a formula for β as a function of α.

Solution: Start with the defining relationships:

$$I_E = I_B + I_C, \qquad I_C = \alpha I_E, \qquad \beta = \frac{I_C}{I_B}.$$

Substituting I_C/α for I_E, and $I_B = I_C/\beta$, we obtain for $I_E = I_B + I_C$,

$$\frac{I_C}{\alpha} = \frac{I_C}{\beta} + I_C \qquad \text{or} \qquad \alpha = \frac{\beta}{1 + \beta}.$$

Therefore,

$$\beta = \frac{\alpha}{1 - \alpha}. \tag{1.16}$$

PROBLEM 1.25 A transistor has an α of 0.98. For an emitter current of 2 ma, calculate the base current I_B. Also calculate $\beta = I_C/I_B$.

Solution: For the stated conditions, collector current equals $0.98 \times 2 = 1.96$ ma. The difference between emitter and collector is necessarily the base current of 40 μa. Therefore,

$$\beta = \frac{I_C}{I_B} = \frac{1.96}{0.04} = 49.$$

PROBLEM 1.26 Sketch the curve of β vs. α for α between 0.95 and 1.

Solution: Calculate points using the formula $\beta = \alpha/(1 - \alpha)$:

α	β
0.95	0.95/0.05 = 19
0.96	0.96/0.04 = 24
0.97	0.97/0.03 = 32
0.98	0.98/0.02 = 49
0.99	0.99/0.01 = 99
1.00	1.00/0 = ∞

The curve is plotted in Fig. 1.20. Note the sharply increasing current gain as $\alpha \doteq 1$. A transistor with an α of 0.99 has three times the β of a transistor with an α of 0.97.
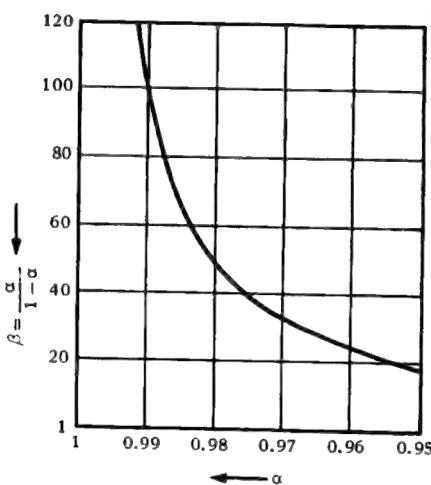
Fig. 1.20 Variation of β with α. Note that large changes in β correspond to small changes in α.

PROBLEM 1.27 A transistor has a β of 60. Find α.

Solution: Start with the equation $\beta = \alpha/(1 - \alpha)$. Solve for α:

$$\alpha = \beta - \alpha \beta,$$

$$\alpha = \frac{\beta}{1 + \beta}. \tag{1.17}$$

Substitute $\beta = 60$, and solve for α:

$$\alpha = \frac{60}{61} = 0.984.$$

The point may be estimated from the curve of Fig. 1.20 as $\alpha \approx 0.98$.

1.5 The Ebers-Moll Model of the Transistor

We are now in a position to develop a *general model* of the transistor applicable to forward- and reversed-bias conditions, and adaptable to a-c as well as d-c conditions. The *Ebers-Moll model*, in effect, presents the transistor *static characteristics* derived from previously developed concepts in convenient form. Although the Ebers-Moll model will later be expanded to cover high-frequency characteristics, for the moment its use will be confined to low frequency where capacitive effects are negligible. The low-frequency model is the starting point for the development of a variety of equivalent circuits and their analyses in succeeding chapters.

The following relationships have already been derived:

$$I = I_s \left(e^{\frac{q}{kT} V} - 1 \right), \tag{1.7}$$

$$I_C = \alpha I_E. \tag{1.13}$$

It is obvious that since the transistor is essentially a symmetrical device, a correct model must likewise exhibit this symmetry. From the point of view of the model, *either outer terminal* relative to the base could be the emitter, with the remaining outer terminal the collector. Whether a terminal is forward- or reverse-biased depends on whether it is the emitter or collector.

The following equations cover the symmetry conditions described above:

$$I_{EF} = I_{ES} \left(e^{\frac{q V_{BE}}{kT}} - 1 \right), \tag{1.18a}$$

$$I_{ER} = -\alpha_R I_{CR}, \tag{1.18b}$$

$$I_{CF} = -\alpha_F I_{EF}, \tag{1.18c}$$

$$I_{CR} = I_{CS} \left(e^{\frac{q V_{BC}}{kT}} - 1 \right). \tag{1.18d}$$

Using the notation of Fig. 1.21, the conditions defined by these equations are depicted on the *Ebers-Moll model* of Fig. 1.22, which also defines the symbols. The representation of the polarities of the separate components of current and voltage is particularly important. As indicated, the model defines the transistor static characteristics, and applies to all polarities of bias conditions.

Since the transistor is usually used with a forward-biased emitter junction, and a reverse-biased collector junction, the Ebers-Moll model may be simplified for this condition. This simplified model is particularly well-suited to the analysis of amplifier circuits.
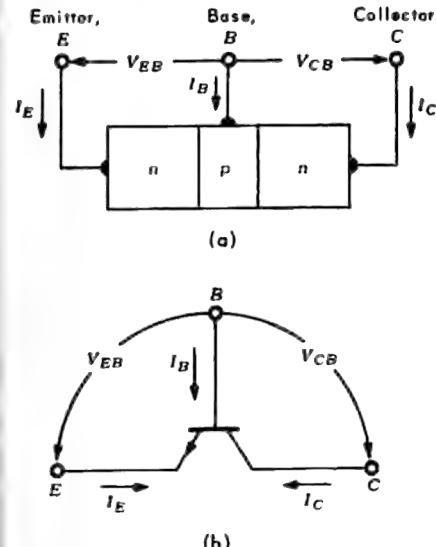
Fig. 1.21 (a) Representation of n-p-n transistor showing standard polarities of voltages and currents. (b) Alternate representation of n-p-n transistor.
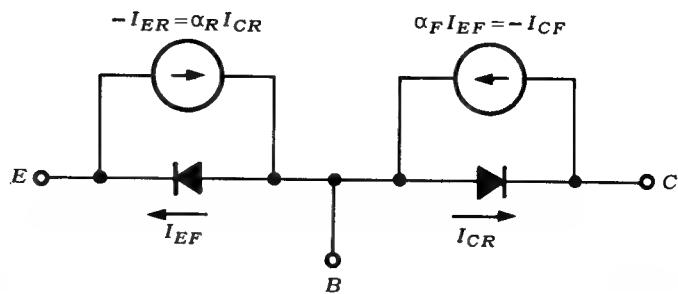
Fig. 1.22 The Ebers-Moll model of the transistor.

Figure 1.23 shows such a model or *equivalent circuit*, adapted only to the specific set of bias conditions. For these conditions,

$$\alpha_R I_{CR} \ll I_{EF};$$

therefore we neglect $\alpha_R I_{CR}$, and

$$I_{CR} = -I_{CS}.$$

A *small-signal* equivalent circuit is one which depicts the response of the transistor to small-signal inputs appearing as small variations about the bias or operating points. The small-signal model is basic to the design of small-signal a-c amplifiers.

The most useful forms of the equivalent circuit are the tee-, the hybrid, and the hybrid-π models. The tee- and hybrid models provide a simple and direct representation of transistor behavior, and are readily suited to circuit calculation at audio frequencies. The hybrid-π is useful for analyzing the performance of transistor amplifiers at high frequencies.
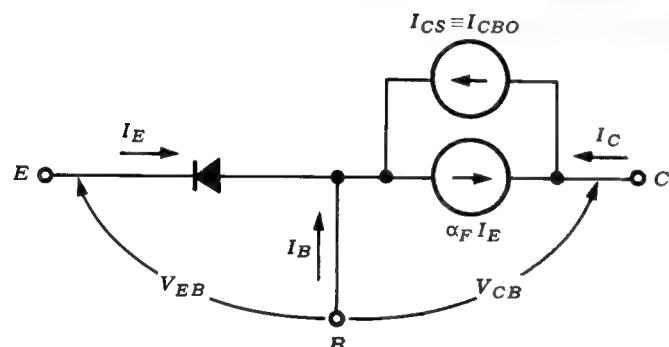
Fig. 1.23 Ebers-Moll model with forward-biased emitter junction and reverse-biased collector junction.
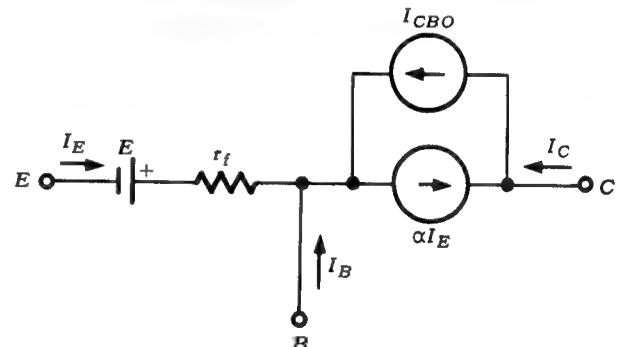
Fig. 1.24 Simplified tee-model with equivalent representation of emitter diode.
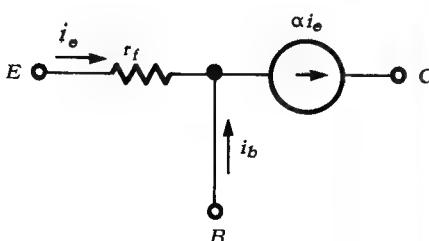
Fig. 1.25 Equivalent tee-circuit with leakage current omitted.

For the present, the tee-equivalent circuit will be developed. Referring to Fig. 1.23, the input diode of the Ebers-Moll model can be replaced by the diode equivalent circuit of Fig. 1.24. This consists of an equivalent battery E, and an incremental resistance r_f. Since the equivalent battery is, in effect, part of the d-c bias, it can be neglected in the incremental a-c equivalent circuit, leading to the further simplified model of Fig. 1.25. The leakage current component is also deleted.

This equivalent circuit is a good practical representation of the small-signal behavior of the transistor biased for amplifier application. However, it can be refined somewhat to improve accuracy.

As V_{CB} is increased, more of the carriers injected into the base from the emitter reach the collector. Recombination in the base region is then reduced.

Thus, collector current increases with V_{CB} for constant I_E. This is equivalent to connecting a resistor across the current source, αI_E. This *collector resistance*, r_c, is defined by the equation

$$\frac{1}{r_c} = \frac{\partial I_C}{\partial V_C}\bigg|_{I_E=constant} \tag{1.19}$$

An increase in V_{CB} causes an increase in emitter current for constant V_{EB}. This feedback effect can be represented by a resistance $r_{b'}$ in the base lead. In addition, the *ohmic* or *base spreading* resistance $r_{bb'}$ of the thin base region is also included in the base lead. Then the total *base resistance* $r_b = r_{b'} + r_{bb'}$ as in Fig. 1.26. Resistance r_t is labeled r_e, the *emitter* resistance.

1.6 Basic Transistor Amplifier Circuits

There are three basic transistor circuits, namely, the common-base, the common-emitter, and the common-collector connections. Their configurations derive from the choice of the input and output terminals and the terminal common to both. In each of them, the basic bias conditions are satisfied; i.e., the collector-base junction is *reverse-biased*, and the emitter-base junction is *forward-biased*. (Of course in an actual circuit, the polarities of the biasing voltage depend on whether the transistor is *p-n-p* or *n-p-n*.)

Figures 1.27–28 show the configurations of *p-n-p* and *n-p-n* transistor circuits. As will be illustrated by numerous examples throughout the book, each configuration has its own area of superiority in specific applications.

Fig. 1.26 More accurate equivalent tee-circuit for the common-base connection.
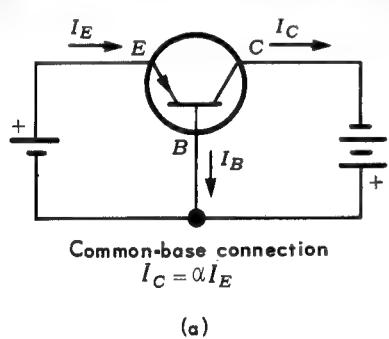
Common-base connection
$I_C = \alpha I_E$

(a)
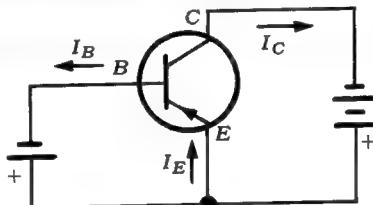
Common-emitter connection

$$I_C = \beta I_B = \left(\frac{\alpha}{1-\alpha}\right) I_B$$

(b)
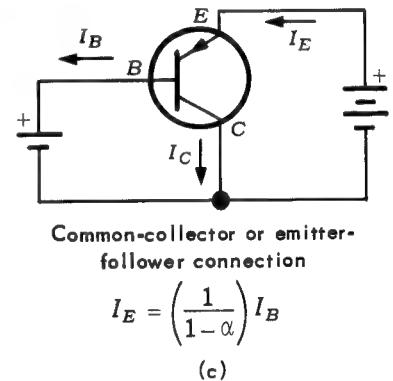
Common-collector or emitter-follower connection

$$I_E = \left(\frac{1}{1-\alpha}\right) I_B$$

(c)

Fig. 1.27 Common circuit configurations for the *p-n-p* transistor. For the above, $I_E = I_B + I_C$, $\alpha = I_C/I_E$, $\beta = I_C/I_B$. The circuits are simplified. Bias and load resistors are not shown.
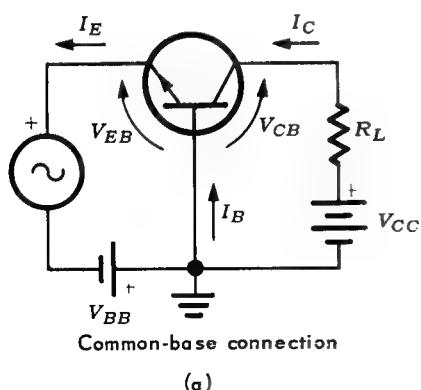
Common-base connection

(a)
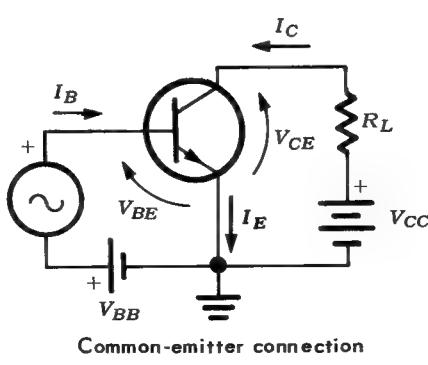
Common-emitter connection

(b)
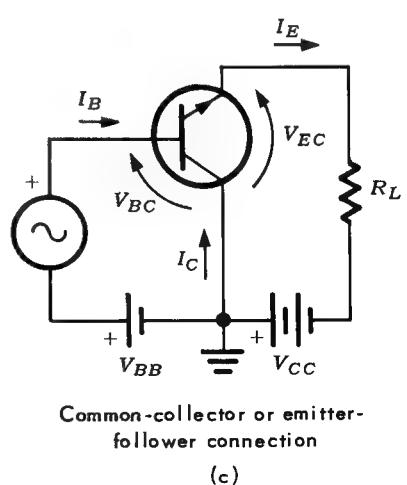
Common-collector or emitter-follower connection

(c)

Fig. 1.28 Basic transistor circuits using an *n-p-n* transistor.

Characteristic curves relating transistor currents and voltages may be used to describe the behavior of each circuit. Typical characteristic curves for the common-base connection are provided by Fig. 1.29. Corresponding sets of curves exist for the common-emitter and common-collector connections. Note that in the common-base connection, collector current flows with $V_{CB} = 0$.
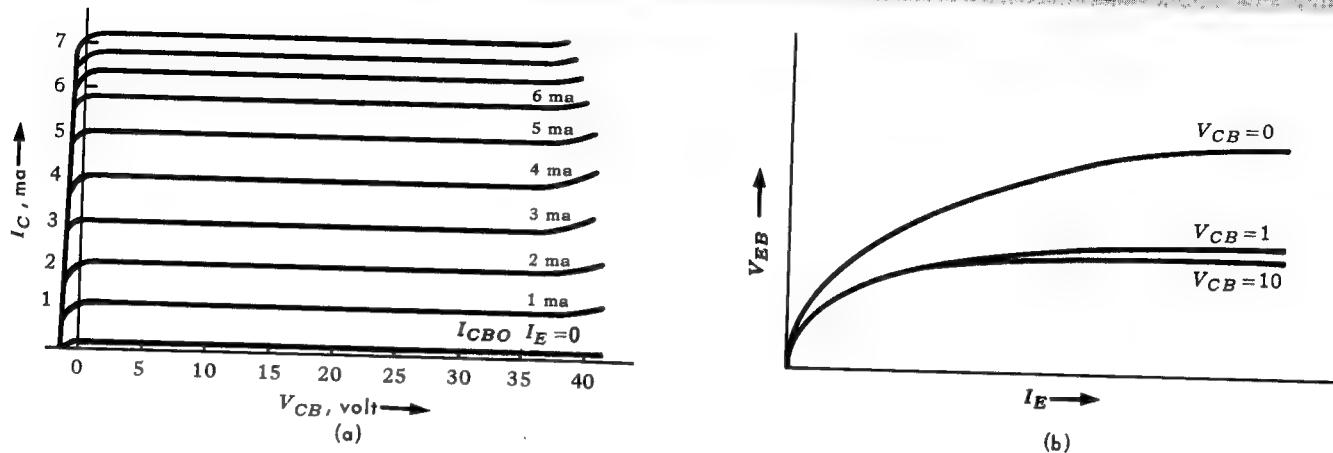
Fig. 1.29 Common-base (a) output and (b) input characteristic curves.
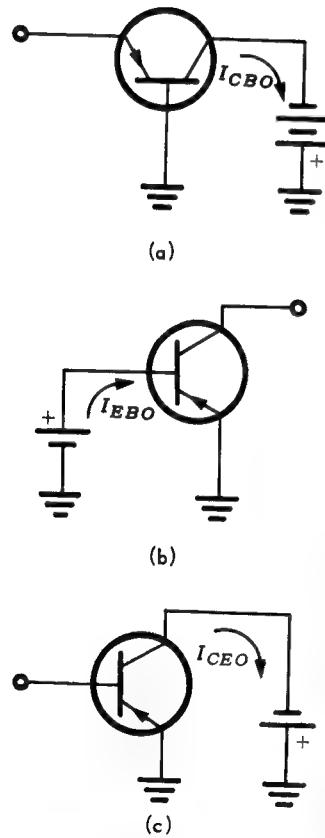
Fig. 1.30 Leakage components for the principal transistor configurations. Since the emitter circuit is not normally reverse-biased, I_{EO} is not significant.

1.7 Transistor Leakage Currents

In transistor circuits a problem arises from the variation of leakage currents with temperature in the collector-base junction. This leakage component is analogous to diode leakage (Fig. 1.9). Since the emitter-base junction is normally forward-biased, leakage current here is not significant.

Figure 1.30 a-c shows the basic leakage current components. Current I_{CO} (as it is usually called) is the common-base leakage component, and is more precisely designated as I_{CBO}; i.e., *leakage to collector from base, with emitter open-circuited*. Analogously, I_{EO} or I_{EBO} applies to the emitter-base junction when it is reverse-biased (not a normal condition) and the collector is open-circuited.

Now consider I_{CBO}. This current varies as noted in Fig. 1.9 with temperature. It is much more significant in relatively high leakage germanium transistors than in silicon transistors. As temperature increases, I_{CBO} rises, and the junction gets warmer due to the increased current component. This, in turn, further increases leakage, and may lead to an unstable condition known as *thermal runaway* (discussed in detail in Chap. 6). Leakage current variation leads to shifts in the d-c operating or bias point of the transistor, and can result in nonlinear operation.

In the connection of Fig. 1.30c, the leakage component I_{CEO} from collector to emitter, with the base connection open-circuited, is an important parameter, which can be expressed in terms of I_{CBO} and β.

PROBLEM 1.28 Find I_{CEO} as a function of I_{CBO} and β, using the transistor equation defined in Fig. 1.24, but including the leakage current I_{CBO}.

Solution: The basic equation is

$$I_C = \alpha I_E + I_{CBO}, \qquad I_E = I_C + I_B.$$

Therefore,

$$I_C = \alpha (I_C + I_B) + I_{CBO} \quad \text{or} \quad I_C (1 - \alpha) = \alpha I_B + I_{CBO}.$$

Solving for I_C,

$$I_C = \frac{\alpha}{1-\alpha} I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}.$$

Since $\beta = \alpha/(1-\alpha)$ and $1 - \alpha = 1/(1+\beta)$,

$$I_C = \beta I_B + (1+\beta) I_{CBO}.$$

The first component is the output current resulting from I_B, and the second component is I_{CEO}, for the common-emitter configuration:

$$I_{CEO} = (1+\beta) I_{CBO}. \tag{1.20}$$

There is an interesting graphical interpretation of the above expression. Refer to Fig. 1.31. Note that when $I_B = 0$, $I_C = I_{CEO}$; when collector and base currents are equal, $I_B = -I_C = I_{CBO}$ (the emitter being open).

PROBLEM 1.29 A transistor has an $I_{CBO} = 50$ μa when measured in the grounded base configuration. If $\beta = 100$, find I_{CEO}.

Solution: $I_{CEO} = (\beta + 1) I_{CBO} = 101 \times 50 \cong 5000$ μa, or 5 ma.
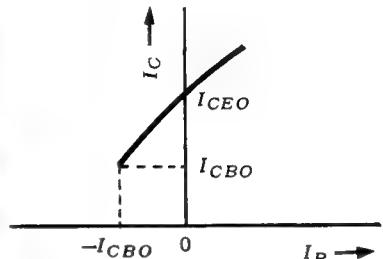
Fig. 1.31 Leakage components on an I_C vs. I_B curve. For $I_B = 0$, only the I_{CEO} leakage current flows.

1.8 Transistor Breakdown

In a transistor the conditions for breakdown, when reverse voltage is applied from collector to base, correspond roughly to the breakdown of a diode under reverse bias conditions. Usually, breakdown is an avalanche effect as previously described. However, when the base-emitter circuit is involved, the breakdown mechanism becomes more complex.

Figure 1.32 shows I_C under reverse voltage conditions which occur in transistor applications. The figure defines the most significant breakdown condi-
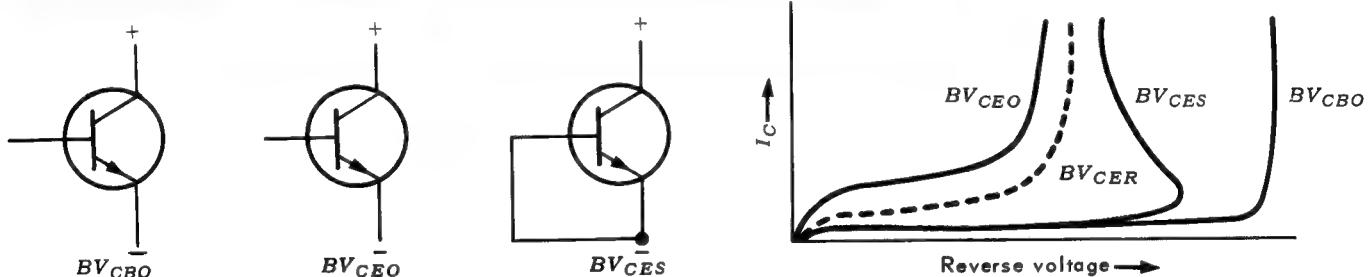
Fig. 1.32 Breakdown voltages for different transistor connections; BV_{CER} corresponds to breakdown voltage for a resistor R_1 connected from base to emitter. This curve must lie between BV_{CEO} $(R = \infty)$ and BV_{CES} $(R = 0)$.

tions. Note that the reverse voltage breakdown across the collector-base junction is the highest of the several breakdown voltages, and may not be used safely as a voltage limit in most transistor circuits. The correct breakdown voltage rating depends on the circuit, and cannot usually exceed BV_{CES}, the breakdown voltage from collector to emitter with the base connected to the emitter. Voltage breakdown is usually not harmful if current is limited, so that the junction does not overheat. Many voltage regulating devices depend on the voltage breakdown phenomenon for their behavior. Voltage breakdown of transistors will be covered in more detail in Chap. 7, as it is most important in power amplifiers.
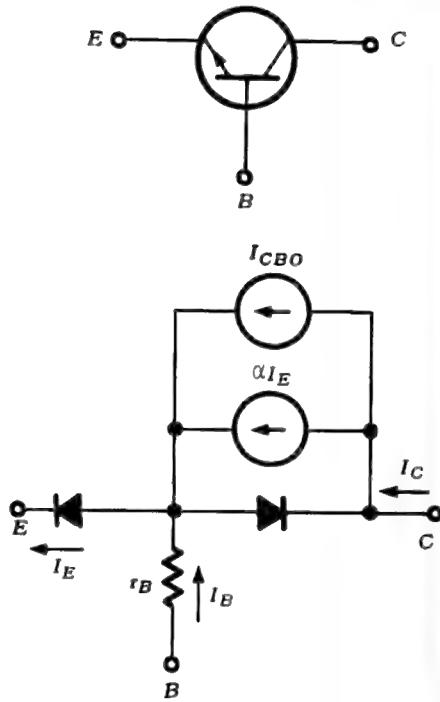
Fig. 1.33 Simplified d-c transistor equivalent circuit, common-base configuration.

Fig. 1.34 Simplified d-c transistor equivalent circuit, common-emitter configuration.

1.9 D-C Models

Let us briefly relate the tee-equivalent circuit (Figs. 1.22-25) derived from the Ebers-Moll model to the n-p-n transistor under static (d-c) conditions as shown in Fig. 1.33. The tee-equivalent circuit suggests, loosely speaking, the representation of the transistor as two back-to-back junction diodes. Output current includes two components, leakage current and amplified input αI_E, as was previously explained. The forward-biased emitter circuit impedance varies substantially with input voltage, as shown in Fig. 1.29b. This impedance, because it is of such low value, is usually swamped by external resistances. The emitter is most conveniently dealt with analytically by assuming a constant voltage drop of several tenths of a volt from emitter to base, and perhaps adding a small resistive component and working from input *currents* rather than input *voltages*. This is exactly analogous to the earlier study of diode circuits. For all except low collector voltages, the emitter-base characteristic is independent of collector voltages.

The collector is always reverse-biased for normal amplifier operation. Its leakage current varies a great deal from transistor to transistor, and also with temperature, much as does the leakage current of the diode. At very low collector voltages and emitter currents, decidedly nonlinear transistor behavior occurs. The equivalent circuit parameters vary over a wide range. Notwithstanding this variability, the tee-equivalent circuit is an invaluable aid in preliminary design, in visualizing the effects of changing external circuitry, and in the establishment of optimum circuit performance. Furthermore, the equivalent circuit itself provides a firm basis for the evaluation of the effects of these variations on overall circuit behavior. The entire subject of transistor circuit biasing is closely tied to the study of the effects of changes in transistor characteristics and methods to minimize the effects of these changes on the operating point. Shifts in the collector current with changes in transistor leakage, with forward current gain α, or with bias voltage, constitute significant problems in the maintenance of a stable operating point. An orderly study of this topic is presented in Chap. 4.

Figure 1.34 shows the d-c equivalent circuit for the common-emitter configuration. Note the leakage component $(\beta + 1)I_{CBO}$, which is the previously derived result. The base-collector current gain is β.
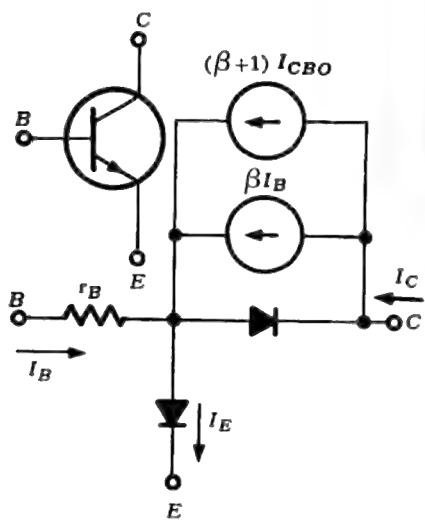
PROBLEM 1.30 The common base d-c equivalent circuit of an n-p-n transistor is shown in Fig. 1.35 driving a resistance load R_L. Using the equivalent circuit, calculate the d-c input and output resistances, R_i and R_o, respectively. Neglect leakage current I_{CBO}, and the small resistor r_E shown in the emitter circuit.

Solution: The basic equations required to find R_i are

$$V_E = -(V_{BE} + I_B R_B), \qquad I = \alpha I_E, \qquad I_B = (1 - \alpha)I_E .$$

Referring to Fig. 1.35b and combining equations,

$$R_i = \frac{V_E}{-I_E} = \frac{[(1 - \alpha) I_E R_B + V_{BE}]}{-I_E},$$

$$R_i = (1 - \alpha) R_B + \frac{V_{BE}}{I_E}.$$

For this idealized configuration, output resistance R_o is infinite as long as V_{CB} is an effective reverse bias. Output current is, of course, αI_E, regardless of R_L.
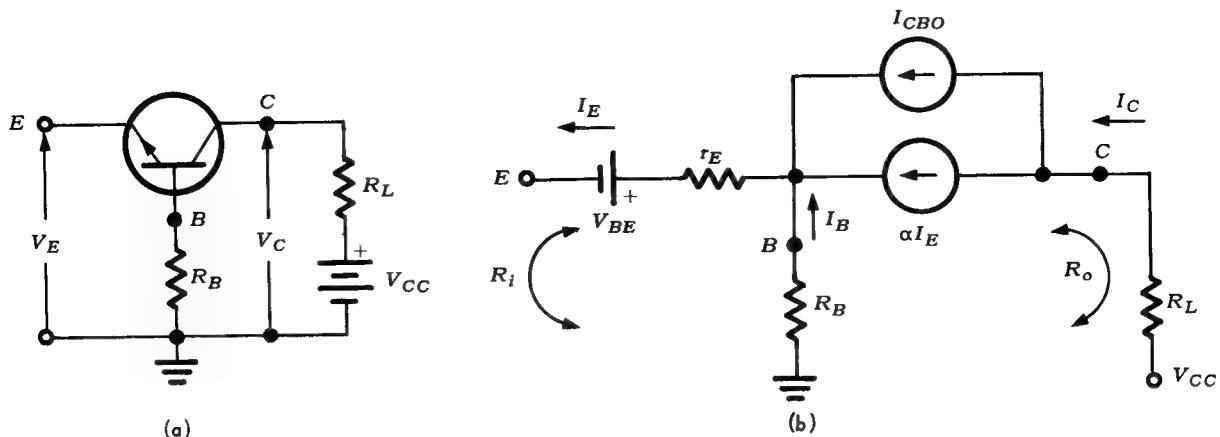
Fig. 1.35 Common-base amplifier. (a) D-c circuit, and (b) equivalent model.

PROBLEM 1.31 Analyze the circuit of Fig. 1.36 for input and output impedances (resistances), R_i and R_o, respectively. Neglect leakage components and the relatively small ohmic resistance in the base circuit.
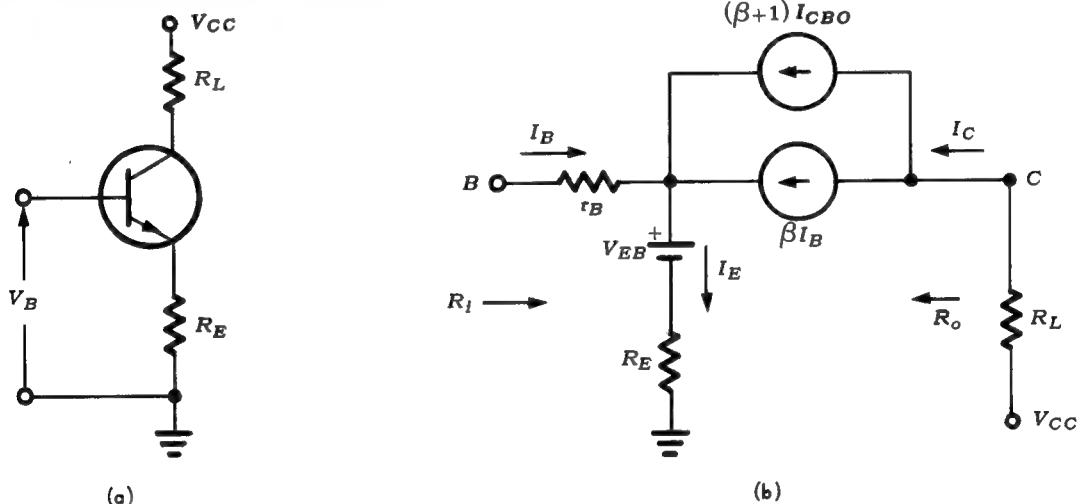
Fig. 1.36 Common-emitter amplifier. (a) D-c circuit, and (b) equivalent model.

Solution: From the equivalent circuit the basic equations are

$$V_B = V_{EB} + R_E I_E, \qquad V_C = V_{CC} - R_L I_C, \qquad I_C = \beta I_B, \qquad I_E = (\beta + 1) I_B.$$

Combining equations,

$$V_B = V_{EB} + R_E (\beta + 1) I_B.$$

The input impedance R_i is the sum of V_{EB}/I_B and $R_E (1 + \beta)$. It is characteristic of this type of circuit which features moderately high input resistance.

The output resistance, $R_o = \infty$, since the output current is supplied by an ideal current source. The output impedance is very high as long as the circuit biasing is correct.

1.10 The Hybrid-π Equivalent Circuit

The *hybrid-π* is an equivalent circuit configuration particularly suited to high-frequency calculations. It may be derived from the Ebers-Moll model of Fig. 1.22 as shown in Fig. 1.37, and some physical considerations
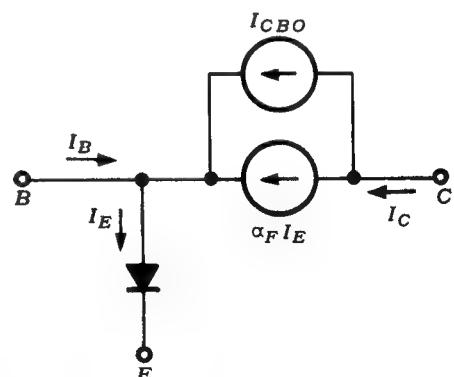
Fig. 1.37 Simplified tee-equivalent circuit used as a basis for derivation of hybrid-π equivalent circuit.
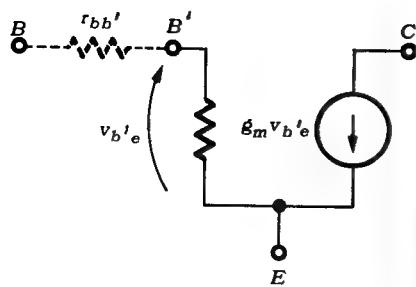
Fig. 1.38 Simplified representation of hybrid-π equivalent circuit for the common-emitter connection.

The hybrid-π circuit is derived for the common-emitter configuration in Fig. 1.38. Only the small-signal model is considered. The pertinent small-signal parameters are

$$g_m = \frac{\partial I_C}{\partial V_{BE}} \quad \text{or} \quad g_m = \frac{i_c}{v_{be}}, \tag{1.21a}$$

$$i_e = \frac{v_{be}}{r_t}. \tag{1.21b}$$

Note that lower case letters and subscripts are used for small-signal parameters. These small-signal relationships lead to the simplified equivalent circuit of Fig. 1.38, in which I_{CBO} and the d-c diode drops are not pertinent. In Fig. 1.38, B' represents a theoretical base point within the transistor, while B is the base terminal. The bulk resistance, $r_{bb'}$, intervenes. This resistance component behaves as a pure ohmic resistance.

The simplified equivalent circuit of Fig. 1.38 may be improved as shown in Fig. 1.39. The added resistors $r_{b'c}$ and r_{ce} are related to the increasing width of the collector-base junction depletion layer with increasing collector-base reverse bias. As the reverse bias voltage increases, the width of the base is effectively reduced so that α increases, while recombination in the base decreases. The increase in collector current with voltage is represented by r_{ce} in Fig. 1.39. The reduced base current is achieved in the equivalent circuit by the feedback from C to B' through $r_{b'c}$.
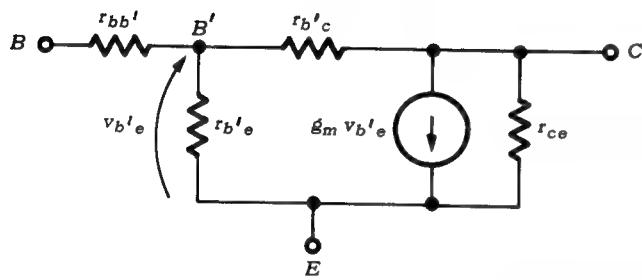
Fig. 1.39 More accurate hybrid-π equivalent circuit for the common-emitter connection.
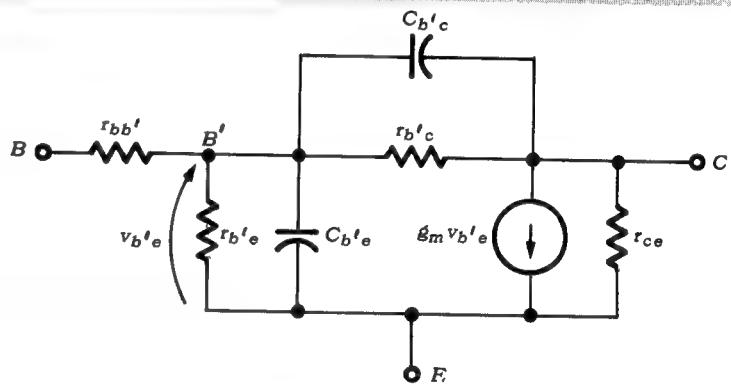
Fig. 1.40 Hybrid-π equivalent circuit incorporating capacitances for a more accurate representation of high-frequency characteristics.

High-frequency features may now be incorporated simply by including capacitances between collector and base, and emitter and base (Fig. 1.40). The capacitances are excellent representations of effective capacitances actually appearing across the junctions. This high-frequency model is relatively unaffected by frequency over a wide and useful range.

The capacitances appear primarily because the depletion layers themselves appear as capacitors. The widening of the collector-base depletion layer, for example, behaves like a reduction in capacitance. This leads to transient currents whose effects are represented very satisfactorily by the capacitors of Fig. 1.40.

1.11 Supplementary Problems

PROBLEM 1.32 Explain (a) kernel, (b) valence electron, (c) excitation level, and (d) free electrons.

PROBLEM 1.33 Explain the meaning of holes in semiconductors.

PROBLEM 1.34 What is the significance of electron-hole pair generation? What are its main causes?

PROBLEM 1.35 Define majority carrier and minority carrier current components.

PROBLEM 1.36 For $kT/q = 0.026$ v and a saturation current of 10 μa, plot I from $v = -5$ to $v = +1$. Use (1.7) and suitable increments to obtain a smooth curve.

PROBLEM 1.37 For a germanium diode, $I_s = 0.0005$ a at 25°C, determine the leakage current at 75°C.

PROBLEM 1.38 Find the incremental resistance of a diode at room temperature (25°C) with a forward current of 1 ma.

PROBLEM 1.39 Explain the behavior of a p-n junction which is (a) back-biased and (b) forward-biased.

PROBLEM 1.40 In a transistor in the common-base connection, $i_b = 0.1$ ma and $i_c = 5$ ma. Determine α and β.

PROBLEM 1.41 Why is the current gain of a transistor in the common-base connection always less than unity?

PROBLEM 1.42 Why is the voltage gain of the common-collector circuit always less than unity?

PROBLEM 1.43 For $I_{CBO} = 10$ μa in the grounded base configuration and $\beta = 50$, find I_{CEO}.

PROBLEM 1.44 Show the directions of all currents in a p-n-p transistor for the three common connections.

2

CHAPTER

TRANSISTOR
CIRCUIT ANALYSIS

2.1 Characteristic Curves
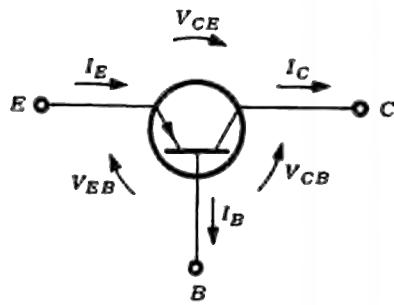
Fig. 2.1 Voltages and currents in a p-n-p transistor.

Fig. 2.2 Common-base n-p-n transistor circuit; R_L is a load resistor.

The *static characteristic curves* of the transistor define the steady-state relationships among its input and output currents and voltages. The curves are easily obtained by means of d-c measurements, and provide:

1. The basis of graphical design procedures.
2. A description of transistor performance under nonlinear conditions.
3. The starting point and final reference in the development of analytical procedures.

The characteristic curves thus constitute the basis for understanding transistor operation.

The transistor is a three-terminal device that in general has six variables comprised of three currents and three voltages as shown in Fig. 2.1. Since any two currents or any two voltages determine the third respective quantity, the actual number of variables is reduced to four. If any two of the four variables are specified, the remaining two are automatically determined.

Now in general terms, let x_1 and x_2 be a pair of specified *independent* variables, and y_1 and y_2 be the automatically determined *dependent* variables. Mathematically,

$$y_1 = f_1(x_1, x_2), \tag{2.1}$$

$$y_2 = f_2(x_1, x_2), \tag{2.2}$$

where f_1 and f_2 are the functional relationships between the independent and dependent variables.

To graphically describe y_1 and y_2, we require a separate family of curves for each. Thus, *two* families or sets of curves are necessary for a *complete* steady-state description of the transistor. From the two sets of curves, all other possible curves may be derived.

The choice of the two independent and two dependent variables from the six possible transistor variables is a matter of convenience. It may depend, for example, on which sets of curves are easier to use than others, or on the particular transistor under investigation. In general, it is most convenient to ascribe one set of curves to the transistor *input*, and the other to the transistor *output*. Thus for the common-base configuration of Fig. 2.2, V_{EB} is plotted versus the independent variable I_E for various values of the second independent variable V_{CB}, as shown in Fig. 2.3a. The output collector current I_C is plotted versus the same independent variables I_E and V_{CB} in Fig. 2.3b. This figure constitutes the *collector* family of curves.

The preferred choices of variables have become somewhat standardized by manufacturers who wish to present their data in the manner most suitable for use. Characteristic curves such as the ones illustrated by Fig. 2.3a are especially
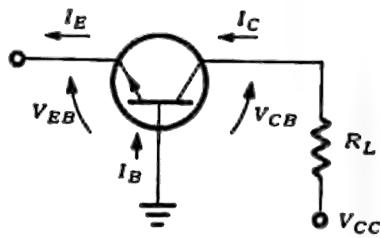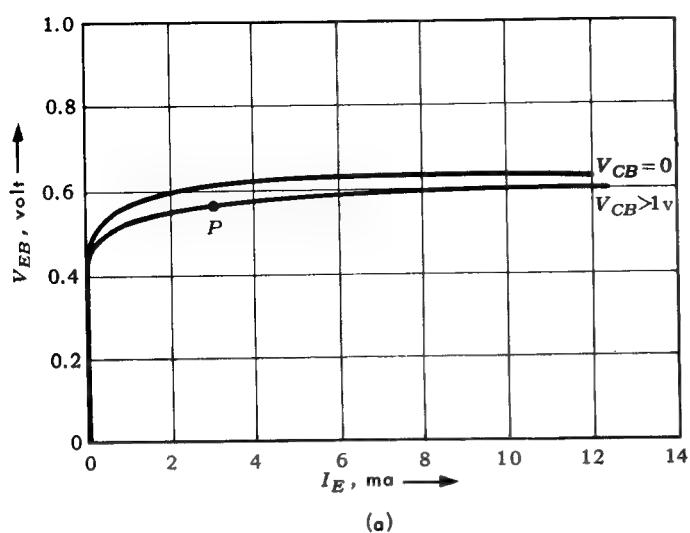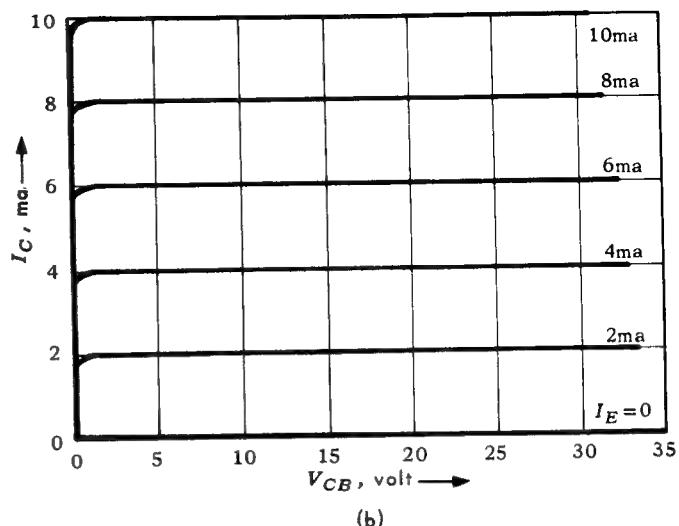
Fig. 2.3 Common-base (a) input and (b) output characteristics of the 2N929 transistor at room temperature.

convenient, because the independent variable is essentially a function of only *one* dependent variable, in this case, the emitter current I_E. Curves such as those of Fig. 2.3b, which are uniformly spaced parallel straight lines over most of the useful transistor operating range, provide a basis for *linearizing* transistor parameters and simplifying circuit analysis.

Static characteristics are directly obtainable by means of elementary methods. Figure 2.4 shows how common-base parameters are measured. The collector-base voltage and emitter current are the independent variables; the collector current and base-emitter voltage are the dependent variables (see Fig. 2.3).

Analogous to the common-base configuration of Fig. 2.2 and its curves of Fig. 2.3 are families of curves particularly descriptive of the behavior of the common-emitter and common-collector configurations. As with the common-base connection, the circuit characteristics of the latter are conveniently described by static characteristic curves as in Figs. 2.5-6, respectively. Note that the characteristics — although shown to different scales — are essentially identical be-
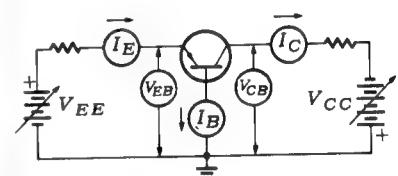
Fig. 2.4 Simple d-c circuit for obtaining the curves of Fig. 2.3. Shown is a common-base connection for a *p-n-p* transistor. With an *n-p-n* transistor, the polarities of all voltages and currents are reversed.
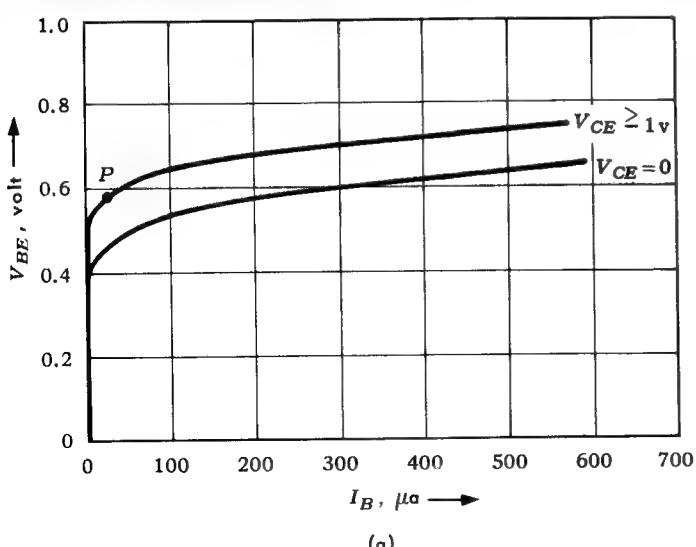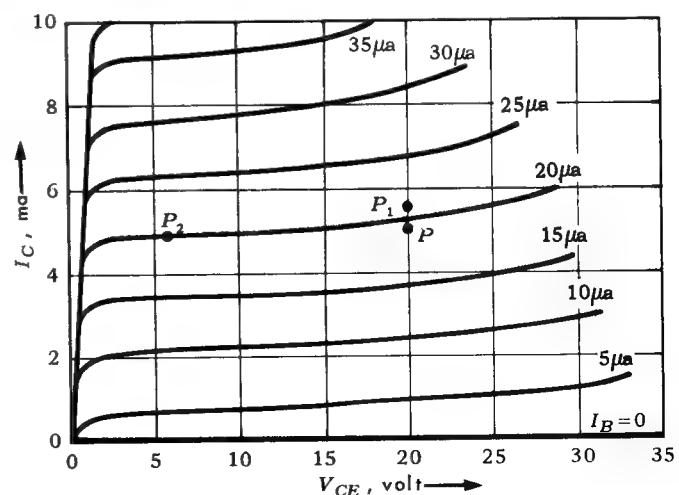
Fig. 2.5 Common-emitter (a) input and (b) output characteristics of the 2N929 transistor at room temperature.
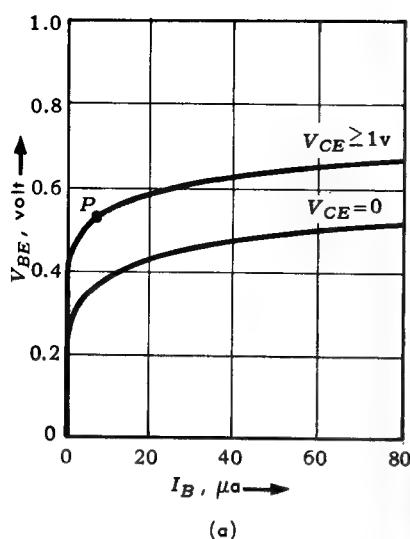
(a)
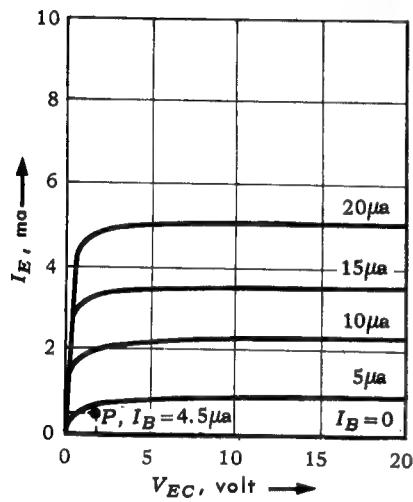
(b)

Fig. 2.6 Common-collector (a) input and (b) output characteristics at low base current of the 2N929 transistor at room temperature.

Fig. 2.7 Simplified d-c circuit for obtaining the curves of Fig. 2.5.

cause $I_E \cong I_C$, and that the curves completely define transistor circuit behavior under d-c or low-frequency conditions. Figure 2.7 shows how the curves of Fig. 2.5 may be determined experimentally.

2.2 The Operating Point

In normal operation of a transistor circuit, as for example, in a linear amplifier, currents and voltages are applied to the transistor to establish a *bias* or *quiescent operating point* in the linear region of the output characteristics (e.g., point P, Fig. 2.5b). In this region variations in input (base current) lead to proportional changes in output (collector current). The proportionality constant represents a *current gain* — comparable to β in Chap. 1 — that can be determined from the characteristic curves. By means of this constant as well as other similar ones applicable in the linear regions, the transistor may be analyzed using a *linear equivalent circuit* or *model*, just as in the case of a vacuum-tube device.

PROBLEM 2.1   The tabulation below lists sets of values of given transistor currents and/or voltages. Verify *by inspection* of the curves of Figs. 2.3 and 2.5 that the currents and/or voltages are consistent.*

$I_E = 3$ ma	$V_{CB} = 3$ v	$V_{EB} = 0.57$ v	Fig. 2.3a
$I_E = 10$ ma	$V_{CB} = 20$ v	$I_C = 10$ ma	Fig. 2.3b
$I_E = 10$ ma	$V_{CB} = 5$ v	$I_C = 10$ ma	Fig. 2.3b
$I_E = 0$	$V_{CB} = 20$ v	$I_C \cong 0$	Fig. 2.3b
$I_B = 30$ μa	$V_{CE} = 20$ v	$I_C = 8.5$ ma	Fig. 2.5a
$I_B = 10$ μa	$V_{CE} = 30$ v	$I_C = 3$ ma	Fig. 2.5a

PROBLEM 2.2   Given the common-emitter characteristics of Fig. 2.5, and $I_B = 20$ μa, and $V_{CE} = 20$ v, find the collector current and the base-emitter voltage drop.

Solution: Point P in Fig. 2.5a shows the base-emitter voltage drop $V_{BE} = 0.58$ v. Point P of Fig. 2.5b shows the collector current $I_C = 5.4$ ma.

PROBLEM 2.3   For a common-collector configuration using the 2N929 transistor, $V_{EC} = 2$ v and $I_E = 0.6$ ma.   Find the collector current I_C and the base-emitter voltage drop V_{BE}.

Solution: Use the common-collector characteristic curves of Fig. 2.6. (Note that if common-collector curves are unavailable, common-emitter curves are almost identical for most transistors.)   In Fig. 2.6b, operating point P is located.   By interpolation, $I_B = 4.5$ μa (between the $I_B = 0$ and 5 μa curves). Thus, $I_C \cong 0.6$ ma.
In Fig. 2.6a, point P is located corresponding to $I_B = 4.5$ μa, and $V_{CE} > 1$ v. The base-emitter drop is found to be $V_{BE} = 0.53$ v.

PROBLEM 2.4   The operating point of a common-emitter circuit using the 2N929 transistor is $I_C = 5.6$ ma, and $V_{CE} = 20$ v. Find I_B, V_{BE}, V_{CB}, and I_E.

*The characteristic curves of the Texas Instrument 2N929 *n-p-n* silicon transistor are used for most of the problems in this chapter.
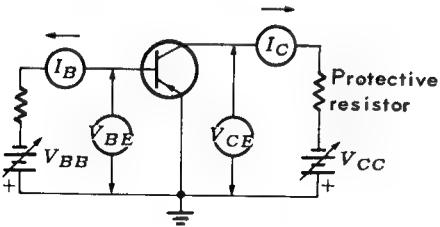
Solution: Use the characteristic curves of Fig. 2.5b to locate point P_1 at $V_{CE} = 20$ v, $I_C = 5.6$ ma. By interpolation, $I_B = 21.5$ μa. From Fig. 2.5a, $V_{BE} = 0.585$ v.

By summing voltages,

$$V_{CB} = V_{CE} - V_{BE} = 20 - 0.585 = 19.42 \text{ v.}$$

Since the algebraic sum of the three transistor currents must equal zero,

$$I_E = I_C + I_B = 6.02 \text{ ma.}$$

This analysis gives all six parameters of the operating point.

PROBLEM 2.5 For a common-base connection using the 2N929 transistor, $I_C = 5$ ma and $V_{CB} = 5$ v. Determine the remaining four voltage and current parameters for the operating point. (Note that in most data sheets only common-emitter curves are provided by the transistor manufacturer. Therefore use only the common-emitter curves of Fig. 2.5 to solve this problem.)

Solution: Start by estimating that for the conditions of this problem, V_{BE} lies between 0.5 v and 0.6 v. Therefore, for $V_{CB} = 5$ v, $V_{CE} \cong 5.6$ v. For $V_{CE} = 5.6$ v and $I_C = 5$ ma (given), from Fig. 2.5b, I_B is estimated at 20 μa (point P_2).

For $I_B = 20$ μa and $V_{CE} > 1$, $V_{BE} = 0.58$ v in Fig. 2.5a. More accurately:

$$V_{CE} = V_{BE} + V_{CB} = 5.58 \text{ v,}$$

$$I_E = I_C + I_B = 5.0 \text{ ma} + 20 \text{ } \mu\text{a} \cong 5.02 \text{ ma.}$$

All parameters are known.

The preceding examples illustrate how calculations may be made using any available family of curves. Often, however, a particular set of curves leads to greater accuracy or convenience in a specific problem. In carrying out the above and other calculations, the following points are worth remembering:

1. The emitter and collector have nearly the same current. Typically, 99% of the emitter current flows in the collector circuit. For this reason, it is usually important to specify base current, and either collector or emitter current.

2. Base-emitter current increases very rapidly with increasing base-emitter voltage. The base-emitter current is, in effect, the forward current of a diode. Excessive base-emitter voltage overheats the base-emitter junction and may burn out the unit. It is important to control base current and not apply low impedance voltage sources to the base-emitter circuit.

2.3 The Load Line

Transistors, of course, are not used as isolated elements. They are usually operated in essentially resistive networks where resistors are employed in biasing circuits to establish an operating point for the transistor, and as load elements. In a-c applications, capacitors are generally used to isolate d-c signals while permitting a-c signals to pass. The combining of transistors and resistors presents no special problem, because the current flow through the resistors determines their corresponding voltage drops, as well as the voltages appearing on the transistor terminals.

The graphical treatment of transistor circuits makes use of the concept of the *load line*. Consider, for example, the output or collector characteristics of a typical common-emitter transistor circuit shown in Fig. 2.8. Assume a collector voltage supply V_{CC} in series with a load resistor R_L. A straight line may be superimposed on the collector characteristics corresponding to the volt-ampere charac-

teristic of the battery-resistor combination. The slope of the load line represents the voltage-current characteristic of resistance R_L. The equation for the load line is

$$V_{CE} = V_{CC} - I_C R_L. \tag{2.3}$$

Setting $I_C = 0$ in (2.3), $V_{CE} = V_{CC}$; setting $V_{CE} = 0$, $I_C = V_{CC}/R_L$. These two points or intercepts define the load line whose slope equals $-1/R_L$. If $I_B = I_{B_1}$ at point P, the quiescent operating point is defined. Figure 2.8 also shows load lines (dashed lines) for increased V_{CC}, and increased V_{CC} combined with reduced R_L. The quiescent point corresponds to the given base current.

Figure 2.9 provides a numerical illustration of the use of the load line. The supply voltage $V_{CC} = 30$ v and $R_L = 5000$ Ω. The load line is superimposed on the collector characteristics. The horizontal intercept occurs at $I_C = 0$ and equals 30 v; the vertical intercept occurs at $V_{CE} = 0$ and equals 30 v/5000 Ω = 6 ma. The figure also shows the load line for $V_{CC} = 10$ v and $R_L = 2000$ Ω.
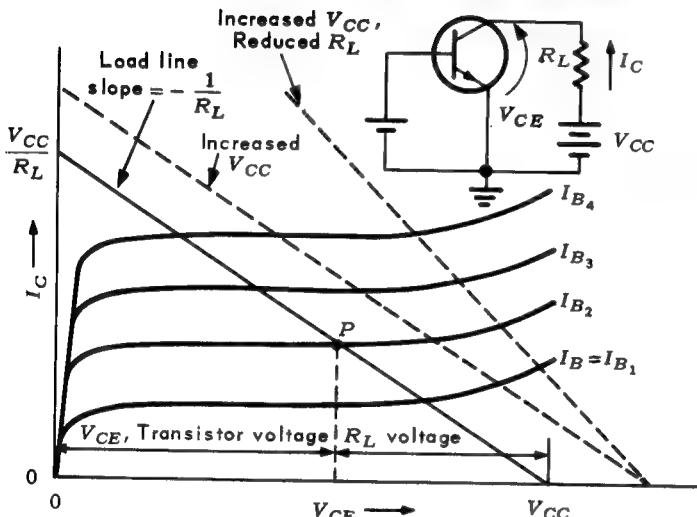
Fig. 2.8 Load lines superimposed on transistor collector characteristics for the common-emitter connection.
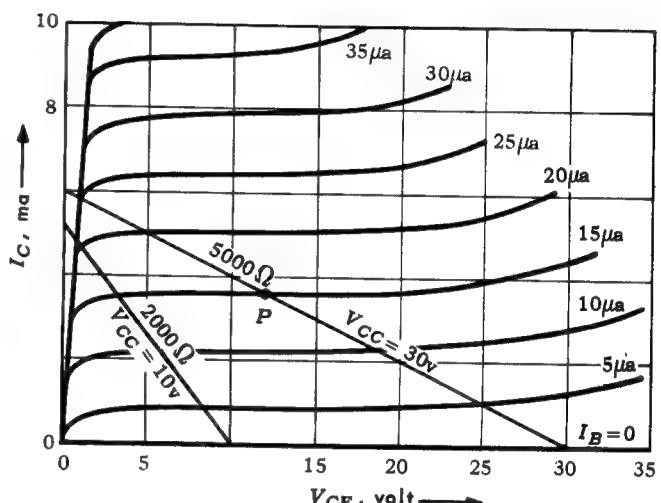
Fig. 2.9 Graphical analysis using the load line.

PROBLEM 2.6 A common-emitter circuit using the 2N929 transistor has a load resistance $R_L = 5000$ Ω in the collector circuit; $V_{CC} = 30$ v, $I_C = 3.7$ ma. Find I_B, V_{CE}, I_E, and V_{BE}.

Solution: The set of curves in Fig. 2.9 shows a superimposed load line representing the voltage-current characteristic of the collector circuit resistor. At $I_C = 3.7$ ma, $I_B = 15$ μa, and $V_{CE} = 11.6$ v. Hence, $I_E = I_C + I_B = 3.7 + 0.015 = 3.715$ ma.

From Fig. 2.6a, which is applicable to the 2N929 transistor, $V_{BE} \cong 0.57$ v for $V_{CE} > 1$ v, and $I_B = 15$ μa.

Note that both voltage across the load resistor and the collector current can be much larger than V_{BE} and I_B, indicating the possibility of large current, voltage, and power gains for the common-emitter circuit.

The load line approach is simpler to use at the transistor input whose characteristics are nearly independent of collector voltage. The load line establishes a simple intersection with the significant input characteristic to determine the operating point. Figure 2.10 shows the manner in which base current is determined from a given voltage and resistance in the base circuit. The parameters in question are indicated.
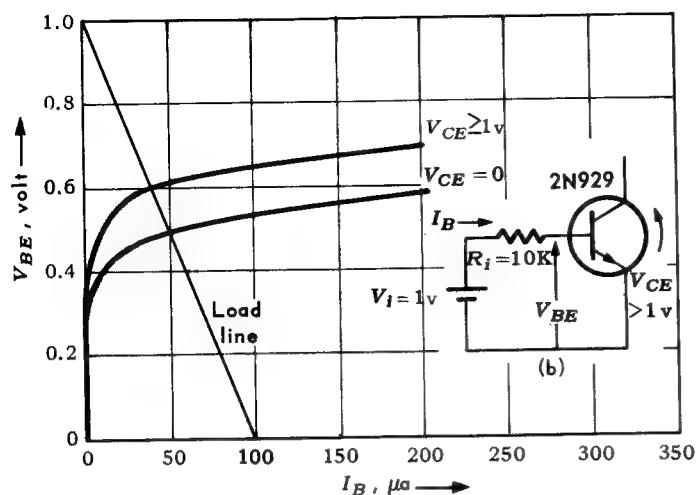
Fig. 2.10 Base circuit load line.
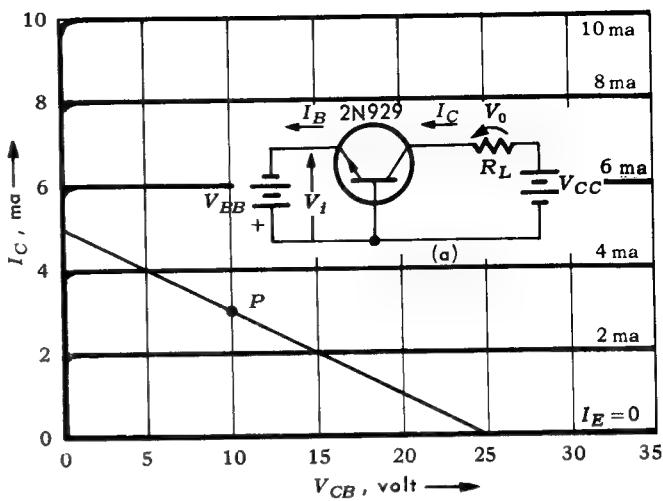
Fig. 2.11 Common-base characteristics with superimposed load line.

PROBLEM 2.7 For a common-base connection using the 2N929 transistor, $V_{CC} = 25$ v, $I_C = 3$ ma, and $R_L = 5000\ \Omega$. Find I_E, V_{BE}, and V_{CB}.

Solution: Refer to Fig. 2.11. Draw a load line corresponding to the 5000 Ω load resistance. For $I_C = 3$ ma, $V_{CB} = 10$ v corresponding to point P. Emitter current $I_E \cong 3$ ma. From Fig. 2.3a, which is applicable to the present problem, $V_{BE} = 0.57$ v.

It is worth noting that since I_B and I_C are almost equal, current amplification does not occur in the common-base configuration. Because of the higher impedance level of the output collector circuit, voltage gain can be realized.

PROBLEM 2.8 For the common-collector configuration of Fig. 2.12a using the 2N929 transistor, $V_{EE} = 30$ v, $I_E = 3.7$ ma, and $R_L = 5000\ \Omega$. Find I_B, I_C, V_{BE}, V_i, and V_o.
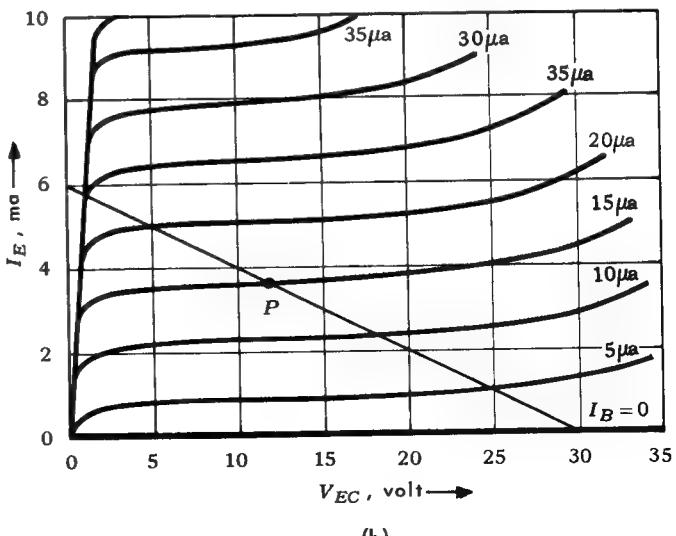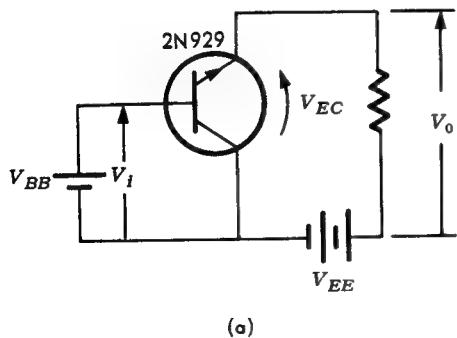
Fig. 2.12 (a) Elementary common-collector amplifier. (b) Common-collector output characteristics with superimposed load line.

Solution: Refer to Fig. 2.12b for the load line construction. From the load line,

$$V_{EC} = 11.6 \text{ v},$$

$$I_B = 15 \text{ } \mu\text{a},$$

$$V_{BE} = 0.57 \text{ v (from Fig. 2.6a)},$$

$$V_o = 3.7 \text{ ma} \times 5000 \text{ } \Omega = 18.5 \text{ v},$$

$$V_i = 3.7 \text{ ma} \times 5000 \text{ } \Omega + V_{BE} = 19.07 \text{ v}.$$

Note that for the common-collector (*emitter-follower*) circuit, V_o is always somewhat lower than V_i. There is no voltage gain. The input current I_B is much smaller, however, than the output current I_E. This configuration is essentially a current amplifier with less than unity voltage gain.
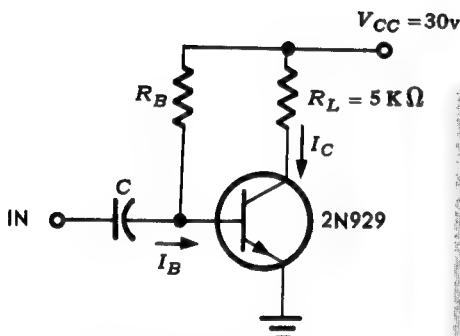
Fig. 2.13 Elementary common-emitter amplifier.

2.4 Small- and Large-Signal A-C Circuits

Refer to the basic common-emitter circuit used as an a-c amplifier in Fig. 2.13. The input coupling capacitor blocks d-c signals but permits transmission of a-c signals. In effect, relatively small a-c signals constitute a *perturbation* or small modification to the bias point.

Figure 2.14 shows the load line superimposed on the collector characteristics of the 2N929 transistor. When a bias point is chosen in the center of the transistor's linear region, the output-to-input ratio with moderate signal amplitudes is constant and may be expressed as a *gain*. To determine this gain, we need only to vary the input by a small amount about the bias point and determine the corresponding variation in output. The transistor parameters associated with small-signal excursions about the bias point, usually in the linear region, are referred to as *small-signal parameters*. Small-signal parameters actually vary somewhat with the bias point, even in the linear region.

PROBLEM 2.9   Given the common-emitter transistor amplifier of Fig. 2.13, capacitor C presents negligible impedance to a-c. Resistance R_B is adjusted so that $I_B = 15 \text{ } \mu\text{a}$. An input a-c current having a 5 μa peak-to-peak (p-p) amplitude is impressed at the input terminals. Using point-by-point graphical construction, plot i_B (t). Also repeat for a 30 μa p-p input current amplitude.

Solution: The required graphical construction is developed from Fig. 2.14. The intersections of the load line with the collector family of curves leads to the I_C vs. I_B *transfer* characteristic of Fig. 2.15. The small and large sinusoidal base currents are shown superimposed on the 15 μa quiescent current. Observe the clipping of the output, resulting from the large amplitude input current, which drives the transistor into the nonlinear region.

Large-signal parameters are based on the static d-c characteristics of the transistor over the full operating range, including nonlinear regions. As a result, they vary substantially with signal amplitude. Large-signal behavior is important in d-c amplifier design, in the design of biasing circuitry, in switching applications where the transistor is intentionally driven into nonlinear regions, and in power amplifiers where large signals are permitted, with distortion maintained within tolerable limits.
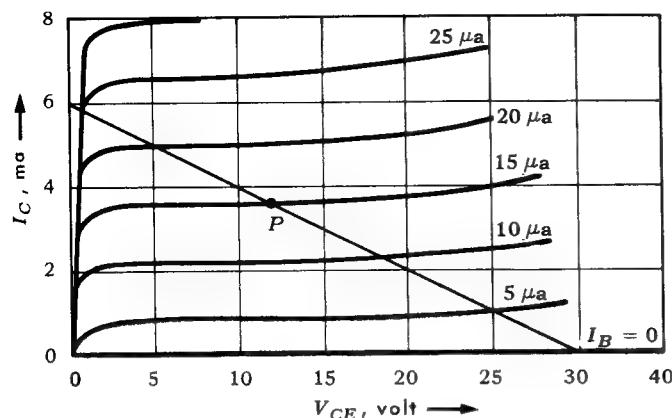
Fig. 2.14 Common-emitter output characteristics with superimposed load line.

Fig. 2.15 Collector current variation with sinusoidal base current drive. Note the large-signal distortion resulting from saturation.

PROBLEM 2.10 For the common-emitter circuit using the 2N929 transistor with a 5000 Ω load and $V_{CC} = 30$ v, find:

(a) I_B needed to operate at $I_C = 5$ ma.

(b) The power P_C dissipated in the collector junction.

(c) The d-c voltage V_L across the load, and the power P_L dissipated in the load resistor.

(d) The input d-c power P_B to the base.

(e) The variation in the parameters I_C, V_{CE}, and V_L if I_B is decreased by 5 μa.

(f) The variation in the parameters V_{BE}, P_B, and P_L if I_B is decreased by 5 μa.

Solution: (a) Refer to Fig. 2.16. Draw the load line corresponding to 5000 Ω. At $I_C = 5$ ma, $I_B = 20$ μa.

(b) D-c power is current multiplied by voltage. From Fig. 2.16, $V_{CE} = 5.3$ v, $I_C = 5$ ma, and $P_C \cong 26$ mw.

(c) The power $P_L = I_C^2 R_L = 125$ mw. The voltage $V_L = 30$ v $- 5.3$ v $= 24.7$ v.

(d) The power $P_B = V_{BE} I_B$. From the applicable curve of Fig. 2.17, $V_B = 0.58$ v. Hence, $P_B = 0.58 \times 20 \times 10^{-6} = 11.6$ μw.

(e) Since I_C must remain on the load line of Fig. 2.16, the new operating point must be at the intersection of the load line and the $I_B = (20 - 5)$ or 15 μa characteristic. From this new operating point, it is found that

Fig. 2.16 Common-emitter output characteristics with superimposed load line.

Fig. 2.17 Low level input characteristics in common-emitter connection.

$$V_{CE} = 11.6 \text{ v},$$

$$I_C = 3.7 \text{ ma},$$

$$V_L = 30 \text{ v} - 11.6 \text{ v} = 18.4 \text{ v}.$$

Use Δ notation to designate changes in these parameters with the shift in I_B :

$$\Delta V_{CE} = 11.6 - 5.3 = 6.3 \text{ v},$$

$$\Delta I_C = 3.7 - 5 \text{ ma} = -1.3 \text{ ma},$$

$$\Delta V_L = 18.4 - 24.7 = -6.3 \text{ v}.$$

The negative signs indicate that the changes are reductions.

(f) The reduction is $\Delta I_B = -5 \ \mu\text{a}$.

From Fig. 2.17, $V_{BE} = 0.569$. Hence, V_{BE} is 0.011 v lower at the reduced base current. This is most accurately estimated from the tangent at the original operating point as the rate of change of V_{BE} with I_B. Thus,

$$\Delta V_{BE} = 0.011 \text{ v},$$

$$\Delta P_B = V_{BE_2} I_{B_2} - V_{BE_1} I_{B_1} = [(0.569 \times 15) - (0.58 \times 20)] \times 10^{-6} = -3 \times 10^{-6} \text{ w}.$$

Now find $\Delta P_L = P_{L_2} - P_{L_1}$:

$$P_{L_2} = I_{C_2}^2 R_L = (3.7 \times 10^{-3})^2 \times 5000 = 58 \text{ mw} \qquad \text{at } I_{B_2} = 15 \ \mu\text{a},$$

$$P_{L_1} = I_{C_1}^2 R_L = (5 \times 10^{-3})^2 \times 5000 = 125 \text{ mw} \qquad \text{at } I_{B_1} = 20 \ \mu\text{a},$$

$$\Delta P_L = 58 - 125 = -67 \text{ mw}.$$

PROBLEM 2.11 From Prob. 2.10, determine the *d-c current gain*, i.e., the *ratio of collector to base current*. Also find the *incremental current gain*, i.e., the *ratio of a change in I_C to a change in I_B*.

Solution: From Prob. 2.10(a), $I_C = 5$ ma, and $I_B = 0.02$ ma. Thus,

$$\text{D-c current gain} = \frac{I_C}{I_B} = \frac{5}{0.02} = 250.$$

From Prob. 2.10(e), $\Delta I_C = -1.3$ ma for $\Delta I_B = -0.005$ ma. Thus,

$$\text{Incremental current gain} = \frac{\Delta I_C}{\Delta I_B} = \frac{-1.3}{-0.005} = 260.$$

PROBLEM 2.12 Using the conditions of Prob. 2.10, determine the input resistance (static d-c value), and the incremental resistance to small input changes.

Solution: Static input resistance is

$$\frac{V_{BE}}{I_B} = \frac{0.58 \text{ v}}{20 \times 10^{-6} \text{ a}} = 29{,}000 \ \Omega.$$

Incremental input resistance is

$$\frac{\Delta V_{BE}}{\Delta I_B} = \frac{-0.011}{-5 \times 10^{-6} \text{ a}} = 2200 \ \Omega.$$

Note the very large difference between static and incremental resistances. The input resistance is decidedly nonlinear.

PROBLEM 2.13 Referring to Prob. 2.10, find the ratio of output power (in R_L) to input power (to the base of the transistor) for static and incremental conditions.

Solution: Static (d-c) power gain is $\dfrac{P_L}{P_B} = \dfrac{0.125 \text{ w}}{11.6 \times 10^{-6} \text{ w}} = 10{,}800.$

From Prob. 2.10(f), incremental power gain is $\dfrac{\Delta P_L}{\Delta P_B} = \dfrac{-6.7 \times 10^{-3}}{-3 \times 10^{-6}} = 22{,}300.$

PROBLEM 2.14 For the conditions of Prob. 2.10, find the incremental voltage gain, $\Delta V_L / \Delta V_{BE}$.

Solution: From Prob. 2.10(e),

$$\Delta V_L = -6.3 \text{ v}, \qquad \Delta V_{BE} = -0.011 \text{ v}, \qquad \text{Voltage gain} = \frac{-6.3}{-0.011} = 570.$$

PROBLEM 2.15 For the 2N929 transistor in the common-emitter circuit of Fig. 2.13, calculate the *static* and *incremental output impedance* for $V_{CE} = 10$ v and $I_B = 15 \,\mu$a from the transistor characteristics.

Solution: *Incremental output impedance* is defined as $\Delta V_{CE}/\Delta I_C$ for constant I_B. To obtain it, use $\Delta V_{CE} = +5$ v (arbitrarily), so that V_{CE} ranges from 10 v to 15 v. Since ΔV_{CE} is noncritical in the linear region of the characteristics, it is selected for convenience. Referring to Fig. 2.18a-b,

$$\left. \begin{array}{llll} \text{Point } P_1\text{:} & V_{CE} = 10 \text{ v}, & I_C = 3.7 \text{ ma} \\ \text{Point } P_2\text{:} & V_{CE} = 15 \text{ v}, & I_C = 3.8 \text{ ma} \end{array} \right\} I_B = 15 \,\mu\text{a (given)}.$$

$$\text{Incremental output impedance} = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{5}{0.0001} = 50{,}000 \ \Omega = \frac{1}{h_{oe}}.$$

$$\text{Static output impedance} = \frac{V_{CE}}{I_C} = \frac{10}{0.0037} = 2700 \ \Omega = \frac{1}{h_{OE}}.$$

The much higher incremental output impedance as compared with the static value is, of course, due to transistor nonlinearity. Note that h_{OE} and h_{oe} are the static and incremental output conductances for the common-emitter connection *by definition*.

(a)

(b)
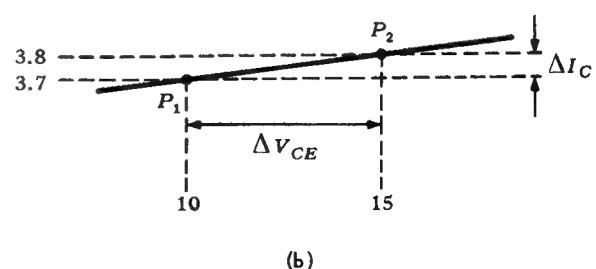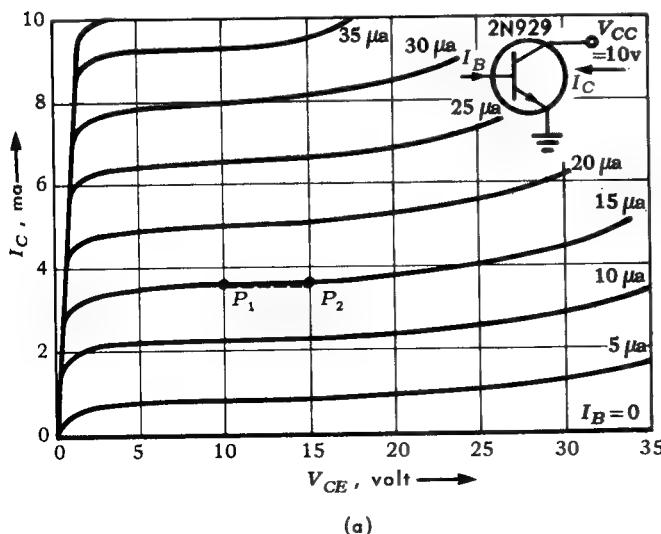
Fig. 2.18 (a) Determining transistor small-signal output impedance from the common-emitter output characteristics. (b) Enlarged view of (a) showing transistor characteristics in region of interest.

PROBLEM 2.16 For the transistor circuit of Prob. 2.15, using the characteristic curves of Fig. 2.17, calculate the *static* and *incremental input impedances*. Use a +5 μa increment for I_B.

Solution: From Fig. 2.17, for $V_{CE} > 1$ v,

$$I_B = 15\ \mu a, \qquad I_B = 20\ \mu a, \qquad \Delta I_B = 5\ \mu a,$$

$$V_{BE} = 0.569, \qquad V_{BE} = 0.580, \qquad \Delta V_{BE} = 0.011\ v,$$

$$\text{Static input impedance} = \frac{0.569}{15 \times 10^{-6}} = 38,000\ \Omega = h_{IE},$$

$$\text{Incremental input impedance} = \frac{0.011}{5 \times 10^{-6}} = 2200\ \Omega = h_{ie}.$$

Parameters h_{IE} and h_{ie} are static and incremental input impedances, respectively, in the common-emitter circuit. Note that the values of input impedance are the same as would be deduced from the calculations of Prob. 2.10, in which V_{CE} is not constant, due to the load resistance R_L. The reason is that the V_{CE} vs. I_B curve is insensitive to collector voltage except when this voltage is very low. Since the calculations are carried out with respect to $I_B = 15$ μa rather than $I_B = 20$ μa as in Prob. 2.13, h_{IE} is much higher, due to the nonlinearity of the base-emitter junction.

PROBLEM 2.17 Using the common-emitter circuit of Prob. 2.15, calculate the static and incremental ratios of collector current to base current for V_{CE} constant. Set $I_B = 15$ μa as operating point, and $\Delta I_B = +5$ μa as increment. Refer to Fig. 2.18.

Solution: Choosing $V_{CE} = 10$ v (Fig. 2.18a),

$$I_B = 15\ \mu a, \qquad I_C = 3.65\ ma,$$

$$I_B = 20\ \mu a, \qquad I_C = 5.1\ ma.$$

Static current ratio is

$$\frac{I_C}{I_B} = \frac{3.65}{0.015} = 246 = h_{FE}.$$

Incremental current ratio is

$$\frac{\Delta I_C}{\Delta I_B} = \frac{1.45 \times 10^{-3}}{5 \times 10^{-6}} = 290 = h_{fe}.$$

The static current ratio with V_{CE} constant in the common-emitter connection is designated as h_{FE}. This is known as the *forward current gain*. The *incremental forward current gain* is designated h_{fe}. These current gains may be compared with the values of Prob. 2.11. Differences are due to differences in V_{CE} for disparate operating conditions.

PROBLEM 2.18 A commonly-used two-transistor circuit is shown in Fig. 2.19. Find the quiescent operating point and the over-all incremental current gain $\Delta I_{C_2}/\Delta I_{B_1}$.

Solution: Since I_{B_1} is undefined, assume $I_{C_2} = 5$ ma, which corresponds to a 5.3 v collector voltage V_{CE_2} on the 5 KΩ load line of the applicable curve of Fig. 2.16. From Fig. 2.16, $I_{B_2} = 20$ μa, and from Fig. 2.19, $I_{B_2} = I_{E_1}$.
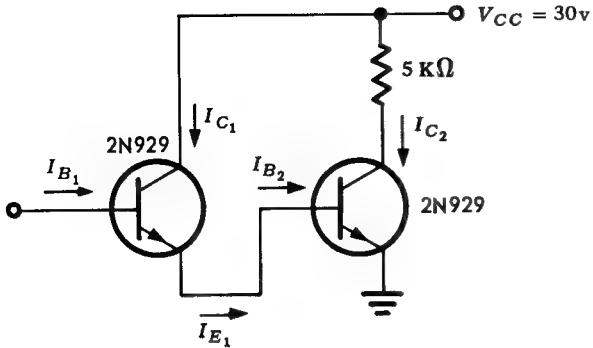
Fig. 2.19 Simplified schematic diagram for Prob. 2.18.
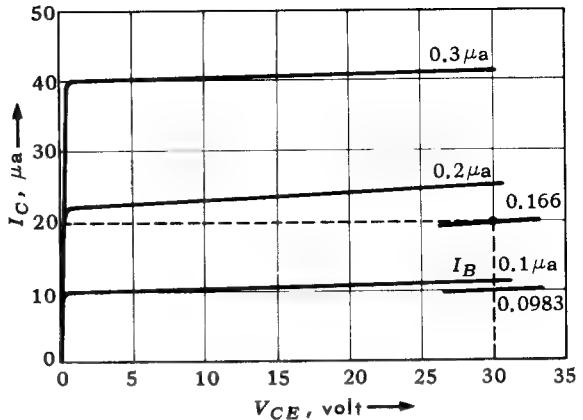
Fig. 2.20 Common-emitter output characteristics in the very low current region of the 2N929 transistor.

Consider Fig. 2.20, the common-emitter curves for the 2N929 transistor applicable to the low current region. For $I_{E_1} \approx I_{C_1} = 20 \ \mu a$ and $V_{CE_1} \cong 30$ v,

$$I_{B_1} = 0.166 \ \mu a = 166 \ ma,$$

scaled from the figure. To determine incremental gain, change I_{B_1} to $0.166/2 = 0.083 \ \mu a$, which yields (from the curves used above) $I_{B_2} = 10 \ \mu a$ and $I_{C_2} = 2.4$ ma. Hence,

$$\Delta I_{B_1} = 83 \ ma, \qquad \Delta I_{C_2} = 4.9 - 2.4 = 2.5 \ ma,$$

Incremental current gain $= \dfrac{2.5 \times 10^{-3}}{83 \times 10^{-9}} = 30,000$

for the two amplifier stages.

Fig. 2.21 Circuit for Probs. 2.19-20.

PROBLEM 2.19 In the circuit of Fig. 2.21, switch Sw is closed. Assume an operating point at $I_B = 10 \ \mu a$. Determine from the characteristic curves the incremental voltage gain for a change of $+10$ mv in V_B, the voltage from base to ground.

Solution: Refer to the curves of Figs. 2.16 and 2.22. From the slope on Fig. 2.22, 10 mv (ΔV_{BE}) corresponds to $\Delta I_B = 3 \ \mu a$ at the specified operating point.

From Fig. 2.16, points P_1 and P_2 locate the operating points for $I_B = 10 \ \mu a$ and $I_B = 13 \ \mu a$, respectively.

At P_1: $\quad I_B = 10 \ \mu a, \qquad I_C = 2.4 \ ma, \qquad V_{CE} = 18$ v.

At P_2: $\quad I_B = 13 \ \mu a, \qquad I_C = 2.9 \ ma, \qquad V_{CE} = 15.6$ v.

And therefore,

$$\Delta I_B = 3 \ \mu a, \quad \Delta I_C = 0.5 \ ma, \quad \Delta V_{CE} = -2.4 \ v.$$

Thus,

$$\text{Voltage gain } A_v = \frac{-2400 \ mv}{10 \ mv} = -240.$$

Note that a small increase in V_B leads to increased collector current and a reduced collector voltage. This is represented mathematically by the negative voltage gain. Because of the exceptional sensitivity to base-emitter voltage, the base is usually fed a *current* input. The gain calculated above is in effect the a-c gain to small-signal voltages about the quiescent operating (bias) point.

Fig. 2.22 Calculation of input impedance at an operating point from the common-emitter input characteristics.

PROBLEM 2.20   Repeat Prob. 2.19 with switch Sw open.

Solution: Because R_L and R_E are in series and the collector current is nearly equal to the emitter current, the load line of Fig. 2.16 is applicable to the present problem.

The most direct approach is to find the base to ground voltages which lead to the same operating points as P_1 and P_2 in Fig. 2.16, and then calculate voltage gain from these values. At P_1, from Prob. 2.19,

$$I_B = 10 \ \mu a, \qquad I_C = 2.4 \ ma,$$

$$I_C R_E = 2.4 \ ma \times 100 \ \Omega = 0.240 \ v.$$

At P_2,

$$\Delta V_{BE} = 10 \ mv, \qquad I_B = 13 \ \mu a, \qquad I_C = 2.9 \ ma,$$

$$I_C R_E = 2.9 \ ma \times 100 \ \Omega = 0.290 \ v.$$

The total change in base to ground (input) voltage is the increase of 10 mv in base to emitter voltage plus the change in drop across the emitter resistor. Hence,

Change in base-ground voltage $= (0.29 - 0.24) + 0.01 = 0.06$ v.

As in Prob. 2.19, the change in output $= \Delta V_{CE} = -2.4$ v :

$$\text{Effective voltage gain } A_v = \frac{-2.40}{0.06} = -40.$$

The calculated voltage gain is substantially reduced by the introduction of the R_E resistor. Note that the 10 mv contribution, which is the increase in base-emitter voltage, is a relatively minor factor in establishing gain. The drop across R_E is a *negative feedback voltage* which stabilizes gain. As V_B is increased, the increased emitter drop tends to reduce the base-emitter voltage. If the base-emitter voltage is relatively small, the base-ground voltage approximately equals the emitter resistor drop. Thus,

$$A_v \cong -\frac{R_L}{R_E} \ ,$$

as long as the voltage gain is much higher with R_E short-circuited.

Fig. 2.23 Circuit and input current for Prob. 2.21.

Fig. 2.24 Solution to Prob. 2.21.

PROBLEM 2.21   Refer to Fig. 2.23. If I_B varies as shown between 0 and 25 μa, what is the variation in output voltage V_o? What is the variation if I_B varies between 0 and 35 μa?

Solution: Figure 2.24 shows the common-emitter characteristics applicable to the present problem. A load line is drawn corresponding to $V_{CC} = 5$ v and a 1000 Ω load resistor. From the load line, it is apparent that as long as $I_B > 20 \ \mu a$, the operating point remains at P_1. The transistor is *saturated* and is said to be *on*. The collector-emitter voltage drop cannot be substantially reduced by further increases in I_B.

Similarly, if $I_B = 0$ or less (reversed in polarity), the operating point moves to P_2 where the collector-emitter drop equals V_{CC}, and the transistor is said to be *off*. Therefore, V_o varies between 5 v and about 0.7 v.

The mode of operation described here is called *switching*, since the output is either *on* or *off*, with output voltages independent of I_B in the extreme nonlinear regions.

PROBLEM 2.22   Using the circuit of Fig. 2.23 but with $R_L = 0.25 \ M\Omega$, find the variation in V_o as I_B varies between 0 and 10 μa.

Solution: Refer to Fig. 2.25, which is the common-emitter characteristic for low values of collector current. Draw the load line for a 0.25 MΩ resistor. The vertical axis intercept of the load line corresponds to a collector current of

$$\frac{5 \text{ v}}{250,000 \ \Omega} = 20 \ \mu\text{a} .$$

Collector-emitter voltage varies between 0.25 v at P_1 ($I_C = 19 \ \mu$a) and 5 v at P_2 ($I_C = 0$). The *on* collector current is determined by the circuit and not by the value of I_B, as long as I_B is greater than the value needed to sustain I_C, in this case, about 0.2 μa.

Fig. 2.25 Solution to Prob. 2.22.

2.5 Supplementary Problems

PROBLEM 2.23 From the curves of Fig. 2.5 for the 2N929 transistor, determine the operating points (a) I_C when $V_{CE} = 30$ v and $I_B = 0.01$ ma, (b) I_B when $V_{CE} = 15$ v and $I_C = 5$ ma, and (c) V_{CE} when $I_B = 30 \ \mu$a and $I_C = 8$ ma.

PROBLEM 2.24 Using the characteristics of the 2N929 transistor of Fig. 2.5, draw a load line for $V_{CC} = 30$ v and $R_L = 10,000 \ \Omega$. Find I_C and V_{CE} for $I_B = 0.01$ ma.

PROBLEM 2.25 Repeat Prob. 2.24 with $R_L = 4000 \ \Omega$.

PROBLEM 2.26 A transistor with a very high β is connected in the common-base mode. Draw a load line for $V_{CC} = 20$ v and $R_L = 5000 \ \Omega$, and find V_{CB} and I_C for $I_E = 1$ ma.

PROBLEM 2.27 For the common-emitter circuit using the 2N929 transistor with a 6000 Ω load and $V_{CC} = 30$ v, find (a) I_B needed to operate at $I_C = 5$ ma, (b) the power P_C dissipated in the collector junction, (c) the d-c voltage V_L across the load and the power P_L dissipated in the load resistor, (d) the input d-c power P_B to the base, (e) the variation in the parameters I_C, V_{CE}, and V_L if I_B is decreased by 5 μa, and (f) the changes in V_{BE}, P_B, and P_L if I_B is decreased by 5μa.

PROBLEM 2.28 From Prob. 2.27, determine the d-c current gain, i.e., the ratio of collector to base current. Also, find the ratio of a change in I_C to a change in I_B (incremental current gain).

PROBLEM 2.29 Using the conditions of Prob. 2.27, determine the input resistance (static d-c value), and the incremental resistance to small input changes.

PROBLEM 2.30 Referring to Prob. 2.27, find the ratio of output power (in R_L) to input power (to the base of the transistor) for static and incremental conditions.

PROBLEM 2.31 For the conditions of Prob. 2.27, find the incremental voltage gain $\Delta V_L / \Delta V_{BE}$.

SMALL-SIGNAL
EQUIVALENT CIRCUITS

3.1 Introduction

Although the tee-equivalent circuit introduced in Chap. 1 provides an easily visualized model of transistor behavior, there are other equivalent circuit configurations that offer characteristic advantages. Alternate models are now presented here on a *small-signal* basis, where essentially linear relationships hold for small-signal excursions about the operating (Q) point on the characteristic curves.

Figures 3.1a-b show typical transistor input and output characteristics with small-signal excursions about the operating point. Note that the assumption of linearity is more valid for the output characteristics — which are well approximated by parallel straight lines — than for the highly-curved input characteristics.
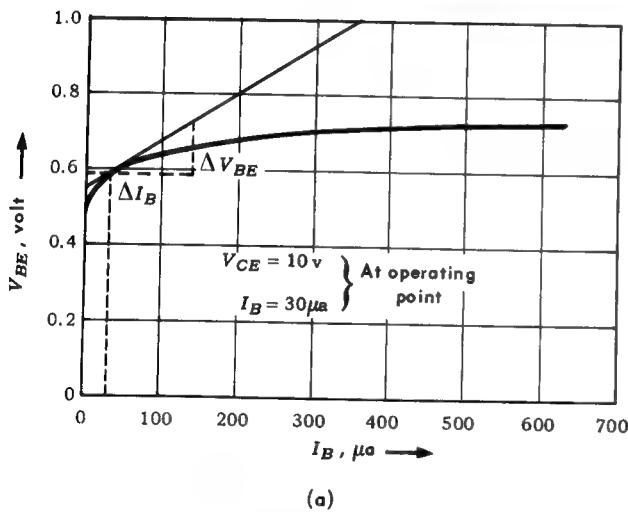
(a)
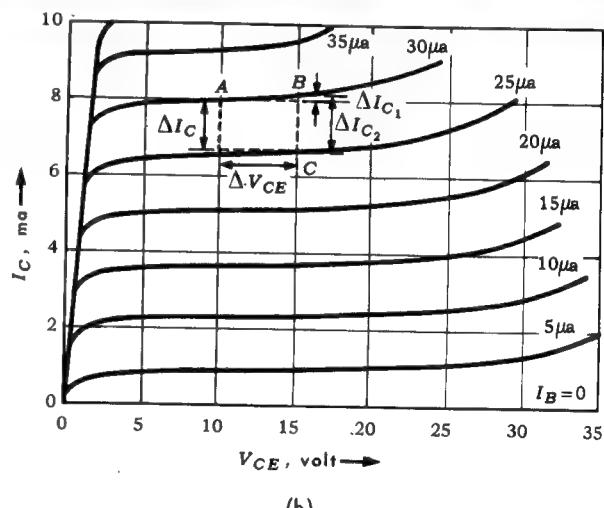
(b)
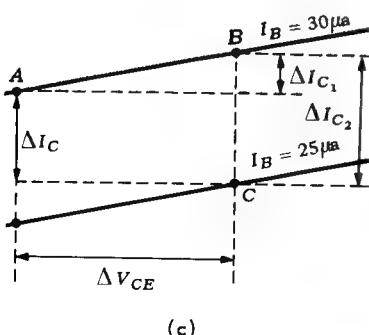
(c)

Fig. 3.1 Type 2N929 common-emitter characteristic curves. (a) Input characteristics, (b) output characteristics, and (c) enlarged view of critical region of output characteristics. Note that A = reference point; C = final point; $\Delta I_{C_1} = 0.25$ ma for $\Delta V_{CE} = 5$ v, where ΔI_{C_1} is the change in I_C due only to the change in V_{CE}; $\Delta I_{C_2} = 1.4$ ma for $\Delta I_B = 5 \ \mu a$, where ΔI_{C_2} is the change in I_C due only to the change in I_B.

3.2 Hybrid Equivalent Circuit

The *hybrid* equivalent circuit is the most widely used for describing the characteristics of the transistor. It is termed *hybrid* because

It combines both *impedance* and *admittance* parameters, known as the *h-parameters*. The ease of measurement of the *h*-parameters has contributed to its widespread adoption.

A set of *h*-parameters can be derived for any *black box* having linear elements and two input and two output terminals. Each of the three basic circuit configurations of the transistor, that is, the common-base, common-emitter, and common-collector, has a corresponding set of *h*-parameters, both for small- and large-signal operation.

The development of the hybrid equivalent circuit is illustrated by the following problem.

PROBLEM 3.1 Derive the equivalent common-emitter circuit equations from the following functional relationships that characterize the families of curves shown by Figs. 3.1a-b:

$$I_C = I_C(V_{CE}, I_B), \tag{3.1}$$

$$V_{BE} = V_{BE}(V_{CE}, I_B). \tag{3.2}$$

Solution: Both (3.1) and (3.2) may be expanded into differential forms:

$$dI_C = \frac{\partial I_C}{\partial V_{CE}}\bigg|_{I_B} V_{CE} + \frac{\partial I_C}{\partial I_B}\bigg|_{V_{CE}} I_B, \tag{3.3}$$

$$dV_{BE} = \frac{\partial V_{BE}}{\partial V_{CE}}\bigg|_{I_B} V_{CE} = \frac{\partial V_{BE}}{\partial I_B}\bigg|_{V_{CE}} I_B. \tag{3.4}$$

Assuming small-signal linear conditions, the partial derivatives,

$$\frac{\partial I_C}{\partial V_{CE}}\bigg|_{I_B}, \quad \frac{\partial V_{BE}}{\partial V_{CE}}\bigg|_{I_B}, \quad \frac{\partial I_C}{\partial I_B}\bigg|_{V_{CE}}, \quad \frac{\partial V_{BE}}{\partial I_B}\bigg|_{V_{CE}},$$

become constants whose values are determined from the characteristic curves. Hence substitution of the appropriate constants leads to the required equations.

$$V_{BE} = h_{IE}I_B + h_{RE}V_{CE}$$
$$I_C = h_{FE}I_B + h_{OE}V_{CE}$$

(a)

The above constants are given a special nomenclature because of their importance:

$$\frac{\partial I_C}{\partial V_{CE}}\bigg|_{I_B} = h_{oe}, \text{ output admittance (mhos)}, \tag{3.5}$$

$$\frac{\partial V_{BE}}{\partial V_{CE}}\bigg|_{I_B} = h_{re}, \text{ reverse voltage ratio (a numeric)}, \tag{3.6}$$

$$\frac{\partial I_C}{\partial I_B}\bigg|_{V_{CE}} = h_{fe}, \text{ forward current gain (a numeric)}, \tag{3.7}$$

$$\frac{\partial V_{BE}}{\partial I_B}\bigg|_{V_{CE}} = h_{ie}, \text{ input resistance (ohms)}. \tag{3.8}$$

$$v_{be} = h_{ie}i_b + h_{re}v_{ce}$$
$$i_e = h_{fe}i_b + h_{oe}v_{ce}$$

(b)

Now using lower case letters for small-signal operation, (3.3) and (3.4) become

$$i_c = h_{oe} v_{ce} + h_{fe} i_b, \tag{3.9}$$

$$v_{be} = h_{re} v_{ce} + h_{ie} i_b. \tag{3.10}$$

Note the *mixed* or *hybrid* nature of the *h*-parameters in (3.5) through (3.8). The second subscript *e* is applied to the individual *h*-parameters, since in this
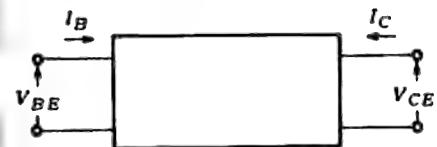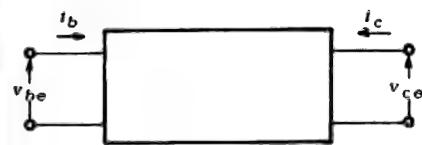
Fig. 3.2 Block diagram representation of the hybrid equivalent circuit for the common-emitter connection. (a) Large-signal parameter (d-c) and (b) small-signal parameter.

PROBLEM 3.2 Illustrate the physical significance of (3.9) and (3.10) by reference to Figs. 3.1a-c. Also establish numerical values for the parameters at the operating points on the input and output characteristics.

Solution: Consider Figs. 3.1b-c in relation to the expression

$$i_c = h_{oe} v_{ce} + h_{fe} i_b, \qquad [3.9]$$

and remember that h_{oe} and h_{fe} are assumed constant for small-signal operation. Now A is the reference point, and C, a new point that shows the shift due to changes, v_{ce} *and* i_b. On the $I_B = 30$ μa curve, I_B is constant, so that $i_b = 0$; hence $i_c = h_{oe} v_{ce}$. At point B, $V_{CE} = 15$ v and $\Delta V_{CE} = v_{ce} = 5$ v. The change $\Delta I_{CI} = i_c$ in I_C is due *only* to a change in V_{CE}. The slope of the characteristic curve is

$$\frac{\Delta I_{C_1}}{\Delta V_{CE}} = h_{oe} = \frac{0.25 \text{ ma}}{5 \text{ v}} = 50 \times 10^{-6} \text{ mhos.}$$

Now consider the component change in I_C due to a change in I_B, $V_{CE} = $ constant ($v_{ce} = 0$):

$$\Delta I_{C_2} = h_{fe} \Delta I_B, \qquad \frac{\Delta I_{C_2}}{\Delta I_B} = h_{fe}.$$

From Fig. 3.1c,

$$\Delta I_{C_2} = 1.4 \text{ ma}, \qquad \Delta I_B = 5 \text{ μa}, \qquad h_{fe} = \frac{1.4 \times 10^{-3}}{5 \times 10^{-6}} = 280.$$

With parameter values substituted in the expression for i_c,

$$i_c = h_{oe} v_{ce} + h_{fe} i_b$$
$$= 50 \times 10^{-6} v_{ce} + 280 \, i_b.$$

A similar procedure can be followed with respect to the input characteristics of Fig. 3.1a, whose defining equation (3.10) is repeated here:

$$v_{be} = h_{re} v_{ce} + h_{ie} i_b. \qquad [3.10]$$

The input characteristic curves, for all but very low values of V_{CE}, are almost independent of V_{CE}. Thus, for practical operating points, h_{re} may be set equal to zero, so that $v_{be} = h_{ie} i_b$.   From Fig. 3.1a, at $I_B = 30$ μa,

$$\Delta I_B = 100 \text{ μa}, \qquad \Delta V_{BE} = 0.13 \text{ v},$$

$$\frac{\Delta V_{BE}}{\Delta I_B} = \frac{v_{be}}{i_b} = \frac{0.13}{100 \times 10^{-6}} = 1300 \ \Omega,$$

$$h_{ie} = 1300 \ \Omega,$$

and (3.10) reduces to $v_{be} = 1300 \, i_b$.

$$v_{be} = i_b h_{ie} + h_{re} v_{ce}$$

(a)

$$i_c = h_{oe} v_{ce} + h_{fe} i_b$$
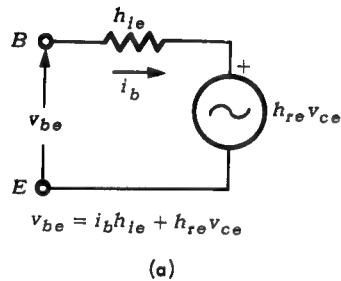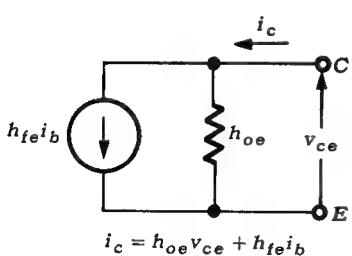
(b)

Fig. 3.3 Equivalent circuit (model) representation of the common-emitter configuration. (a) Input side and (b) output side.

PROBLEM 3.3 Show how (3.9) and (3.10) may be represented by equivalent circuits.

Solution: Figures 3.3-4 show the set of equations and the equivalent circuit representations. It is seen that the circuit equations are identical with (3.9) and (3.10). The equivalent circuit or model provides an exceptionally simple basis for calculation.

$$v_{be} = h_{ie} i_b + h_{re} v_{ce}$$

$$i_c = h_{fe} i_b + h_{oe} v_{ce}$$

Fig. 3.4 Complete hybrid parameter model for the common-emitter connection. This circuit applies to small-signal operating conditions.

PROBLEM 3.4 For the 2N929 transistor whose characteristic curves and operating points are defined in Figs. 3.5a-b, compute the *h*-parameters for the common-emitter connection, and draw the equivalent circuit.

Solution: The output operating point, *A*, is defined in Fig. 3.5b as

$$I_B = 15 \ \mu a, \qquad V_{CE} = 12 \ v.$$

Proceeding as before in Probs. 3.1-2,

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} \bigg|_{I_B} = \frac{0.3 \times 10^{-3}}{10} = 30 \times 10^{-6} \text{ mhos},$$

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B} \bigg|_{V_{CE}} = \frac{1.4 \times 10^{-3}}{5 \times 10^{-6}} = 290,$$

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \bigg|_{V_{CE}} = \frac{0.22}{100 \times 10^{-6}} = 2,200 \ \Omega,$$

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \bigg|_{I_B} = 0 \,(\text{essentially}), \text{ for } V_{CE} > 1 \text{ v.}$$

The equivalent circuit corresponding to these parameters is shown in Fig. 3.6.
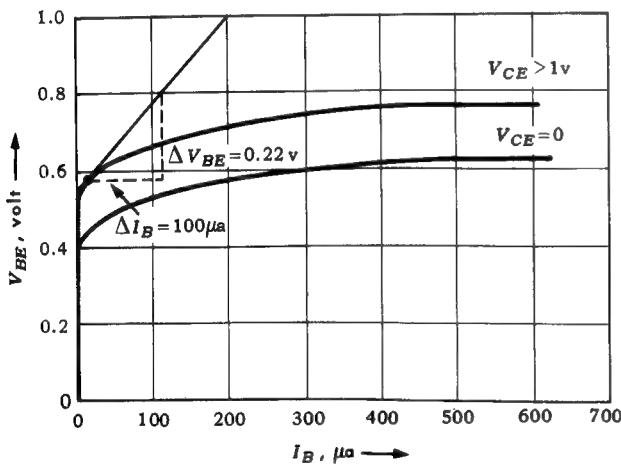
(a)
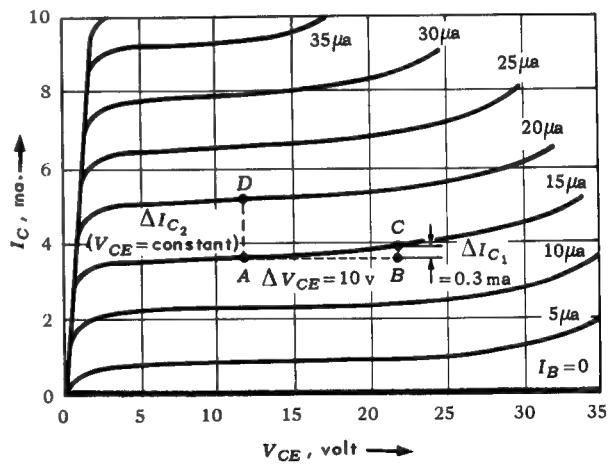
(b)

Fig 3.5 Computing *h*-parameters for Prob. 3.4. (a) Input characteristics and (b) output characteristics.

The equivalent circuit based upon small-signal variations about an operating point is, of course, immediately adaptable to the analysis of small-signal a-c amplifiers. The calculation of amplifier performance is merely the determination of output signals with given input signals.

Fig. 3.6 Equivalent circuit corresponding to the *h*-parameters derived in Prob. 3.4.

PROBLEM 3.5 We are given the circuit of Fig. 3.7 whose operating conditions and parameters correspond to those of Fig. 3.6. The input capacitor is assumed to have zero a-c impedance.

(a) For an input signal $v_g = 10$ mv rms, calculate the currents i_b and i_c, and the voltage across and power in R_L.

(b) Calculate the current gain $A_i = i_c/i_b$. (This is not the same as h_{fe}, since the external resistance R_L enters into the calculations. Parameter h_{fe} is defined for short-circuit conditions; i.e., $v_{ce} = 0$.)

(c) Calculate the voltage gain $A_v = v_{ce}/v_{be}$.

(d) Calculate the power gain, i.e., the ratio of a-c load power to transistor a-c input power.

(e) Calculate the input impedance Z_i.

(f) Calculate the output impedance Z_o.

It is assumed that $h_{re} = 0$. This is generally a valid or realistic assumption for small-signal operation which results in simplified calculations.
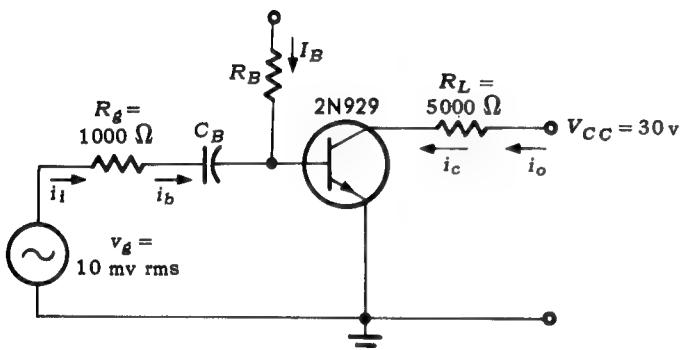
Fig. 3.7 Circuit for Prob. 3.5. The bias point is set at a base current of 15 μa supplied through R_B. Capacitor C_B blocks the d-c bias current to prevent its flowing in the low impedance generator circuit, components R_B and C_B are neglected in calculations, and v_g and R_g are a-c generator voltage and internal resistance, respectively.
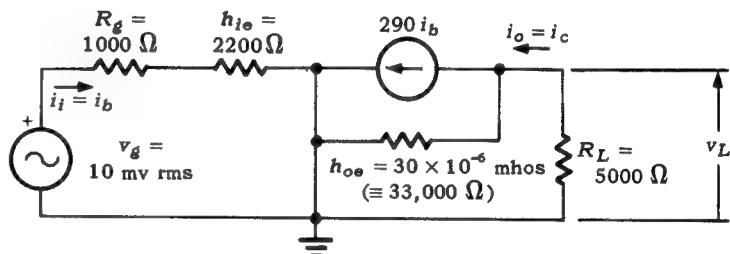
Fig. 3.8 The a-c hybrid model corresponding to the circuit of Fig. 3.7.

Solution: The first step is to draw an a-c model for the circuit of Fig. 3.7, as shown by Fig. 3.8. Calculations are then made in a straightforward manner using ordinary circuit theory.

(a) To calculate i_b:

$$i_b = \frac{v_g}{R_g + h_{ie}} = \frac{10^{-2}}{1000 + 2200} \cong 3.1 \times 10^{-6} \text{ a.}$$

The current generator develops $h_{fe} i_b$, or $290 \times 3.1 \times 10^{-6} = 0.90$ ma.

The current source output divides between h_{oe} and R_L in accordance with Ohm's law:

$$i_c = h_{fe} i_b \left(\frac{\dfrac{1}{h_{oe}}}{R_L + \dfrac{1}{h_{oe}}} \right) = 0.90 \left(\frac{1}{R_L h_{oe} + 1} \right) \text{ ma} = 0.90 \left(\frac{1}{5000 \times 30 \times 10^{-6} + 1} \right)$$

$$= \frac{0.90}{1.15}$$

$$\cong 0.78 \text{ ma.}$$

The voltage across R_L is $v_L = 5000 \times (-0.78 \times 10^{-3}) = -3.9$ v rms. The voltage is negative because of the assumed current and voltage polarities of Fig. 3.8. The power dissipated in $R_L = 0.78 \times 3.9$ v $= 3.04$ mw.

(b) The calculation of current amplification is

$$A_i = \frac{i_c}{i_b} = \frac{0.78 \times 10^{-3}}{3.1 \times 10^{-6}} = 252.$$

(c) To calculate voltage amplification, input voltage is taken as the input voltage *at the transistor base:*

$$A_v = \frac{v_L}{v_{be}} = \frac{-3.9}{i_b h_{ie}} = \frac{-3.9}{3.1 \times 10^{-6} \times 2.2 \times 10^3} = \frac{-3.9}{6.8 \times 10^{-3}} = -574.$$

Note that input voltage $= i_b Z_i$ where $Z_i \cong h_{ie}$. The minus sign in the voltage gain calculation arises because i_c is flowing away from the assumed positive side of of R_L. In the common-emitter circuit at low frequencies, the output voltage is $180°$ out of phase with the input signal.

(d) Calculation of power gain: Load power, previously calculated, is 3.04 mw,

$$\text{Power input} = i_b \times v_{be} = (3.1 \times 10^{-6})(6.8 \times 10^{-3}) = 21 \times 10^{-9} \text{ w,}$$

$$\text{Power gain} = \frac{3.04 \times 10^{-3}}{21 \times 10^{-9}} \cong 145,000,$$

or calculated somewhat differently,

$$\text{Power gain} = |A_i A_v| = 252 \times 574 \cong 145,000.$$

(e) Input impedance $\cong h_{ie} = 2200 \ \Omega$.
(f) Output impedance $\cong 1/h_{oe} = 33,000 \ \Omega$. This is the a-c impedance seen looking toward the transistor from R_L.

3.3 Tee-Equivalent Circuit

The tee-equivalent circuit (Fig. 3.9) provides a close approximation of transistor behavior. Within the scope of the linearity assumptions, it is easy to relate its circuit parameters to physical ones. However, it is difficult to measure tee-parameters directly with high accuracy, in contrast to the ease with which h-parameters may be measured. The best way therefore to determine tee-parameters is to convert from known h-parameters.

The basis for converting between h- and tee-parameters depends on the necessary identity of behavior of each configuration for different input and output conditions. The conditions that will be used in the subsequent analysis are as follows:

1. Input impedance is measured with output short-circuited.
2. Output impedance is measured with input open-circuited.
3. Reverse voltage ratio is measured with input open-circuited.
4. Forward current gain is measured with output short-circuited.

For the above conditions, all valid equivalent circuits must yield the same numerical results.

PROBLEM 3.6 Using the common-emitter hybrid and tee-equivalent circuits of Figs. 3.9-10, calculate the four quantities listed above. Also, develop comparable equations for the two circuit configurations.
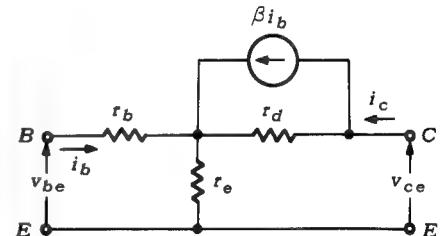
Fig. 3.9 The tee-equivalent circuit for the common-emitter connection. The parameters r_b, r_e, r_d, and β are constant only for small-signal operation. The fixed bias currents and voltages are not shown.
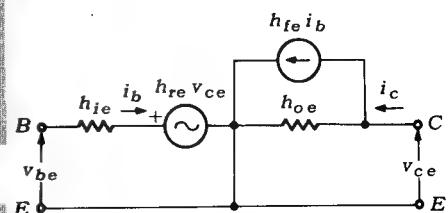
Fig. 3.10 Common-emitter hybrid model.
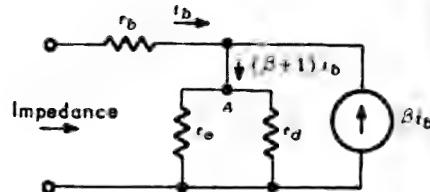
Fig. 3.11 Calculation of input impedance of the tee-configuration.

Solution: (a) To calculate the input impedance for the tee-equivalent circuit, redraw Fig. 3.9 as shown in Fig. 3.11, with the output short-circuited. The current entering node A is $(\beta + 1)i_b$. The voltage across the parallel shunting resistors is therefore,

$$i_b (\beta + 1) \frac{r_e r_d}{r_e + r_d}.$$

The input voltage equals

$$i_b r_b + i_b (\beta + 1) \frac{r_e r_d}{r_e + r_d}.$$

Since the input voltage $= Z_i i_b$, where Z_i is the input impedance,

$$Z_i = r_b + (\beta + 1) \frac{r_e r_d}{r_e + r_d}. \tag{3.11a}$$

The input impedance of the hybrid equivalent circuit is determined by inspection of Fig. 3.10. Note that $h_{re} v_{ce} = 0$, since the output (v_{ce}) is short-circuited. Therefore,

$$Z_i = h_{ie}. \tag{3.11b}$$

(b) To determine the output impedance from the tee-equivalent circuit of Fig. 3.9, the input is open-circuited. Since $i_b = 0$, $\beta i_b = 0$, and the output impedance Z_o is

$$Z_o = r_d + r_e. \tag{3.12a}$$

Analogously, referring to Fig. 3.10, with $i_b = 0$ and therefore $h_{fe} i_b = 0$,

$$Z_o = \frac{1}{h_{oe}}. \tag{3.12b}$$

(c) The reverse voltage ratio is also calculated for $i_b = 0$. From Fig. 3.9,

$$v_{be} = v_{ce} \frac{r_e}{r_e + r_d}.$$

and for the hybrid equivalent circuit of Fig. 3.10,

$$v_{be} = v_{ce} h_{re}.$$

(d) Referring to Fig. 3.11 to calculate the forward current gain in the tee-equivalent circuit, the current in r_d is

$$i_b (\beta + 1) \frac{r_e}{r_e + r_d}.$$

Solving for i_c,

$$i_c = \beta i_b - (\beta + 1) i_b \frac{r_e}{r_e + r_d}.$$

Since $r_e \ll r_d$, the following approximation is valid:

$$i_c \cong \beta i_b, \text{ or } \frac{i_c}{i_b} \cong \beta.$$

For the hybrid circuit of Fig. 3.10, since the output is short-circuited for the forward current gain calculation,

$$i_c = h_{fe} i_b; \quad \frac{i_c}{i_b} = h_{fe}.$$

Notice the simplicity with which results are obtained from the hybrid equivalent circuit. The simple relationships between easily measureable circuit characteristics and hybrid parameters are a prime reason for using h-parameters.

PROBLEM 3.7 Using the results of Prob. 3.6, derive formulae for conversion between tee- and h-parameters.

Solution The equations derived in Prob. 3.6 lead naturally to expressions for the h-parameters in terms of the tee-parameters. These are listed below

$$Z_i = h_{ie} = r_b + (1 + \beta) \frac{r_e r_d}{r_e + r_d} . \tag{3.13}$$

$$Z_o = \frac{1}{h_{oe}} = r_e + r_d, \qquad h_{oe} = \frac{1}{r_e + r_d} . \tag{3.14}$$

$$h_{re} = \frac{r_e}{r_e + r_c} . \tag{3.15}$$

$$h_{fe} = \beta. \tag{3.16}$$

The above formulae may be solved for tee-parameters in terms of h-parameters. Obviously,

$$\beta = h_{fe}.$$

Dividing (3.15) by (3.14),

$$r_e = \frac{h_{re}}{h_{oe}} . \tag{3.17}$$

From (3.14) and (3.17),

$$r_d = \frac{1}{h_{oe}} - r_e = \frac{1}{h_{oe}} - \frac{h_{re}}{h_{oe}} = \frac{1 - h_{re}}{h_{oe}} . \tag{3.18}$$

Solving for r_b in (3.13),

$$r_b = h_{ie} - (1 + \beta) \frac{r_e r_d}{r_e + r_d} .$$

However,

$$\frac{r_e r_d}{r_e + r_d} = \frac{\dfrac{h_{re}}{h_{oe}} \left(\dfrac{1 - h_{re}}{h_{oe}} \right)}{\dfrac{h_{re}}{h_{oe}} + \dfrac{1 - h_{re}}{h_{oe}}} = h_{re} \left(\frac{1 - h_{re}}{h_{oe}} \right) .$$

But $\beta = h_{fe}$ and

$$r_b = h_{ie} - (1 + h_{fe}) h_{re} \left(\frac{1 - h_{re}}{h_{oe}} \right) .$$

Since $h_{re} \ll 1$,

$$r_b \cong h_{ie} - (1 + h_{fe}) \frac{h_{re}}{h_{oe}} . \tag{3.19}$$

PROBLEM 3.8 Using the results of Prob. 3.7, convert the hybrid equivalent circuit of Fig. 3.6 to the corresponding tee-equivalent circuit for the common-emitter connection.

Fig. 3.12 Equivalent tee-circuit, identical to the hybrid circuit of Fig. 3.6 because h_{re} is assumed to be zero.

Because h_{re} is so small, it is generally not feasible to determine it from the transistor static characteristics. Instead, it may be obtained by making small-signal a-c measurements on the transistor. With the transistor properly biased, a small a-c voltage is applied to the output with the input circuit open (to a-c), as in Fig. 3.13. The ratio of the open-circuit voltage to the applied voltage is h_{re}. This technique is also used for determining h_{rb} and h_{rc}.

For example, using the above procedure, the value of h_{re} for the 2N929 transistor at $V_{CE} = 12$ v and $I_B = 15$ μa was found to be 2×10^{-4}. This means that a 1 v change in V_{CE} produces a 0.2 mv change in the coupled base-to-emitter voltage. This magnitude of change cannot be seen on the characteristic curves, which explains why the previously derived h_{re} equals zero.

PROBLEM 3.9 For the equivalent circuit of Fig. 3.8, determine the errors in voltage gain (A_v) and current gain (A_i) resulting from the assumption that $h_{re} = 0$. (In this problem, $h_{re} = 2 \times 10^{-4}$.)

Solution: The equivalent circuit with the same operating point as in Prob. 3.5 but with the $h_{re}v_{ce}$ voltage source inserted, is shown in Fig. 3.14. It will be recalled that $v_{ce} = -3.9$ v, yielding an $h_{re}v_{ce} = 2 \times 10^{-4} \times -3.9 \approx -0.8$ mv rms. If i_b is held constant, v_d must decrease by 0.8 mv to 9.2 mv. For this condition, the output current i_c is unchanged. The input voltage v_{be} becomes

Fig. 3.13 Simplified circuit diagram showing how to measure h_{re}.

$$v_{be} = 9.2 \times \frac{h_{ie}}{h_{ie} + R_g} = 9.2 \times \frac{2200}{2200 + 1000} = 6.3 \ \text{mv,}$$

$$A_v = \frac{-3.9}{6.3 \times 10^{-3}} = -618 \ \text{(vs. } -574, \text{ neglecting } h_{re}).$$

The approximate gain is 7% lower than the "exact" value. This approximation error is almost always acceptable, since the variability in transistor parameters is much greater than 7%. The current gain is unchanged, because it depends primarily on h_{fe}.

PROBLEM 3.10 Obtain the tee-equivalent circuit from the hybrid model of Fig. 3.14.

Solution: The *h*-parameters are

$$h_{ie} = 2200 \ \Omega,$$
$$h_{oe} = 30 \times 10^{-6} \ \text{mhos},$$
$$h_{re} = 2 \times 10^{-4},$$
$$h_{fe} = 290.$$

Substitute in the conversion formulae:

$$\beta = h_{fe} = 290,$$

$$r_d \cong \frac{1}{h_{oe}} = 33,000 \ \Omega,$$

$$r_e = \frac{h_{re}}{h_{oe}} = \frac{2 \times 10^{-4}}{30 \times 10^{-6}} = 6.67 \ \Omega,$$

$$r_b = h_{ie} - (1 + h_{fe}) \frac{h_{re}}{h_{oe}} = 2200 - 291 \,(6.67) = 260 \ \Omega.$$
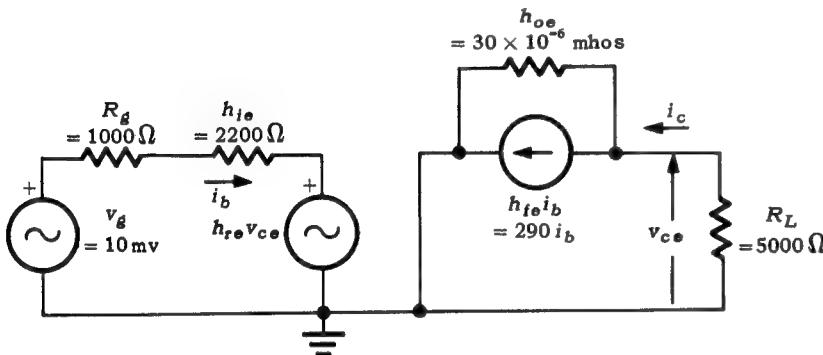
Fig. 3.14 Hybrid equivalent circuit, common-emitter connection.
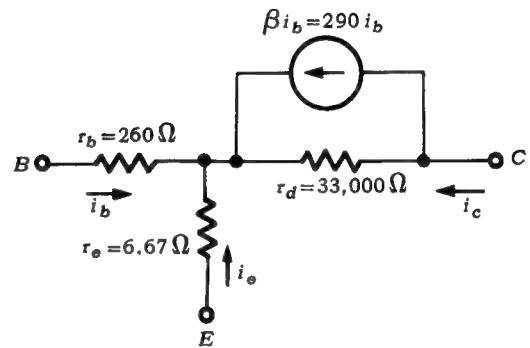
Fig. 3.15 The tee-model derived from the hybrid circuit of Fig. 3.14.

The tee-equivalent circuit is shown in Fig. 3.15. Note the substantial change in r_b in contrast to Fig. 3.12. The coupled voltage (i_e through r_e) introduces a large effective resistance value, equivalent in over-all effect to the previous 2200 Ω base resistance.

3.4 Common-Base Parameters

Since many manufacturers' data sheets list only the common-emitter characteristics, it is important to be able to determine the common-base parameters by calculation. The parameters under discussion are h_{ib}, h_{ob}, h_{fb}, and h_{rb}. The defining equations for the common-base circuit are

$$v_{be} = h_{ib} i_e + h_{rb} v_{cb}, \tag{3.20}$$

$$i_c = h_{fb} i_e + h_{ob} v_{cb}. \tag{3.21}$$

PROBLEM 3.11 Determine the common-base *h*-parameters for the 2N929 transistor at an operating point $I_C = 4$ ma, $V_{CB} = 12$ v.

Solution: Refer to (3.20) and (3.21). These expressions are most easily investigated by letting $i_e = \Delta I_E = 0$, and in turn, $v_{cb} = \Delta V_{CB} = 0$, then graphically determining the relationships among the remaining variables.

Consider Fig. 3.16a:

$$h_{ob} = \frac{\Delta I_{C_1}}{\Delta V_{CB}}\bigg|_{I_E} = \frac{\Delta I_{C_1}}{AB} \cong 0, \qquad h_{fb} = \frac{\Delta I_{C_2}}{\Delta I_E}\bigg|_{V_{CB}} = \frac{BC}{\Delta I_E} \cong \frac{2 \times 10^{-3}}{2 \times 10^{-3}} = 1.$$

It is clear that for a high-quality transistor with low leakage current and high-current gain, the collector family curves are almost useless in establishing the output circuit parameters in the common base configuration.
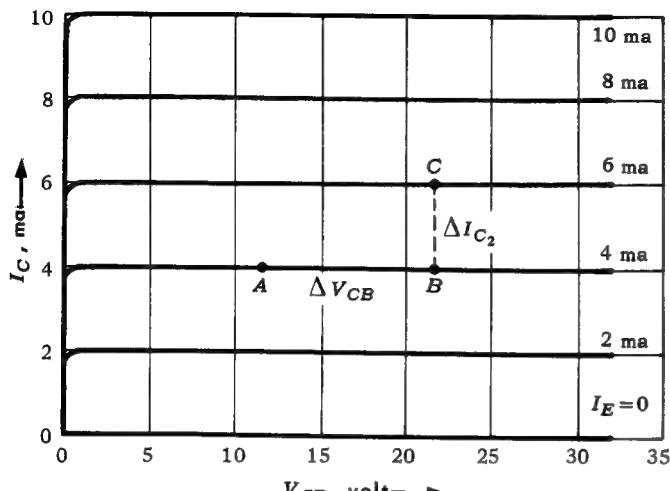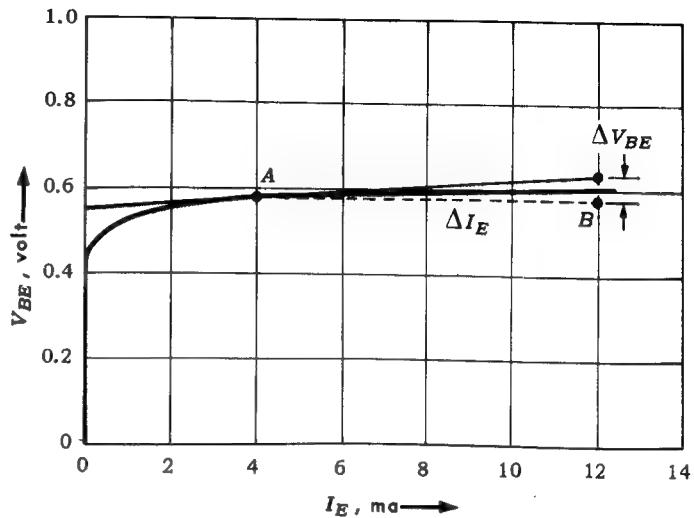
Fig. 3.16   Type 2N929 common-base characteristic curves. (a) Output characteristics and (b) input characteristics.

The input characteristics are more amenable to calculation. Referring to Fig. 3.16b,

$$h_{ib} = \frac{\Delta V_{BE}}{\Delta I_E}\bigg|_{V_{CB}} = \frac{0.06 \text{ v}}{8 \times 10^{-3} \text{ a}} = 7.5 \ \Omega.$$

Parameter $h_{rb} \cong 0$, since V_{BE} is almost independent of V_{CB}.

The h_{ib} parameter can be established with fair accuracy from the characteristic curves; the remaining hybrid parameters cannot. The parameters can still be measured by a-c techniques, as previously explained, but it is usually more convenient to compute them from the generally available common-emitter parameters.

3.5 Derivation of Common-Base Parameters

Common-base parameters may be derived from common-emitter parameters by the following procedure:

1. Redraw the common-emitter hybrid equivalent circuit, taking the transistor base as the common terminal between the emitter and collector sides.

2. For the redrawn circuit, calculate the four quantities listed in Sec. 3.3 from which the hybrid parameters are derived.

3. Equate the results obtained in Step 2 to the hybrid parameters of the common-base circuit.

PROBLEM 3.12 Using the procedure given above, calculate the common-base hybrid parameters of a transistor from known values of the common-emitter hybrid parameters.

Solution: Refer to Figs. 3.17a-b which show the hybrid common-emitter circuit, and its redrawing, in which the base B is made common to the input and output.

The four quantities to be calculated are repeated below:

1. Input impedance, measured with output short-circuited.
2. Output impedance, measured with input open.
3. Reverse voltage ratio, measured with input open.
4. Forward current gain measured with output short-circuited.

Calculate the input impedance of Fig. 3.17b with the collector short-circuited to the base, as shown in Fig. 3.18a. The circuit may be simplified by replacing the active sources, $h_{re} v_{ce}$ and $h_{fe} i_b$, by equivalent resistances. The base leg can be simplified as follows:

$$i_b = \frac{v_{be} - h_{re} v_{ce}}{h_{ie}}. \tag{3.22}$$

Because the output is short-circuited, $v_{ce} = v_{be}$, and (3.22) becomes

$$i_b = \frac{v_{be}(1 - h_{re})}{h_{ie}}.$$

Solving for the equivalent resistance of this leg,

$$\frac{v_{be}}{i_b} = \frac{h_{ie}}{1 - h_{re}}.$$

Consider the current generator, $h_{fe} i_b$. Using the value of i_b from (3.22),

$$h_{fe} i_b = \frac{v_{be} h_{fe}(1 - h_{re})}{h_{ie}}.$$

Since the voltage across the current generator is v_{be}, the current generator can be replaced by an equivalent resistor:

$$\frac{h_{ie}}{h_{fe}(1 - h_{re})}.$$

With the above simplifications, the equivalent circuit takes the form shown in Fig. 3.18b, with three resistors in parallel and the active sources eliminated. The circuit can be further simplified by the following approximations:

$$h_{re} \ll 1,$$

$$\frac{1}{h_{oe}} \gg \frac{h_{ie}}{h_{fe}(1 - h_{re})} \gg \frac{h_{ie}}{h_{fe}}.$$

With these approximations, the equivalent circuit reduces to h_{ie} in parallel with h_{ie}/h_{fe}. The common-base input impedance is therefore,

$$h_{ie} \approx \frac{\dfrac{h_{ie}}{h_{fe}}}{h_{ie} + \dfrac{h_{ie}}{h_{fe}}}.$$

This may be simplified and equated to the hybrid common-base input impedance parameter:

$$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}. \tag{3.23}$$

The forward current gain h_{fb} is determined in a similar manner. Referring again to Fig. 3.18b and using the above approximations,

$$h_{fb} = \frac{i_o}{i_i}. \tag{3.24}$$
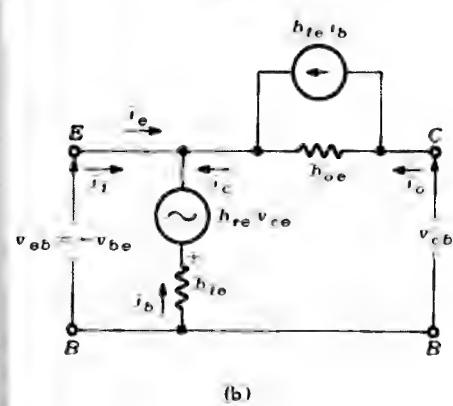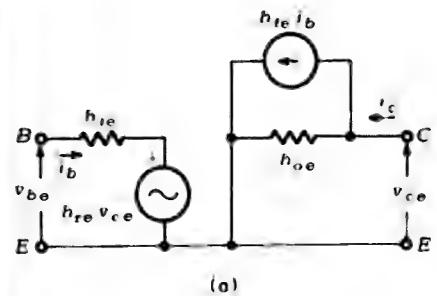
Fig. 3.17 Deriving the common-base parameters. (a) Original common-emitter circuit, and (b) redrawn so the base is now the common terminal.
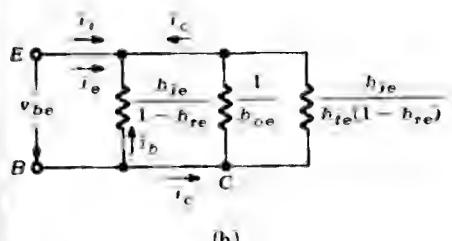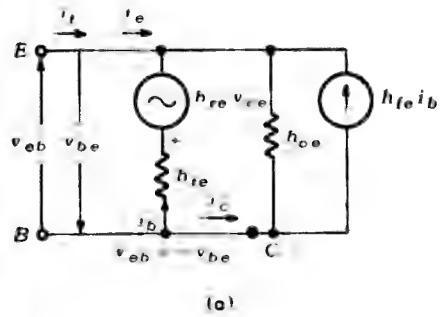
Fig. 3.18 Determining h_{ib} and h_{fb}. (a) Circuit of Fig. 3.17 (b) redrawn with C short-circuited to B. (b) Elimination of active sources.

and

$$i_c = v_{be} \frac{h_{fe}}{h_{ie}},$$

$$i_i = -v_{be} \left(\frac{h_{fe}}{h_{ie}} + \frac{1}{h_{ie}} \right) = -\frac{v_{be}}{h_{ie}} (1 + h_{fe}).$$

Substituting the last two expressions in (3.24),

$$h_{ib} = -\frac{h_{fe}}{1 + h_{fe}}. \tag{3.25}$$

Consider now the calculation of the hybrid output admittance parameter in the common-base configuration. Referring to Fig. 3.17b, let $i_e = 0$ and calculate the admittance from collector to base. By Kirchhoff's laws,

$$i_b + i_c = 0, \tag{3.26a}$$

$$v_{bc} = v_{be} + v_{ec}. \tag{3.26b}$$

$$i_c = -i_b = h_{fe} i_b - v_{ec} h_{oe}. \tag{3.26c}$$

Solving this last expression for v_{ec},

$$v_{ec} = \frac{i_b (1 + h_{fe})}{h_{oe}}. \tag{3.27}$$

Also,

$$v_{be} = i_b h_{ie} + h_{re} v_{ce} \tag{3.28a}$$

or

$$v_{be} = i_b h_{ie} - h_{re} v_{ec}. \tag{3.28b}$$

Substitute (3.27) and (3.28b) in (3.26b),

$$v_{bc} = i_b h_{ie} - \frac{h_{re}}{h_{oe}} i_b (1 + h_{fe}) + \frac{i_b (1 + h_{fe})}{h_{oe}}. \tag{3.28c}$$

Simplifying,

$$\frac{v_{bc}}{i_b} = h_{ie} + \frac{(1 + h_{fe})}{h_{oe}} (1 - h_{re}). \tag{3.29}$$

This is the output impedance. In terms of common-base parameters,

$$\frac{1}{h_{ob}} = h_{ie} + \frac{1 + h_{fe}}{h_{oe}} (1 - h_{re}).$$

Using the previous approximations,

$$h_{oe} \ll 1, \qquad h_{ie} \ll \frac{1 + h_{fe}}{h_{oe}},$$

and substituting,

$$h_{ob} = \frac{h_{oe}}{1 + h_{fe}}. \tag{3.30}$$

It remains now to determine h_{rb} in terms of the common-emitter hybrid parameters. Refer to the common-base hybrid model of Fig. 3.19. This equivalent circuit should be compared with Fig. 3.17b, where

$$v_{eb} = v_{cb} h_{rb}, \qquad v_{be} = v_{bc} h_{rb}.$$

Substituting (3.27) in (3.28b) for v_{be} and using (3.28c) for v_{bc},
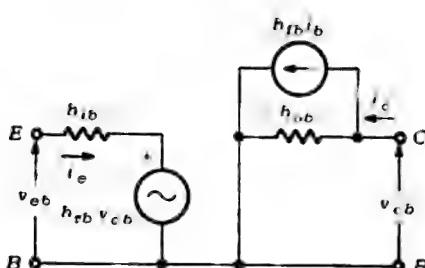
Fig. 3.19 Hybrid model for the common-base configuration.

$$h_{rb} = \frac{v_{be}}{v_{bc}} = \frac{i_b h_{ie} - h_{re} i_b \dfrac{(1 + h_{fe})}{h_{oe}}}{i_b h_{ie} - \dfrac{h_{re}}{h_{oe}} i_b (1 + h_{fe}) + i_b \dfrac{(1 + h_{fe})}{h_{oe}}} = \frac{\dfrac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}}{\dfrac{h_{ie} h_{oe}}{1 + h_{fe}} + (1 - h_{re})}. \quad (3.31)$$

Making the usual approximations,

$$h_{re} \ll 1, \qquad \frac{1 + h_{fe}}{h_{oe}} \gg h_{ie}.$$

Then h_{rb} becomes

$$h_{rb} \approx \frac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}. \quad (3.32)$$

Fig. 3.20 Common-emitter tee-equivalent circuit.

The above problem concludes the development of formulae for the conversion of common-emitter hybrid parameters to common-base hybrid parameters. The simplified conversion formulae are summarized below:

$$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}, \quad [3.23]$$

$$h_{rb} = -\frac{h_{fe}}{1 + h_{fe}}, \quad [3.25]$$

$$h_{ob} = \frac{h_{oe}}{1 + h_{fe}}, \quad [3.30]$$

$$h_{rb} = \frac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}. \quad [3.32]$$
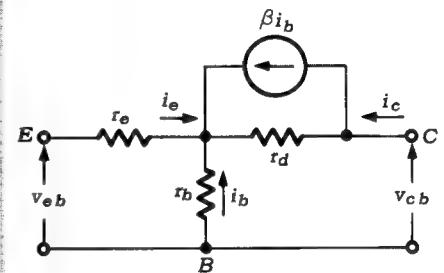
Fig. 3.21 Circuit of Fig. 3.20 redrawn so that the base is now the common terminal.

PROBLEM 3.13 Convert the parameters of the common-emitter tee-equivalent circuit to corresponding common-base parameters.

(a)

(b)
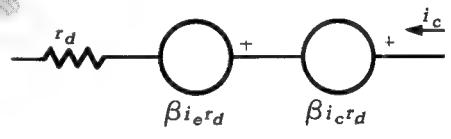
(c)
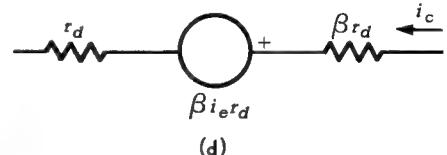
(d)
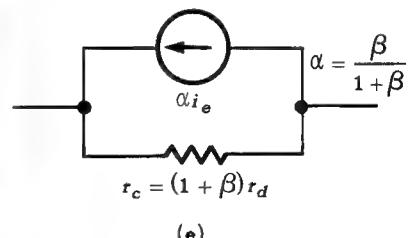
(e)

Fig. 3.22 Steps in the network conversion of Prob. 3.13. For (a) and (b): output resistance $= r_d$, open circuit voltage $= \beta i_b r_d$.

Solution: The common-emitter tee-equivalent circuit is shown in Fig. 3.20. It is redrawn in Fig. 3.21 for the common-base configuration. For a true common-base model, the network consisting of βi_b in parallel with r_d must be developed in terms of input current i_e, rather than input current i_b.

Therefore convert the current source βi_b in *parallel* with r_d shown in Fig. 3.22a to an equivalent voltage source in *series* with a resistor, as in Fig. 3.22b. The equivalency of the two networks is obvious from the figures, where they exhibit *equal open-circuit voltages* and *equal output impedances*.

The network of Fig. 3.22b must be expressed in terms of i_e instead of i_b. The following fundamental equations have been developed in Chap. 1:

$$i_b = -i_e - i_c, \qquad i_c = \beta i_b.$$

Using these relationships, Fig. 3.22b takes the modified form of Fig. 3.22c, in which two voltage generators are shown. Note that the generator $\beta i_c r_d$ has a voltage drop opposing i_c exactly equivalent to the drop across a resistor, βr_d. This suggests the modification shown in Fig. 3.22d.

The above network is converted to a current source in parallel with a resistor to obtain the common-base tee-equivalent circuit. The output impedance of the network is $r_d(1 + \beta)$. The parallel current source, multiplied by $r_d(1 + \beta)$, must equal the open-circuit voltage, $\beta i_e r_d$. Thus, the current source is $[\beta/(1 + \beta)]i_e$, or αi_e. Figure 3.22e shows this parallel configuration. The resultant common-base tee-equivalent configuration is given in Fig. 3.23.

Figures 3.24–7 summarize approximate conversion formulae between hybrid and tee-models for the common-base, common-emitter, and common-collector configurations. Those formulae not derived here may be verified using the methods of the previous problems. A table of "exact" formulae is given in Appendix B, but these are rarely used in practice.
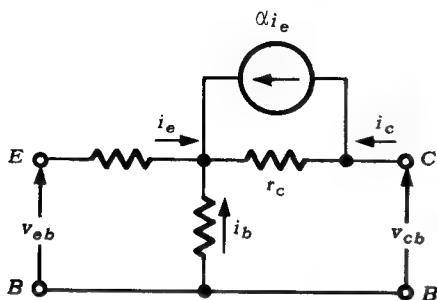
Fig. 3.23 Common-base tee-equivalent circuit.

3.6 Calculation of Amplifier Performance

A prime application of transistor models is in the calculation of small-signal amplifier performance. This includes the determination of voltage, current, and power gains, and input and output impedances.

(a) Common-emitter configuration.

(b) Hybrid equivalent circuit.

Hybrid	Common-base	Common-collector	Tee-equivalent
h_{ie}	$\dfrac{h_{ib}}{1 + h_{fb}}$	h_{ic}	$r_b + \dfrac{r_e}{1 - \alpha}$
h_{re}	$\dfrac{h_{ib} h_{ob}}{1 + h_{fb}} - h_{rb}$	$1 - h_{rc}$	$\dfrac{r_e}{(1 - \alpha) r_c}$
h_{fe}	$\dfrac{-h_{fb}}{1 + h_{fb}}$	$-(1 + h_{fc})$	$\dfrac{\alpha}{1 - \alpha}$
h_{oe}	$\dfrac{h_{ob}}{1 + h_{fb}}$	h_{oc}	$\dfrac{1}{(1 - \alpha) r_c}$

(c) Approximate parameter conversion formulae.

$$h_{ie} = 2200 \ \Omega$$
$$h_{re} = 2 \times 10^{-4}$$
$$h_{fe} = 290$$
$$h_{oe} = 30 \times 10^{-6} \ \text{mhos}$$

(d) Typical values for type 2N929 transistor at $I_C = 4$ ma, $V_{CE} = 12$ v.

Fig. 3.24 Conversion to common-emitter *h*-parameters.

(a) Common-base configuration.

(b) Hybrid equivalent circuit.

Hybrid	Common-emitter	Common-collector	Tee-equivalent
h_{ib}	$\dfrac{h_{ie}}{1+h_{fe}}$	$-\dfrac{h_{ic}}{h_{fc}}$	$r_e + (1-\alpha)r_b$
h_{rb}	$\dfrac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$	$h_{rc} - 1 - \dfrac{h_{ic}h_{oc}}{h_{fc}}$	$\dfrac{r_b}{r_c}$
h_{fb}	$-\dfrac{h_{fe}}{1+h_{fe}}$	$-\dfrac{1+h_{fc}}{h_{fc}}$	$-\alpha$
h_{ob}	$\dfrac{h_{oe}}{1+h_{fe}}$	$-\dfrac{h_{oc}}{h_{fc}}$	$\dfrac{1}{r_c}$

(c) Approximate parameter conversion formulae.

$$h_{ib} = 7.57\ \Omega$$
$$h_{rb} = 0.268 \times 10^{-4}$$
$$h_{fb} = -0.996$$
$$h_{ob} = 0.103 \times 10^{-6}\ \text{mhos}$$

(d) Typical values for type 2N929 transistor.

Fig. 3.25 Conversion to common-base h-parameters.

(a) Common-collector configuration.

(b) Hybrid equivalent circuit.

Hybrid	Common-emitter	Common-base	Tee-equivalent
h_{ic}	h_{ie}	$\dfrac{h_{ib}}{1+h_{fb}}$	$r_b + \dfrac{r_e}{1-\alpha}$
h_{rc}	$1 - h_{re} \cong 1$	$1 - h_{rb} - \dfrac{h_{ib}h_{ob}}{1+h_{fb}} \cong 1$	$1 - \dfrac{r_e}{(1-\alpha)r_c} \cong 1$
h_{fc}	$-(1+h_{fe})$	$-\dfrac{1}{1+h_{fb}}$	$\dfrac{-1}{1-\alpha}$
h_{oc}	h_{oe}	$\dfrac{h_{ob}}{1+h_{fb}}$	$\dfrac{1}{(1-\alpha)r_c}$

(c) Approximate parameter conversion formulae.

$$h_{ic} = 2200\ \Omega$$
$$h_{rc} = 0.9999 \cong 1.0$$
$$h_{fc} = -291$$
$$h_{oc} = 30 \times 10^{-6}\ \text{mhos}$$

(d) Typical values for type 2N929 transistor.

Fig. 3.26 Conversion to common-collector h-parameters.

(a) Tee-equivalent circuit, common-base.

(b) Tee-equivalent circuit, common-emitter.

(c) Approximate parameter conversion formulae.

Tee-parameter	Common-emitter	Common-base	Common-collector
α	$\dfrac{h_{fe}}{1 + h_{fe}}$	$- h_{fb}$	$\dfrac{1 + h_{fc}}{h_{fc}}$
r_c	$\dfrac{h_{fe} + 1}{h_{oe}}$	$\dfrac{1 - h_{rb}}{h_{ob}}$	$- \dfrac{h_{fc}}{h_{oc}}$
r_e	$\dfrac{h_{re}}{h_{oe}}$	$h_{ib} - (1 + h_{fb})\dfrac{h_{rb}}{h_{ob}}$	$\dfrac{1 - h_{rc}}{h_{oc}}$
r_b	$h_{ie} - \dfrac{h_{re}(1 + h_{fe})}{h_{oe}}$	$\dfrac{h_{rb}}{h_{ob}}$	$h_{ic} + \dfrac{h_{tc}(1 - h_{rc})}{h_{oc}}$
β	h_{fe}	$- \dfrac{h_{fb}}{1 + h_{fb}}$	$-(1 + h_{fc})$

(d) Typical values for type 2N929 transistor.

$$\alpha = +0.996$$
$$r_c = 9.7 \text{ M}\Omega$$
$$r_e = 6.667 \ \Omega$$
$$r_b = 260 \ \Omega$$

Fig. 3.27 Conversion to tee-parameters.

Fig. 3.28 The a-c emitter-follower amplifier for Prob. 3.14. Choke L and capacitors C_1 and C_2 isolate a-c and d-c circuits.

PROBLEM 3.14 Figure 3.28 shows a single-stage, a-c transistor amplifier. The collector characteristics for the type 2N929 transistor are given in Fig. 3.29. Determine:

(a) A-c voltage gain, for a 10 mv input signal.
(b) Input impedance.
(c) Output impedance.

Solution: (a) This is a common-collector circuit, thus requiring common-collector parameters to be used in the analysis. Let us first establish the d-c operating point at which the small-signal parameters are to be determined. Since $I_E \cong I_C$ for the very low base current of this example, a load line can be superimposed on Fig. 3.29, even though the 5000 Ω resistor is in the *emitter* circuit. The operating (Q) point is determined as

$$V_{CE} = 11.6 \text{ v}, \qquad I_C = 3.7 \text{ ma}, \qquad I_B = 15 \mu\text{a (as given)}.$$

This is close to the operating point of Fig. 3.6, in which the h-parameters were determined for the common-emitter connection. These parameters are repeated below for convenience:

$$h_{ie} = 2200 \Omega,$$
$$h_{re} = 2 \times 10^{-4},$$
$$h_{fe} = 290,$$
$$h_{oe} = 30 \times 10^{-6} \text{ mhos.}$$

The above parameters are converted to common-collector parameters using the conversion formulae of Fig. 3.26c:

$$h_{ic} = h_{ie} = 2200\,\Omega,$$
$$h_{rc} = 1,$$
$$h_{fc} = -(1 + h_{fe}) = -291,$$
$$h_{oc} = h_{oe} = 30 \times 10^{-6}\ \text{mhos}.$$

The common-collector hybrid equivalent circuit therefore takes the form of Fig. 3.30. Using this equivalent circuit,

$$v_{ec} = v_o.$$
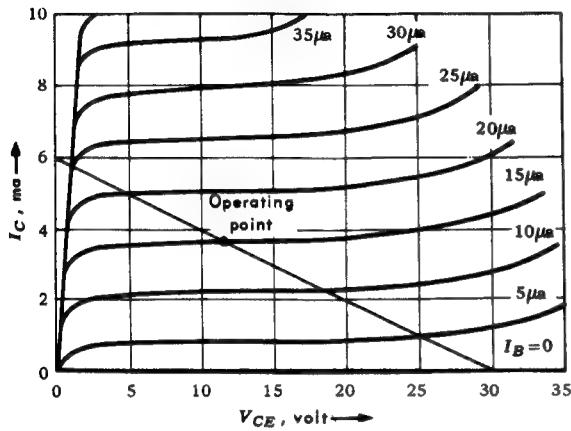
Fig. 3.29 Determining the operating point in Prob. 3.14.
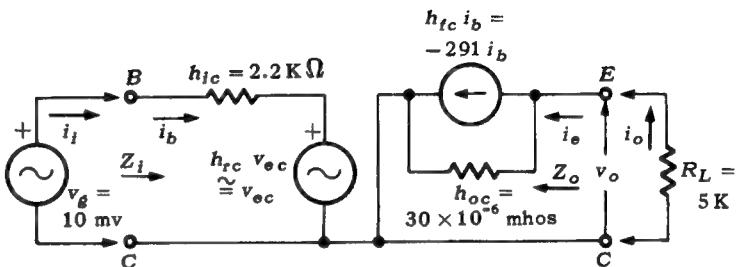
Fig. 3.30 Common-collector equivalent circuit corresponding to the amplifier of Fig. 3.28.

The basic equations are

$$i_i = i_b = \frac{v_g - h_{rc}\,v_{ec}}{h_{ic}},$$

$$i_o = i_e = \frac{\dfrac{h_{fc}\,i_b}{h_{oc}}}{R_L + \dfrac{1}{h_{oc}}} = \frac{h_{fc}\,i_b}{h_{oc}\,R_L + 1},$$

$$v_o = -i_o R_L.$$

Since $v_{ec} = v_o$, we may combine the above equations to solve for v_o in terms of i_b:

$$v_o = -\frac{h_{fc}\,R_L}{1 + h_{oc}\,R_L} \times \frac{v_g - h_{rc}\,v_o}{h_{ic}}.$$

Simplifying,

$$v_o\left(1 - \frac{h_{fc}\,R_L}{1 + h_{oc}\,R_L} \times \frac{h_{rc}}{h_{ic}}\right) = -\frac{h_{fc}\,R_L}{1 + h_{oc}\,R_L}\left(\frac{v_g}{h_{ic}}\right). \qquad (3.33)$$

Substituting numerical values,

$$1 + h_{oc}\,R_L = 1.15, \qquad \frac{h_{rc}}{h_{ic}} = \frac{1}{2200} = 4.54 \times 10^{-4}, \qquad \frac{h_{fc}}{1 + h_{oc}\,R_L} = -\frac{291}{1.15} = -253.$$

Thus,

$$v_o\left[1 - \frac{(-253)(5000)}{2200}\right] = -\frac{(-253)(5000)\,v_g}{2200}.$$

Amplifier voltage gain is now determined:

$$\frac{v_o}{v_g} = \frac{575}{1 + 575} = 1 - 0.00174 \cong 1.$$

The voltage gain is slightly less than unity.

(b) If $v_g = 10$ mv, then $v_{ec} = v_o \cong 10$ mv. Now substitute in (3.22) and calculate i_b in order to determine the input impedance Z_i:

$$i_b = \frac{v_{bc} - h_{rc} v_{ec}}{h_{ic}} = \frac{v_g - h_{rc} v_o}{h_{ic}}. \qquad [3.22]$$

Since the voltage gain is only slightly less than unity, let

$$v_o = v_g \left(1 - \frac{\Delta v_o}{v_o}\right),$$

where $\Delta v_o / v_o$ is the *per unit deviation* of output from that corresponding to exactly unity gain. Substituting this expression in (3.22),

$$i_b = \frac{v_g}{h_{ic}} - \frac{h_{rc}}{h_{ic}} \ v_g \left(1 - \frac{\Delta v_o}{v_o}\right). \qquad (3.34)$$

Let $h_{rc} = 1$, and simplify:

$$i_b = \frac{v_g}{h_{ic}} \left(\frac{\Delta v_o}{v_o}\right).$$

Calculate the input impedance, Z_i:

$$Z_i = \frac{v_g}{i_b} = \frac{h_{ic}}{\dfrac{\Delta v_o}{v_o}}.$$

Substitute numerical values:

$$h_{ic} = 2200, \qquad \frac{\Delta v_o}{v_o} = 0.00174, \qquad Z_i = \frac{2200}{0.00174} = 1.264 \times 10^6 = 1.264 \ \text{M}\Omega.$$

(c) The output impedance is obtained by inspection of Fig. 3.30 as

$$Z_o = \frac{1}{\dfrac{1}{R_L} + h_{oc}}.$$

Substituting numerical values,

$$Z_o = \frac{1}{1/5000 + 30 \times 10^{-6}} = 4350 \ \Omega.$$

The common-collector amplifier studied in the preceding problem exhibits the following characteristic features:

1. The voltage gain is very close to unity.
2. Input impedance is relatively high.
3. Output impedance is relatively low.

This circuit is called an *emitter-follower*, analogous to the vacuum tube cathode-follower.

While the calculations of Prob. 3.14 usually provide satisfactory accuracy, it is often important to know the deviation of voltage gain from unity to a high degree of precision. The approximation $h_{rc} = 1$ is not sufficiently accurate, and a more precise figure is required.

PROBLEM 3.15 For the emitter-follower of Fig. 3.28, using the "exact" value of h_{rc}, calculate the percent deviation from unity gain and the input impedance. Use the equivalent circuit of Fig. 3.30.

Solution: Rewrite (3.33) to obtain the voltage gain v_o/v_g:

$$A_v = \frac{v_o}{v_g} = \frac{\dfrac{-h_{fc} R_L}{1 + h_{oc} R_L}\left(\dfrac{1}{h_{ic}}\right)}{1 - \dfrac{h_{fc} R_L}{1 + h_{oc} R_L} \times \dfrac{h_{rc}}{h_{ic}}}. \tag{3.35}$$

Equation (3.35) may be expressed as

$$A_v = \frac{\dfrac{1}{h_{rc}}}{1 - \left[\dfrac{1 + h_{oc} R_L}{h_{fc} R_L}\left(\dfrac{h_{ic}}{h_{rc}}\right)\right]}.$$

The quantity in brackets is very much less than unity. Therefore, dividing and keeping the first two terms of the quotient,

$$A_v \cong \frac{1}{h_{rc}}\left[1 + \left(\frac{1 + h_{oc} R_L}{h_{fc} R_L}\right)\left(\frac{h_{ic}}{h_{rc}}\right)\right]. \tag{3.36}$$

For $h_{rc} \cong 1$,

$$\left(\frac{1 + h_{oc} R_L}{h_{fc} R_L}\right)\left(\frac{h_{ic}}{h_{rc}}\right) = -\frac{1}{575}, \qquad A_v = \frac{1}{h_{rc}}\left(1 - \frac{1}{575}\right).$$

This is the value that was obtained in Prob. 3.14. More accurately,

$$h_{rc} = 1 - h_{re} = 1 - 2 \times 10^{-4},$$

$$\frac{1}{h_{rc}} = \frac{1}{1 - 2 \times 10^{-4}} \cong 1 + 2 \times 10^{-4},$$

$$A_v = (1 + 2 \times 10^{-4})(1 - 17.4 \times 10^{-4}),$$

$$A_v \cong 1 - 15.4 \times 10^{-4}.$$

The deviation from unity voltage gain is 0.154%.

The input impedance may be calculated from (3.34):

$$i_b = \frac{v_g}{h_{ic}}\left[1 - h_{rc}\left(1 - \frac{\Delta v_o}{v_o}\right)\right], \tag{3.34}$$

$$Z_i = \frac{v_g}{i_b} = \frac{h_{ic}}{1 - h_{rc}\left(1 - \dfrac{\Delta v_o}{v_o}\right)}. \tag{3.37}$$

From the previous gain calculation,

$$1 - \frac{\Delta v_o}{v_o} = 1 - 15.4 \times 10^{-4},$$

$$h_{rc} = 1 - 2 \times 10^{-4},$$

$$1 - h_{rc}\left(1 - \frac{\Delta v_o}{v_o}\right) = 1 - (1 - 2 \times 10^{-4})(1 - 15.4 \times 10^{-4}) = 17.4 \times 10^{-4}.$$

Substituting in (3.37),

$$Z_i = \frac{2200}{17.4} \times 10^4 \cong 1.264 \text{ M}\Omega.$$
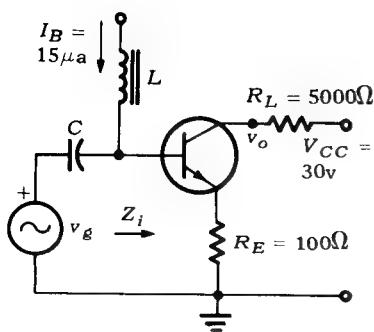
Fig. 3.31 The a-c amplifier circuit for Prob. 3.16.

The input impedance is not particularly susceptible to the error introduced by using the approximate value of h_{rc}.

PROBLEM 3.16 Calculate the input impedance Z_i and the voltage gain v_o/v_g for the circuit of Fig. 3.31.

Solution: Figure 3.31 is treated as a common-emitter circuit where R_E is a *current feedback* resistor. Since I_E and I_C are nearly equal, the effective load line resistor is $R_L + R_E$, as shown in Fig. 3.32. The Q point is approximately 3.7 ma at 11.2 v. This is close enough to the operating point of Prob. 3.4; therefore the same h_e parameters may be used:

$$h_{ie} = 2200\,\Omega,$$
$$h_{re} = 2 \times 10^{-4},$$
$$h_{fe} = 290,$$
$$h_{oe} = 30 \times 10^{-6} \text{ mhos.}$$
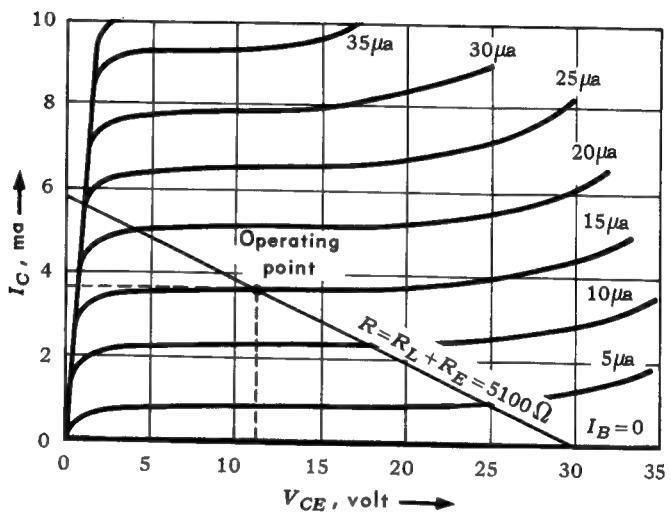
Fig. 3.32 Finding the operating point for the circuit of Fig. 3.31.
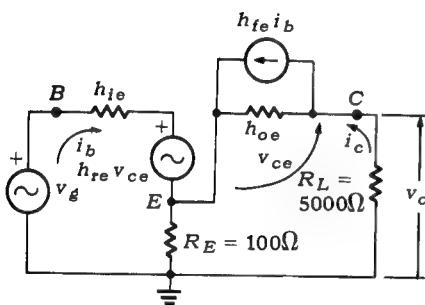
(a)
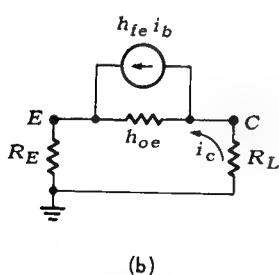
(b)

Fig. 3.33 Model for the amplifier of Fig. 3.31. (a) Exact equivalent circuit and (b) simplified output circuit.

The equivalent circuit takes the form of Fig. 3.33a. The emitter resistor acts as a coupling element between the base and collector circuits, and is best dealt with on an approximation basis. This practice is almost always legitimate in transistor circuitry where parameters are rarely known to a high degree of accuracy. The following two approximations are very helpful.

1. Let $h_{re} \cong 0$, since $v_{ce} h_{re}$ is very small for $A_v h_{re} \ll 1$. (This may be checked after the voltage gain has been approximately determined, as explained below.)

2. Let $i_e \cong i_c$, an excellent assumption for high current gain transistors.

Using the above approximations, the output equivalent circuit can be simplified as shown in Fig. 3.33b and analyzed by conventional methods:

$$i_c \cong \frac{h_{fe} i_b \left(\dfrac{1}{h_{oe}} \right)}{\dfrac{1}{h_{oe}} + R_E + R_L} = \frac{h_{fe} i_b}{1 + (R_E + R_L) h_{oe}}. \tag{3.38}$$

From Fig. 3.33a,

$$v_g = i_b h_{ie} + \frac{R_E h_{fe} i_b}{1 + (R_E + R_L) h_{oe}}.$$

Solving for $Z_i = v_{\delta}/i_b$,

$$Z_i = h_{ie} + \frac{R_E h_{fe}}{1 + h_{oe} (R_E + R_L)}. \tag{3.39}$$

Substituting numerical values,

$$Z_i = 2200 + \frac{29,000}{1 + (30 \times 10^{-6})(5100)} = 27,300 \,\Omega.$$

The output voltage v_o is

$$v_o = -R_L i_c = \frac{-R_L h_{fe} i_b}{1 + h_{oe} (R_E + R_L)}.$$

Substituting v_{δ}/Z_i for i_b,

$$v_o = \frac{-R_L h_{fe}}{1 + h_{oe} (R_E + R_L)} \times \frac{v_{\delta}}{Z_i}.$$

The voltage gain is

$$A_v = \frac{v_o}{v_{\delta}} = \frac{-R_L h_{fe}}{1 + h_{oe} (R_E + R_L)} \times \frac{1}{Z_i}. \tag{3.40}$$

Substituting for Z_i and simplifying,

$$A_v = \frac{-R_L h_{fe}}{h_{ie} + h_{ie} h_{oe} (R_E + R_L) + h_{fe} R_E}. \tag{3.41}$$

Before substituting numerical values, observe that if h_{fe} is very large, the voltage gain reduces to

$$A_v \cong \frac{-R_L}{R_E}. \tag{3.42}$$

This approximate formula is very valuable in estimating the approximate behavior of circuits having the configuration of Fig. 3.31.

The numerical results of this problem confirm the validity of (3.42). Using (3.41),

$$A_v = \frac{-5000 \times 290}{2200 + 2200(30 \times 10^{-6})(5100) + (290)(100)}$$

$$= \frac{-5000 \times 290}{2200 + 337 + 29,000} = -46.$$

This compares well with a value of -50 determined from the approximation of (3.42).

Check the validity of our assumption that $h_{re} v_{ce}$ is negligible. Assume $v_{\delta} = 10$ mv. Then $v_o = A_v v_{\delta} = 460$ mv. Thus,

$$h_{re} v_{ce} = 2 \times 10^{-4} \times -460 = -0.092 \text{ mv}.$$

This voltage aiding the input signal is less than 1% of v_{δ}, confirming the soundness of the earlier assumption.

The characteristics of the above circuit can be further clarified by solving for input impedance and voltage gain using the common-emitter tee-model. The parameters were determined earlier in Prob. 3.8:

$$r_b = 260 \,\Omega, \qquad r_e = 6.67 \,\Omega, \qquad r_c = \frac{291}{30 \times 10^{-6}} = 9.7 \text{ M}\Omega,$$

$$\beta = 290, \qquad r_d = \frac{r_c}{1 + \beta} = 33,000 \,\Omega.$$

PROBLEM 3.17   Using the above parameters, solve the tee-equivalent circuit of Fig. 3.34 for Z_i and A_v.

Solution: The tee-circuit is easily solved using conventional two-mesh analysis. Since most engineers are more adept in using voltage generators, these are substituted for the current generators of Fig. 3.34, yielding the modified circuit of Fig. 3.35.

The mesh equations are

$$v_g = (r_b + r_e + R_E)i_b + (r_e + R_E)i_c, \tag{3.43}$$

$$\frac{\beta r_c}{1 + \beta}\, i_b = (R_E + r_e)i_b + \left(r_e + R_E + \frac{r_c}{1 + \beta} + R_L\right) i_c.$$

The second of these equations may be rewritten as

$$0 = \left(R_E + r_e - \frac{\beta r_c}{1 + \beta}\right) i_b + \left(r_e + R_E + \frac{r_c}{1 + \beta} + R_L\right) i_c. \tag{3.44}$$

Using determinants, solve (3.43) and (3.44) for i_b:

$$i_b = \frac{1}{\Delta} \begin{vmatrix} v_g & r_e + R_E \\ 0 & r_e + R_E + \dfrac{r_c}{1 + \beta} + R_L \end{vmatrix}$$

$$= v_g \frac{\left(r_e + R_E + \dfrac{r_c}{1 + \beta} + R_L\right)}{\Delta},$$

where Δ is the determinant of the system equations. Solving for $Z_i = v_g/i_b$,

$$Z_i = \frac{\Delta}{r_e + R_E + \dfrac{r_c}{1 + \beta} + R_L}. \tag{3.45}$$

The determinant Δ is

$$\Delta = \begin{vmatrix} r_b + r_e + R_E & r_e + R_E \\ R_E + r_e - \dfrac{\beta r_c}{1 + \beta} & r_e + R_E + \dfrac{r_c}{1 + \beta} + R_L \end{vmatrix}$$

$$= r_b \left(r_e + R_E + \frac{r_c}{1 + \beta} + R_L\right) + (r_e + R_E)(r_c + R_L). \tag{3.46}$$

Substituting (3.46) in (3.45),

$$Z_i = r_b + \frac{(r_e + R_E)(r_c + R_L)}{(r_e + R_E) + \dfrac{r_c}{1 + \beta} + R_L}. \tag{3.47}$$

Insert numerical values:

$$Z_i = 260 + \frac{(106.67)(9.7 \times 10^6 + 5000)}{(106.67) + \dfrac{9.7 \times 10^6}{291} + 5000} = 27,100\,\Omega.$$

This checks very closely with the value of input impedance calculated for the hybrid circuit of the previous example.

Simplifying (3.47) by making the following approximations,

$$r_e + R_E \ll \frac{r_c}{1 + \beta} + R_L, \qquad r_b \ll \frac{(r_e + R_E)(r_c + R_L)}{\dfrac{r_c}{1 + \beta} + R_L},$$
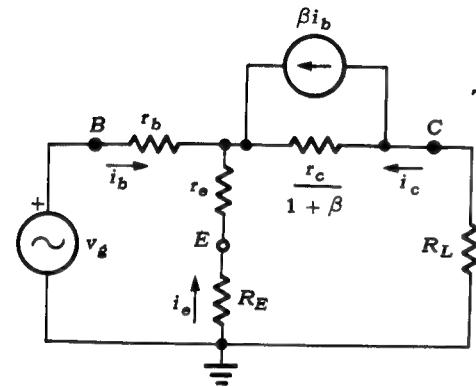
Fig. 3.34 Tee-equivalent circuit for common-emitter connection showing resistor R_E.
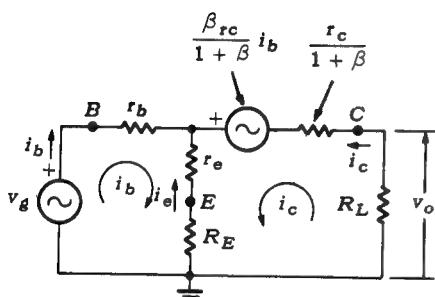
Fig. 3.35 Equivalent circuit solved by using mesh currents.

we obtain

$$Z_i \cong \frac{(r_e + R_E)(r_c + R_L)}{\dfrac{r_c}{1 + \beta} + R_L}. \tag{3.48}$$

A further level of approximation with consequent simplification is introduced by assuming that

$$\frac{r_c}{1 + \beta} \gg R_L,$$

which leads to

$$Z_i = (1 + \beta)(r_e + R_E). \tag{3.49}$$

Check this approximate Z_i with the more accurate value of $27,100\,\Omega$ by substituting numerical values:

$$Z_i = (1 + 290)(106.7) = 31,000\,\Omega.$$

This approximation is perfectly satisfactory for many purposes.

Now calculate voltage gain. Determine i_c by the use of determinants,

$$i_c = \frac{1}{\Delta} \begin{vmatrix} r_b + r_e + R_E & v_s \\ r_e + R_E - \dfrac{\beta r_c}{1 + \beta} & 0 \end{vmatrix}$$

$$= \frac{1}{\Delta} \left[-v_s \left(r_e + R_E - \frac{\beta r_c}{1 + \beta} \right) \right].$$

Since $v_o = -i_c R_L$, and $A_v = v_o/v_s$,

$$A_v = \frac{R_L}{\Delta} \left(r_e + R_E - \frac{\beta r_c}{1 + \beta} \right). \tag{3.50}$$

We now substitute the expression for the determinant:

$$\Delta = r_b \left(r_e + R_E + \frac{r_c}{1 + \beta} + R_L \right) + (r_e + R_E)(r_c + R_L). \tag{3.46}$$

Simplifying (3.50) and (3.46) by the following approximations,

$$r_c \gg r_e + R_E, \qquad \frac{r_c}{1 + \beta} \gg r_e + R_E, \qquad r_c \gg R_L,$$

the equation reduces to

$$\Delta \cong r_b \left(\frac{r_c}{1 + \beta} + R_L \right) + r_c (r_e + R_E),$$

$$A_v = \frac{-R_L \dfrac{\beta r_c}{1 + \beta}}{r_b \left(\dfrac{r_c}{1 + \beta} + R_L \right) + r_c (r_e + R_E)}. \tag{3.51}$$

Substituting numerical values,

$$A_v = \frac{-(5000) \dfrac{290}{291} \, 9.7 \times 10^6}{260 \left(\dfrac{9.7 \times 10^6}{291} + 5000 \right) + 9.7 \times 10^6 \, (106.7)}$$

$$= -46.3.$$

This confirms the previously calculated value of – 46.

The expression for gain (3.51) can be further simplified. The second term in the denominator of (3.51) is often much greater than the first term when R_E is present in the circuit. Therefore,

$$A_v \cong \frac{-R_L}{r_e + R_E} \left(\frac{\beta}{1 + \beta}\right),$$

or simply,

$$A_v \cong \frac{-R_L}{r_e + R_E}. \tag{3.52}$$

As a check, substitute numerical values from the above problem:

$$A_v = \frac{-5000}{106.7} = -47.$$

This is obviously an excellent check of the approximate expression.

The significance of the simplified gain formula $-R_L/R_E$ is readily apparent from a physical viewpoint. The base-emitter voltage is small, so that changes in base voltage must be approximately duplicated by changes in emitter voltage. The presence of an emitter resistor means that emitter (and therefore collector) *current* must follow changes in base voltage. If the collector current follows base voltage changes, then the drop across R_L must do likewise. The drop across R_L is equal to R_L/R_E times the emitter resistor drop, which approximately equals the base voltage. Hence, the voltage gain approximates $-R_L/R_E$. If R_E is substantially larger than the variations of r_e due to temperature, long term drift in the Q point and voltage gain will be relatively insensitive to these factors. Voltage gain is also relatively insensitive to changes in β. In the above circuit, if β doubles, the voltage gain will increase by about 0.2%. Although this use of R_E—an example of current feedback—reduces voltage gain, it provides a simple method of introducing negative feedback around a single stage for increased stability and input impedance.

3.7 Hybrid-π Equivalent Circuit

This equivalent circuit was originally derived by means of fundamental considerations in Chap. 1. Its value rests primarily on its use at high frequencies. However, in this chapter we will concentrate on its low-frequency characteristics, in particular, the development of conversion formulae between h- and hybrid-π parameters. Accordingly, the capacitors which represent high-frequency effects are momentarily ignored.

Figures 3.36a-b show the h- and hybrid-π models for comparison purposes. Note that the hybrid-π circuit has *five* independent low-frequency parameters; i.e., one more parameter than the other equivalent circuits we have thus far studied. One parameter may be specified in an arbitrary manner. Usually it is convenient to select $r_{bb'}$ as this arbitrary parameter, although at high frequencies the actual value can be measured. No problems arise from this arbitrary selection; however, it is preferable to choose $r_{bb'}$ so that all hybrid-π parameters are then positive.

$h_{ie} = 2200\Omega$ $h_{fe} = 290$
$h_{re} = 2 \times 10^{-4}$ $h_{oe} = 30 \times 10^{-6}$ mho

(a)

(b)

Fig. 3.36 (a) Hybrid equivalent circuit for common-emitter connection. (b) Hybrid-π equivalent circuit for common-emitter connection. Capacitive components are not shown in this low-frequency model.

PROBLEM 3.18 Given the h-parameters of Fig. 3.36a, derive conversion formulae for the hybrid-π parameters.

Solution: The basic approach is to compare the behavior of the circuits for the conditions of the output short-circuited and the input open-circuited; i.e., short-

circuiting the collector to the emitter so that $v_{ce} = 0$. Then i_c/i_b is calculated for both configurations and equated.

For the hybrid-π,

$$i_c = g_m\, v_{b'e} = i_b\, g_m \frac{r_{b'c}\, r_{b'e}}{r_{b'c} + r_{b'e}}\,. \tag{3.53}$$

For the h-parameter circuit,

$$i_c = h_{fe}\, i_b.$$

Equating,

$$g_m = \frac{h_{fe}}{r_{eq}}, \qquad r_{eq} = \frac{r_{b'c}\, r_{b'e}}{r_{b'c} + r_{b'e}}. \tag{3.54}$$

Note that $r_{eq} \equiv r_{b'e}$ since normally $r_{b'c} \gg r_{b'e}$.

In a similar manner, the short-circuit input impedance is calculated. For the hybrid-π,

$$Z_i = r_{bb'} + r_{eq},$$

and for the h-parameter circuit,

$$Z_i = h_{ie}.$$

Equating,

$$h_{ie} = r_{bb'} + r_{eq}\,.$$

If we determine $r_{bb'}$ either by measurement at high frequency or arbitrarily, we can determine r_{eq}:

$$r_{eq} = h_{ie} - r_{bb'}. \tag{3.55}$$

From (3.54), g_m is determined:

$$g_m = \frac{h_{fe}}{h_{ie} - r_{bb'}}\,. \tag{3.56}$$

A simple approximate expression for the large-signal value of g_m may be derived. From (3.53),

$$I_c = g_m\, v_{b'e}.$$

Dividing both sides by I_B,

$$\frac{I_c}{I_B} = g_m \frac{V_{b'e}}{I_B}. \tag{3.57}$$

However, based on (1.11) at room temperature (300 °K),

$$\frac{V_{b'e}}{I_B} = \frac{0.026}{I_B}.$$

Substituting in (3.57),

$$g_m = \frac{I_c}{0.026}\,.$$

For commercial silicon transistors, a somewhat more accurate expression for g_m is

$$g_m = \frac{I_c}{0.043}. \tag{3.58}$$

If no measured value of $r_{bb'}$ is available, this expression can be used to estimate g_m and $r_{bb'}$.

To continue our conversion of parameters, v_{ce}/v_{be} is determined with the input circuit open, and v_{ce} applied at the collector. For the hybrid-π,

$$v_{be} = v_{ce} \frac{r_{b'e}}{r_{b'e} + r_{b'c}} = v_{ce} \frac{r_{eq}}{r_{b'c}}. \tag{3.59}$$

For the h-parameter circuit,

$$v_{be} = h_{re} \, v_{ce}.$$

Equating these expressions,

$$\frac{r_{eq}}{r_{b'c}} = h_{re}, \qquad r_{b'c} = \frac{r_{eq}}{h_{re}} = \frac{h_{ie} - r_{bb'}}{h_{re}}. \tag{3.60}$$

For these same conditions,

$$h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}}. \tag{3.59}$$

Substituting (3.60) for $r_{b'c}$ in (3.59) to determine $r_{b'e}$,

$$r_{b'e} = \frac{h_{ie} - r_{bb'}}{1 - h_{re}}. \tag{3.61}$$

Again, for these same conditions, the base circuit open and v_{ce} applied to the collector circuit,

$$v_{b'e} = v_{ce} \frac{r_{b'e}}{r_{b'e} + r_{b'c}}. \tag{3.59}$$

All currents at node C of the hybrid-π circuit are now summed:

$$i_c = v_{ce} \left(g_m \frac{r_{b'e}}{r_{b'e} + r_{b'c}} + \frac{1}{r_{ce}} + \frac{1}{r_{b'e} + r_{b'c}} \right). \tag{3.62}$$

This may be modified by substituting the hybrid parameters already determined:

$$\frac{i_c}{v_{ce}} = \frac{h_{ie} \, h_{re}}{h_{ie} - r_{bb'}} + \frac{h_{re}(1 - h_{re})}{h_{ie} - r_{bb'}} + \frac{1}{r_{ce}}.$$

But by definition,

$$\frac{i_c}{v_{ce}} = h_{oe}.$$

so that

$$\frac{1}{r_{ce}} = h_{oe} - h_{re} \frac{1 + h_{fe} - h_{re}}{h_{ie} - r_{bb'}} \cong h_{oe}. \tag{3.63}$$

This completes the required conversion. The results are summarized in Table 3.1.

PROBLEM 3.19 Using the parameters of Fig. 3.36a, derive the corresponding hybrid-π parameters for $r_{bb'} = 0$.

Solution: The required parameters are found by direct substitution. Referring to Table 3.1,

$$g_m = \frac{290}{2200} = 0.132 \text{ mho}, \tag{3.56}$$

$$r_{b'c} = \frac{2200}{2 \times 10^{-4}} = 11 \times 10^{6} \ \Omega, \tag{3.60}$$

$$r_{b'e} = 2200 \ \Omega, \tag{3.61}$$

TABLE 3.1 Conversion from hybrid to hybrid-π parameters.

$$g_m = \frac{h_{fe}}{h_{ie} - r_{bb'}} \tag{3.56}$$

$$r_{b'c} = \frac{h_{ie} - r_{bb'}}{h_{re}} \tag{3.60}$$

$$r_{b'e} = \frac{h_{ie} - r_{bb'}}{1 - h_{re}} \cong h_{ie} - r_{bb'} \tag{3.61}$$

$$\frac{1}{r_{ce}} = h_{oe} - h_{re} \frac{1 + h_{fe} - h_{re}}{h_{ie} - r_{bb'}} \cong h_{oe} \tag{3.63}$$

$$\frac{1}{r_{ce}} = 30 \times 10^{-6} - 2 \times 10^{-4} \left(\frac{291}{2200}\right) = 3.4 \times 10^{-6} \text{ mhos}, \qquad [3.63]$$

so that $r_{ce} = 286,000 \ \Omega$.

PROBLEM 3.20 Repeat the previous problem using $r_{bb'} = 255 \ \Omega$.

Solution: Proceed as before:

$$g_m = \frac{290}{1945} = 0.149 \text{ mho}, \qquad [3.56]$$

$$r_{b'c} = \frac{1945}{2 \times 10^{-4}} = 9.73 \times 10^6 \ \Omega, \qquad [3.60]$$

$$r_{b'e} = 1945 \ \Omega, \qquad [3.61]$$

$$\frac{1}{r_{ce}} = 30 \times 10^{-6} - 2 \times 10^{-4} \frac{291}{1945} \cong 0 \text{ mho}, \qquad [3.63]$$

so that $r_{ce} = \infty$.

For $r_{bb'} > 255 \ \Omega$, r_{ce} would be negative, making it inconvenient for calculations.

PROBLEM 3.21 Figure 3.37 shows the hybrid-π amplifier model. Using the hybrid-π values found in Prob. 3.20, calculate load power, and current and voltage gains.
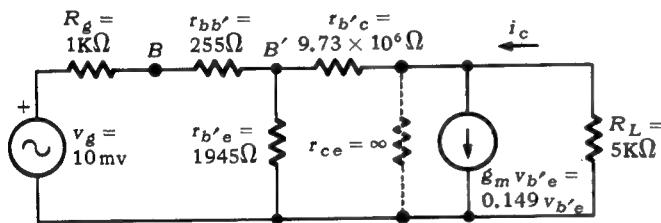
Fig. 3.37 Hybrid-π amplifier circuit for Prob. 3.20.

$V_L = 0.149 \, v_{b'e} R_L = 745 \, v_{b'e}$
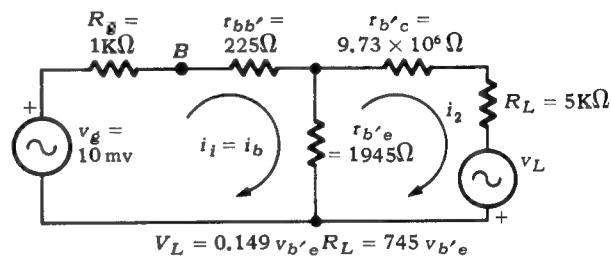
Fig. 3.38 Hybrid-π amplifier circuit of Fig. 3.37, with current source replaced by voltage source for easier calculation.

Solution: Start by replacing the current source and R_L of Fig. 3.37 with the equivalent voltage source shown in Fig. 3.38. The basic equations are

$$v_g = (R_g + r_{bb'} + r_{b'e}) \, i_1 - r_{b'e} \, i_2,$$

$$v_L = - r_{b'e} \, i_1 + (r_{b'e} + r_{b'c} + R_L) \, i_2.$$

Substituting numerical values and solving by determinants,

$$i_1 = 3.38 \ \mu \text{ a},$$

$$i_2 = 0.44 \ \mu \text{ a}.$$

Since $v_{b'e} = r_{b'e} \, (i_1 - i_2)$,

$$v_L = 745 \, r_{b'e} \, (i_1 - i_2) = 4.12 \text{ v},$$

and continuing,

$$- v_{ce} = v_L + i_2 \, R_L = 4.12 + 0.44 \times 10^{-6} \times 5 \times 10^3 \cong 4.12 \text{ v},$$

$$i_c = - \frac{v_{ce}}{R_L} = \frac{4.12}{5000} = 0.824 \text{ ma},$$

$$P_L \cong i_c \, v_{ce} = 3.12 \text{ mw}.$$

Thus,

$$A_I = \frac{i_1}{i_2} = \frac{824 \times 10^{-6}}{3.38 \times 10^{-6}} = 244,$$

$$A_v = \frac{-v_{ce}}{v_{be}} = \frac{-v_{ce}}{v_{b'e} + r_{b'b}\, i_b} = -625.$$

3.8 Supplementary Problems

PROBLEM 3.22 Give the generalized definitions of static and incremental h-parameters.

PROBLEM 3.23 Define mathematically the static and incremental h-parameters for the common-base connection.

PROBLEM 3.24 For the characteristics shown in Fig. 3.5, find the h-parameters for a 2N929 transistor when the CE connection is at $V_{CE} = 10$ v and $I_C = 2$ ma.

PROBLEM 3.25 Determine r_e, r_b, and r_d for the h-parameters of Prob. 3.24.

PROBLEM 3.26 In the circuit of Fig. 3.7, let $R_L = 10\,K\Omega$, $R_B = \infty$, $R_g = 2\,K\Omega$, $C_B = \infty$, and $I_B = 20\,\mu a$. Determine (a) the operating point, (b) the incremental h-parameters at the operating point, and (c) r_e, r_b, and r_d. Draw this circuit, replacing the transistor by its tee-equivalent network, and determine the input and voltage gain using standard circuit analysis and assuming r_d infinite as an approximation.

PROBLEM 3.27 How are r_e and r_d measured?

PROBLEM 3.28 Design a simple β measuring circuit.

PROBLEM 3.29 In the circuit of Fig. 3.28, if $I_B = 5\,\mu a$, find (a) the maximum rms output voltage without distortion, (b) the v_g that generates the maximum voltage, and (c) the approximate input impedance.

PROBLEM 3.30 If $R_L = 10^6\,\Omega$ in Fig. 3.31, the approximate formula (3.42) is no longer valid. Why?

PROBLEM 3.31 If $h_{ie} = 5000\,\Omega$, $h_{fe} = 300\,\Omega$, $h_{re} = 10^{-4}\,\Omega$, and $h_{oe} = 10^{-6}\,\Omega$ for a transistor, find (a) the tee-equivalent circuit parameters and (b) the input and output impedances.

PROBLEM 3.32 For Fig. 3.2b, define the small signal h-parameter in physical terms for the common-emitter circuit.

BIAS CIRCUITS
AND STABILITY

4.1 Introduction

The key to correct transistor operation is the establishment of a *quiescent operating (Q) point*. This corresponds to the steady current condition that occurs in the absence of an input signal. Setting up a bias point for transistors is more difficult than for vacuum-tube circuits because of transistor *leakage currents*, which are extremely sensitive to temperature. A transistor which is correctly biased at room temperature may be incorrectly biased at high temperature.

This *drift* in operating point is far more characteristic of high-leakage germanium transistors than low-leakage silicon ones. However, leakage currents are important even for silicon transistors. Therefore, this chapter not only considers how to set the correct bias point but also how to compare circuit configurations for sensitivity to leakage changes. It will be found that some configurations are far more stable than others with changing temperature.

4.2 Leakage Current

Diode leakage has been described in Chap. 1. The reverse-biased collector-base junction of a transistor (emitter open) exhibits similar leakage characteristics. Transistor *collector-base leakage* I_{CBO} varies with temperature typically as shown in Fig. 4.1. Since leakage currents in silicon transistors are far lower than in germanium devices, Fig. 4.1 tells only part of the story.

PROBLEM 4.1 A germanium transistor has a leakage current of 5 μa at room temperature (25°C). If Fig. 4.1 applies, find the leakage at 75°C.

Solution: The room temperature value is 5 μa. At 75°C, this is multiplied by a factor of 30, for a leakage current of 150 μa.

PROBLEM 4.2 A 2N929 silicon transistor has a maximum 25°C leakage current of 0.01 μa. Find the maximum leakage from Fig. 4.1 at 125°C.

Solution: From Fig. 4.1, the leakage is multiplied by a factor of 45, for a leakage of 0.45 μa.

Because germanium transistors have much greater leakage currents than silicon ones, a germanium 2N1308 n-p-n type has been selected for examples in this chapter. Figures 4.2–3 show its common-emitter characteristic curves, which will provide the necessary data for subsequent calculations. Although this transistor
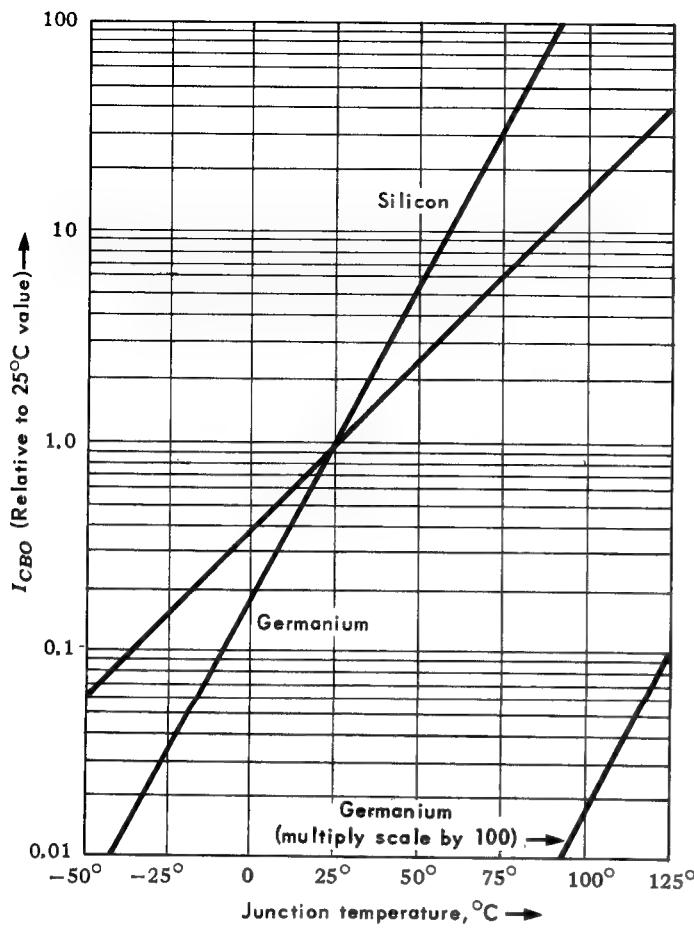
Fig. 4.1 Variation of I_{CBO} with temperature relative to 25°C.
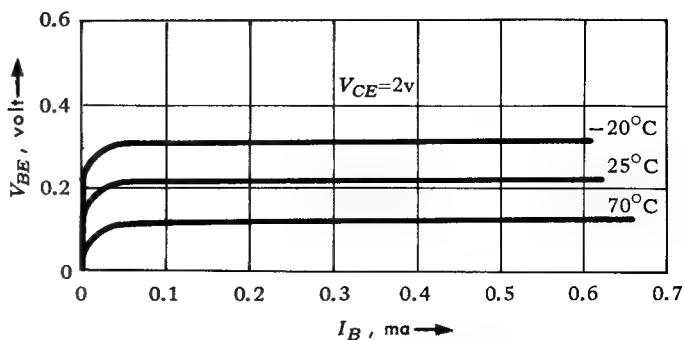
Fig. 4.2 Input characteristics of 2N1308 *n-p-n* germanium transistor vs. junction temperature for the common-emitter connection.

Fig. 4.3 Collector characteristics of 2N1308 *n-p-n* germanium transistor vs. junction temperature for the common-emitter connection.

has a 5 μa maximum leakage at room temperature, 1 μa is more typical and is *assumed* here.

4.3 Tee-Equivalent Circuit Representation of Leakage*

The *tee-equivalent* circuit, discussed in Chaps. 1 and 3, is particularly convenient for studying the effects of leakage in transistor circuits. Figure 4.4 gives the equivalent circuit for d-c or *bias* conditions. If the emitter circuit is open, $I_E = 0$, and the output current from collector to base is I_{CBO} (sometimes abbreviated to I_{CO}). This circuit, in effect, provides a definition of collector-base leakage.

A modified tee-equivalent circuit for the common-emitter connection is provided in Fig. 4.5. Here, the leakage component is between *collector* and *emitter*. The value of leakage current, I_{CEO}, in terms of I_{CBO}, may be determined from simple transistor equations.

Fig. 4.4 Common-base tee-equivalent circuit. The directions of current flow correspond to an *n-p-n* transistor.

* As we are analyzing only d-c signals in this chapter, β and α correspond to *static characteristics*. Currents and voltages are shown with their normal polarities.

PROBLEM 4.3 Derive a formula for I_{CEO} in terms of current gain β and I_{CBO}.

Solution: The basic transistor current equations are

$$I_E + I_B + I_C = 0,$$

$$I_C = I_{CBO} + \alpha I_E.$$

We combine the two expressions to eliminate I_E and then solve for I_C:

$$I_C = \frac{I_{CBO} - \alpha I_B}{1 + \alpha}. \tag{4.1}$$

Now we substitute the common-emitter current gain β as a new variable to replace α in (4.1), where $\beta = \alpha/(1 - \alpha)$. Therefore,

$$I_C = I_{CBO}(\beta + 1) + I_B \beta. \tag{4.2}$$

Since the second term in (4.2) is the normal transistor output current, the first term must be the required leakage component, I_{CEO}. Therefore,

$$I_{CEO} = I_{CBO}(1 + \beta). \tag{4.3}$$

The current gain factor β leads to a relatively high leakage current in the common-emitter circuit.

Fig. 4.5 Tee-equivalent circuit in the common-emitter connection.

Since the leakage current occurs with the base open, the leakage is *identical* in the common-collector circuit. The multiplied leakage currents in the common-emitter and common-collector connections, and their high temperature sensitivity, lead to *bias point instability*. The drift in bias point due to temperature or interchanging transistors of the same type is the central problem of biasing. The essential requirement is that I_C be *maintained constant over all operating conditions*, because this fixes the quiescent point on the load line.

Figure 4.6 provides additional clarification on the effect of leakage. The figure shows I_C vs. I_B in the common-emitter connection. Note that at $I_B = 0$, the collector current must equal I_{CEO}. Furthermore, when base current becomes *negative* and *equal* to the collector current, emitter current must be zero, so that the coordinates of point P are as shown.

Fig. 4.6 Leakage in a common-emitter circuit.

PROBLEM 4.4 For the circuit of Fig. 4.7, determine R_B at 25°C, such that $I_C = 19$ ma at the operating point.

Solution: Refer to Figs. 4.2 and 4.8a. On the latter, draw a load line corresponding to $R_L = 100$. The I_C intercept is 5 v/100 Ω = 50 ma. Thus, $I_C = 19$ ma at $I_B = 0.1$ ma (point P_1).

From Fig. 4.2, for $I_B = 0.1$ ma, $V_{BE} = 0.22$ v. The voltage across R_B is therefore $5 - 0.22 = 4.78$ v. For this voltage, and a base current of 0.1 ma,

$$R_B = \frac{4.78}{0.1} \times 10^3 = 47,800 \ \Omega.$$

Fig. 4.7 Common-emitter amplifier with bias set by adjusting R_B.

PROBLEM 4.5 For the conditions of Prob. 4.4, find I_C at 70°C.

Solution: From Fig. 4.2, V_{BE} has decreased to 0.12 v. Now I_B is

$$\frac{4.88 \text{ v}}{47,800 \ \Omega} = 0.102 \text{ ma}.$$

In Fig. 4.8a, the operating point has moved from P_1 ($I_C = 19$ ma) to P_2, where $I_C = 23$ ma. This is a considerable change.
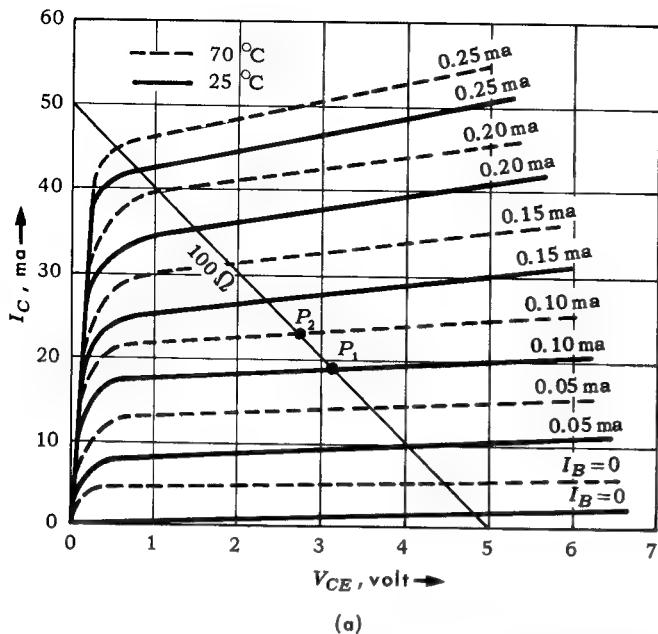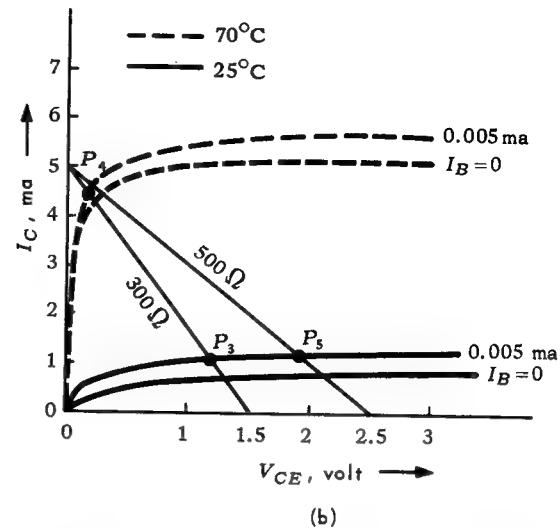
Fig. 4.8 (a) Collector characteristics of common-emitter connection with superimposed load line. (b) Expanded region showing load lines.

PROBLEM 4.6 Referring to Fig. 4.9, determine R_B so that $V_{CE} = 1.25$ v at 25°C. With this same R_B, find V_{CE} at 70°C.

Solution: Draw a new load line on Fig. 4.8b. At point P_3, $V_{CE} = 1.25$ v and $I_B = 0.005$ ma. From Fig. 4.2, $V_{BE} = 0.22$ v. The drop across R_B is $1.5 - 0.22 = 1.28$ v. With a base current of 0.005 ma,

$$R_B = \frac{1.28}{5 \times 10^{-6}} = 256,000 \; \Omega .$$

At 70°C, V_{BE} decreases to 0.12 v (approximately -2.2 mv change per degree C). Base current, at 70°C can be calculated:

$$I_B = \frac{1.5 - 0.12}{256,000} = \frac{1.38}{256} \times 10^{-3} \cong 0.0054 \text{ ma.}$$

This results in an operating point (P_4) of $V_{CE} \cong 0.2$ v. At such low voltage, the transistor is almost inoperative, showing the possible critical effects of leakage change with temperature.

PROBLEM 4.7 In Prob. 4.6, find the quiescent collector current I_C at 25°C and at 70°C.

Solution: From Fig. 4.8b, $I_C = 1$ ma at 25°C (P_3) and 4.5 ma at 70°C (P_4). This is an enormous percentage change and is due to the fact that at low operating levels, I_C contains a particularly high leakage component.
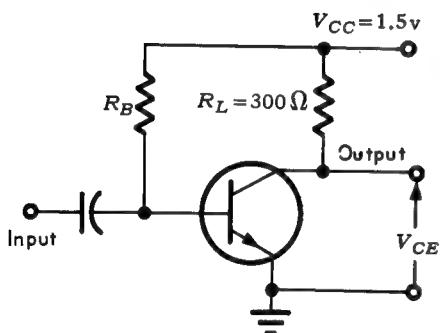
Fig. 4.9 Resistor R_B is adjusted for $V_{CE} = 1.25$ v at 25°C.

4.4 Constant Base Voltage Biasing Techniques

The following problems illustrate the stability of the transistor operating point (collector current) with the base *voltage* held reasonably constant with temperature, in contrast to constant base *current* conditions.

Fig. 4.10 Voltage divider for adjusting base bias voltage.

PROBLEM 4.8 Referring to Fig. 4.10, determine R_B so that $V_{CE} = 2$ v at 25°C. Find I_B and I_C. Calculate I_B at 70°C.

Solution: Draw a load line on Fig. 4.8b. The operating point for $V_{CE} = 2$ v is shown at P_s. At this point, $I_C = 1.25$ ma and $I_B = 5$ μa.

To determine R_B, use Thevenin's theorem which states (with reference to this problem) that the source resistance R_{eq} driving the transistor base equals the parallel resistance of R_B and 1 KΩ, and that the equivalent source potential V_{eq} equals the open base circuit voltage at the junction of the two resistors. Figure 4.11 shows how the circuit is simplified for analysis by the application of Thevenin's theorem. The base-to-emitter drop is represented by a battery of 0.22 v at room temperature (see Fig. 4.2).

Resistance R_B is now calculated:

$$\frac{V_{eq}}{R_{eq}} = \frac{2.5 \dfrac{R_B}{1000 + R_B} - 0.22}{\dfrac{1000 \times R_B}{1000 + R_B}}$$

$$= 5 \times 10^{-6}.$$

Solving,

$$R_B = 97 \ \Omega.$$

At 70°C, V_{BE} is reduced to 0.12 v, and the base current becomes

$$\frac{\left(2.5 \times \dfrac{97}{1097}\right) - 0.12}{\dfrac{1000 \times 97}{1097}} = 1.13 \text{ ma.}$$

This is over two hundred times the base current at room temperature. Obviously we may conclude that constant voltage base-emitter bias is impractical.

The previous considerations may be examined from a somewhat simpler viewpoint. The change in base-emitter voltage is 0.1 v. The effective resistance is $97 \times 1000/1097 = 88.5$ Ω. The *change* in current is $0.1/88.5 = 1.13$ ma.

The result might have been expected. Figure 4.2 shows that small changes in base-emitter voltage can lead to very large current changes when the effective external resistance in the base circuit is small. A large base resistance is necessary to achieve relative insensitivity to changes in V_{BE}.

Fig. 4.11 Simplification of the circuit of Fig. 4.10 using Thevenin's theorem.

PROBLEM 4.9 For the circuit of Fig. 4.12 and the transistor characteristics of Fig. 4.13:

(a) Determine I_B and I_C for $V_{CE} = 2$ v at 25°C.
(b) Using the above value of I_B, find V_{CE} and I_C at 70°C.
(c) Determine a new I'_B at 70°C, so that I_C is restored to its 25°C value.
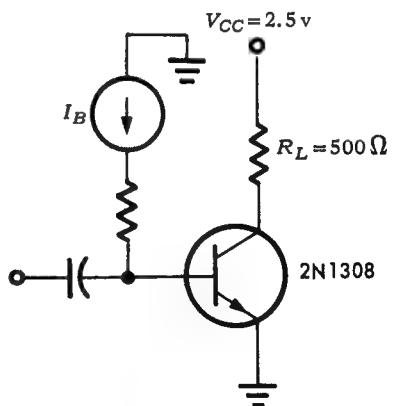
Fig. 4.12 Transistor in common-emitter circuit with constant base current drive.

Solution: From Fig. 4.13:

(a) Point P_1 at $I_B = 0.005$ ma; $I_C = 1$ ma at 25°C.

(b) At 70°C, for $I_B = 0.005$ ma, $I_C = 4.7$ ma and $V_{CE} \cong 0.2$ v at point P_2.

(c) Since $I_B' = -0.025$ ma gives $V_{CE} = 2$ v, $I_C = 1$ ma at point P_1 at 70°C.
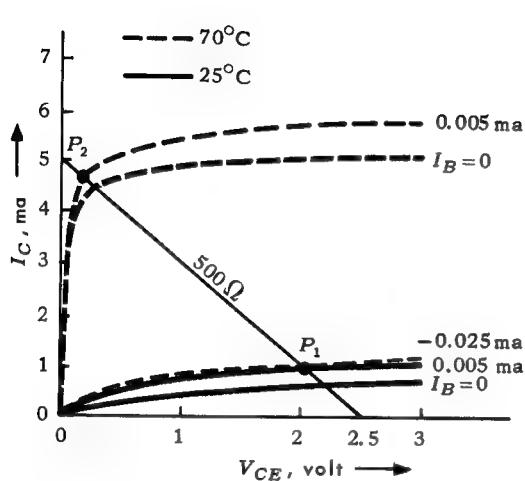
Fig. 4.13 Low level transistor characteristics of common-emitter connection with superimposed load line.
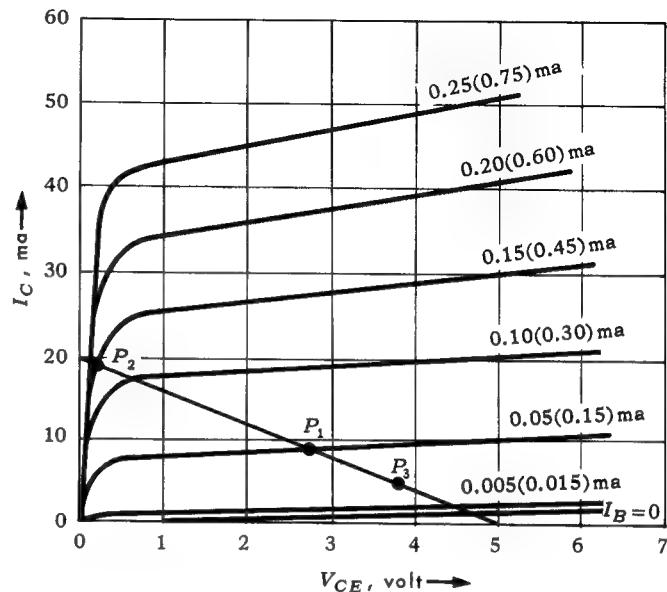
Fig. 4.14 Common-emitter collector characteristics of the 2N1308 transistor at 25°C. The two values of base current for each curve correspond to two different transistors of the same type.

Aside from the effects of temperature on transistor stability due to changes in V_{BE} and I_{CBO}, there is a considerable *spread in characteristics* among transistors of the *same type. Replacing* a transistor in a given circuit can lead to a *major shift* in operating point.

Figure 4.14 displays a family of collector characteristics for a 2N1308 germanium transistor. The values of I_B in parentheses correspond to a low current gain unit. The unbracketed base currents refer to a medium β transistor. The three-to-one variation in β is not uncommon; similar variations occur over military temperature ranges such as $-55°$ to $+85°$C.
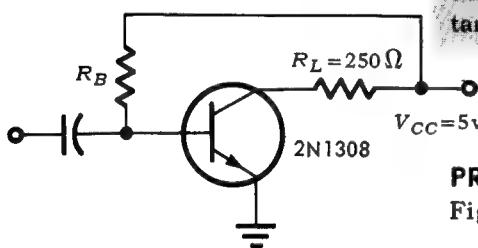
Fig. 4.15 Common-emitter circuit with approximately constant base current drive for Prob. 4.10.

PROBLEM 4.10 The transistor used in Fig. 4.15 has the characteristics of Fig. 4.14. Calculate the following:

(a) R_B, such that $I_C = 9$ ma with the low β transistor. Also determine V_{CE}.

(b) With R_B fixed, change to the higher β unit. Obtain a new operating point, and discuss its usability.

(c) Readjust R_B to achieve $I_C = 9$ ma for the high β transistor. Discuss the usability of the new operating point.

Solution: (a) Referring to Fig. 4.14, at $I_C = 9$ ma (point P_1), $I_B = 0.15$ ma and $V_{CE} = 2.7$ v. The operating point is centrally located in the usable area of the characteristics. Since the base-emitter drop is 0.22 v (see Fig. 4.2), the drop across R_B is 5 v $-$ 0.22 v $=$ 4.78 v:

$$R_B = \frac{4.78}{0.15 \times 10^{-3}} = 31,800 \ \Omega.$$

(b) The base current is essentially unchanged with the high β transistor, because I_B is almost entirely determined by the values of R_B and V_{CC}. Assuming $I_B = 0.15$ ma on the same load line as before, the new operating point is located at P_2, where $I_C = 19$ ma and $V_{CE} \cong 0.2$ v. This point is not in the useful operating region of the transistor (the transistor is in *saturation*).

(c) To restore $I_C = 9$ ma using the high β transistor, reduce I_B to 0.05 ma, thus returning to the original operating point in the center of the linear region. A new R_B is now required:

$$R_B = \frac{5 - 0.22}{0.05 \times 10^{-3}} = 95,600 \ \Omega.$$

If we now use the low β transistor with the new R_B, the operating point moves to near *cut-off*, point P_3.

The foregoing example illustrates the difficulty in maintaining a stable operating point as transistor parameters vary. *For stable operation, it is important to hold I_C reasonably constant as V_{BE}, I_{CBO}, and β vary with temperature, aging, and from transistor to transistor.* The next section develops a quantitative approach to stability, so that different circuits may readily be compared.

4.5 Stability Factors

For the purpose of comparing the relative stabilities of different transistor circuits, a *stability factor* S is defined as

$$S = \frac{\partial I_C}{\partial I_{CBO}}, \tag{4.4}$$

where S is a measure of the sensitivity of the collector current I_C to changes in leakage current I_{CBO}, and varies with the circuit configuration, such that the lower the value of S, the more stable the circuit. This stability factor can be calculated using convenient formulae applicable to the specific circuit configurations.

The permissible value of S depends on both the transistor material and the requirements of the application. Generally speaking, low-leakage silicon transistor circuits tolerate a much higher S than relatively high-leakage germanium transistor circuits. For silicon, leakage current may typically be $0.01 \ \mu a$, while a comparable germanium transistor may have an I_{OBO} of $5 \ \mu a$. For an S of 25 and similar bias circuitry, I_C changes by $0.25 \ \mu a$ in the silicon circuit, and by $125 \ \mu a$ in the germanium one.

The following discussion investigates common bias circuits, establishes design procedures, and evaluates stability. The common-base circuit is not considered because a constant bias current I_E leads to a practically constant I_C. This follows since $I_C \cong I_E$. The common-emitter circuits considered will lead to results directly applicable to the common-collector circuits, by setting the collector circuit resistance R_L equal to zero.

Figure 4.16a shows the general form of the most commonly-used bias circuit. A single battery source and current feedback (R_E) characterize the circuit. A simplified equivalent circuit ($r_D = \infty$, $r_E = 0$) is shown in Fig. 4.16b.

If R_1 in parallel with R_2 constitutes a very low equivalent resistance R_{eq} in the base circuit, the base voltage V_B is essentially constant. The drop across R_E is significantly higher than V_{BE}. The emitter current adjusts to satisfy the relationship:

$$I_E = \frac{V_B - V_{BE}}{R_E} \cong \frac{V_B}{R_E},$$

if $V_B \gg V_{BE}$, which is a valid approximation. Since $I_C \cong I_E$, the collector current remains about as constant as the voltage at the base, notwithstanding changes in V_{BE}, I_{CBO}, and β.

The behavior of the circuit depends on a low value of the combination of R_1 in parallel with R_2. The current in these resistors should be substantially more than the base current. However, the resistances must be high compared to the reactance of the blocking capacitor at the minimum a-c input signal frequency.

Note that in practical a-c amplifiers, R_E is by-passed to avoid gain reduction due to a-c negative feedback. The negative feedback is, of course, the basis for *d-c stabilization*, on which the capacitor has no effect.

PROBLEM 4.11 Derive formulae for I_C and the stability factor S in terms of circuit parameters for the common-emitter amplifier of Fig. 4.16a.
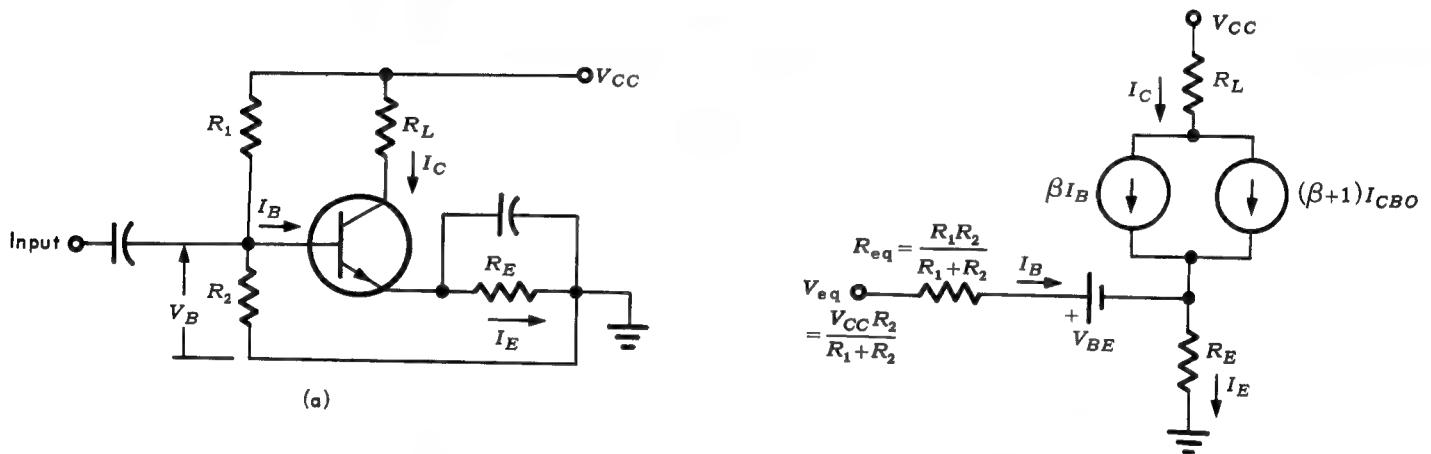
Fig. 4.16 (a) General bias circuit for common-emitter connection.
(b) Simplified equivalent circuit.

Solution: The collector current is

$$I_C = \beta I_B + (\beta + 1) I_{CBO}. \qquad [4.2]$$

From Fig. 4.16b,

$$V_{CC} \frac{R_2}{R_1 + R_2} - V_{BE} = \frac{R_1 R_2}{R_1 + R_2} I_B + R_E I_E. \qquad (4.5)$$

Also

$$I_E = I_C + I_B.$$

The above equations may be combined, eliminating I_B and I_E, and solved for I_C in terms of the parameters of the circuit. The basic bias equation becomes

$$I_C = \frac{\left(\dfrac{V_{CC} R_2}{R_1 + R_2} - V_{BE}\right)\left(\dfrac{\beta}{1 + \beta}\right) + I_{CBO}\left(R_E + \dfrac{R_1 R_2}{R_1 + R_2}\right)}{R_E + \left(\dfrac{1}{1 + \beta}\right)\dfrac{R_1 R_2}{R_1 + R_2}}. \qquad (4.6)$$

Equation (4.6) is a fundamental one, readily modified and adapted to the solution of a variety of problems. Now differentiating (4.6) with respect to I_{CBO} yields

$$S = \frac{\partial I_C}{\partial I_{CBO}} = \frac{R_E + \left(\frac{R_1 R_2}{R_1 + R_2}\right)}{R_E + \left(\frac{1}{1 + \beta}\right)\frac{R_1 R_2}{R_1 + R_2}}. \tag{4.7}$$

Since $1/(1 + \beta)$ is very small, minimum S occurs when $R_E \gg R_1 R_2/(R_1 + R_2)$. As this condition is approached, S approaches unity.

It is appropriate at this point to introduce the additional stability factors

$$M = \frac{\partial I_C}{\partial V_{BE}} \quad \text{and} \quad N = \frac{\partial I_C}{\partial \beta}, \tag{4.8}$$

which are measures of the sensitivity of collector current to changes in V_{BE} and β, respectively. Applying these definitions to (4.6),

$$M = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\dfrac{\beta}{1 + \beta}}{R_E + \left(\dfrac{1}{1 + \beta}\right)\dfrac{R_1 R_2}{R_1 + R_2}} = \frac{-\beta}{R_E(1 + \beta) + \dfrac{R_1 R_2}{R_1 + R_2}}. \tag{4.9}$$

Solving for $N = \partial I_C/\partial \beta$ is tedious but *absolutely* direct. The mathematics can be simplified by differentiating with respect to α:

$$\frac{\partial I_C}{\partial \beta} = \frac{\partial I_C}{\partial \alpha}\frac{d\alpha}{d\beta}.$$

remembering that $\beta = \alpha/(1 - \alpha)$ and $1/(1 + \beta) = 1 - \alpha$. Let $R_1 R_2/(R_1 + R_2) = R_{eq}$, an *equivalent* base circuit resistance, and $k = R_2/(R_1 + R_2)$, an *attenuation factor*. Substituting in (4.6),

$$I_C = \frac{(k V_{CC} - V_{BE})\alpha + I_{CBO}(R_B + R_{eq})}{R_B + (1 - \alpha) R_{eq}}. \tag{4.10}$$

Differentiate with respect to α:

$$\frac{\partial I_C}{\partial \alpha} = \frac{[R_B + (1 - \alpha)R_{eq}](k V_{CC} - V_{BE}) - [(k V_{CC} - V_{BE})\alpha + I_{CBO}(R_B + R_{eq})](- R_{eq})}{[R_B + (1 - \alpha)R_{eq}]^2}.$$

Simplifying,

$$\frac{\partial I_C}{\partial \alpha} = \frac{(k V_{CC} - V_{BE})(R_B + R_{eq}) - \alpha R_{eq}(k V_{CC} - V_{BE}) + (k V_{CC} - V_{BE})\alpha R_{eq} + I_{CBO} R_{eq}(R_B + R_{eq})}{[R_B + (1 - \alpha)R_{eq}]^2},$$

$$\frac{\partial I_C}{\partial \alpha} = N^* = \frac{(R_B + R_{eq})(k V_{CC} - V_{BE} + I_{CBO} R_{eq})}{[R_B + (1 - \alpha) R_{eq}]^2}. \tag{4.11}$$

The expression (4.11) gives the variation of I_C with α, and is a valuable measure of stability in its own right. The symbol for $\partial I_C/\partial \alpha$ is N^*.

Now return to the problem of finding N:

$$N = \frac{\partial I_C}{\partial \beta} = \frac{\partial I_C}{\partial \alpha}\frac{d\alpha}{d\beta} = N^* \frac{d\alpha}{d\beta}.$$

Substitute β for α in the expression for N^*:

$$\frac{\partial I_C}{\partial \alpha} = \frac{(R_B + R_{eq})(k V_{CC} - V_{BE} + I_{CBO} R_{eq})}{\left(R_B + \dfrac{R_{eq}}{1 + \beta}\right)^2}.$$

Since $\alpha = \beta/(1 + \beta)$ and $d\alpha/d\beta = [1/(1 + \beta)]^2$,

$$N = \frac{\partial I_C}{\partial \beta} = \frac{(R_B + R_{eq})(k V_{CC} - V_{BE} + I_{CBO} R_{eq})}{[(\beta + 1) R_E + R_{eq}]^2}. \qquad (4.12)$$

The factor N^* is often more convenient to use than N since it changes very little as β varies.

An additional, sometimes convenient relationship, is established by comparing the expressions for S and N^*, i.e., (4.7) and (4.11):

$$N^* = \frac{\partial I_C}{\partial \alpha} = S \times \frac{k V_{CC} - V_{BE} + I_{CBO} R_{eq}}{[R_E + R_{eq}(1 - \alpha)]}. \qquad (4.13)$$

There are many practical approximations which increase the utility of the above formulae. Consider a room temperature bias condition where leakage is a negligible component of collector current. The approximate collector current is easily obtained from (4.6):

$$I_C = I_Q \cong \frac{\dfrac{\beta}{1 + \beta}(k V_{CC} - V_{BE})}{R_E + \left(\dfrac{1}{1 + \beta}\right) R_{eq}}.$$

Comparing with (4.13),

$$N^* \cong S I_Q \left(\frac{\beta + 1}{\beta}\right) = S I_Q \left(\frac{1}{\alpha}\right), \qquad (4.14)$$

where I_Q is the quiescent collector current, neglecting leakage current. This formula shows how S may be used as a convenient figure of merit, even for discovering sensitivity to changes in β.

Since $N^* = \partial I_C / \partial \alpha$, the following approximate relations hold:

$$\Delta I_Q = N^* \Delta \alpha = S I_Q \left(\frac{1}{\alpha}\right) \Delta \alpha,$$

$$\frac{\Delta I_Q}{I_Q} = \text{per unit change in quiescent collector current} = S \frac{\Delta \alpha}{\alpha}. \qquad (4.15)$$

The percentage change in collector current equals S times the percentage change in α.

A further realistic simplification in the above formulae assumes that $R_E \gg R_{eq}/(1 + \beta)$. To minimize the influence of variations in β, it is important to adjust the circuit resistors so that this inequality is valid. When this is not the case, it is necessary to return to the more exact formulae as originally derived. The three sensitivity formulae simplify as follows:

$$S = \frac{R_E + R_{eq}}{R_E + \left(\dfrac{1}{1 + \beta}\right) R_{eq}} \cong 1 + \frac{R_{eq}}{R_E}. \qquad (4.16)$$

$$M = \frac{-\dfrac{\beta}{1 + \beta}}{R_E + \dfrac{R_{eq}}{1 + \beta}} \cong -\frac{1}{R_E} \quad (\text{for } \beta > 10). \qquad (4.17)$$

$$N^* = S \left[\frac{k V_{CC} - V_{BE} + I_{CBO} R_{eq}}{R_E + \dfrac{R_{eq}}{1 + \beta}}\right] \cong S \frac{I_Q}{\alpha}. \qquad (4.18)$$

PROBLEM 4.12 Refer to the circuit of Fig. 4.17. Assume $I_{CBO} = 3$ μa at room temperature.

(a) Calculate the current I_C in R_L using (4.6), after first determining the approximate operating point from the collector characteristics and the load line.

(b) Calculate V_{CE} at the operating point.

(c) Calculate S, M, and N^*.

(d) If $I_{CBO} = 3$ μa at 25°C, what change occurs in I_C due to the change in I_{CBO} at 30°C?

(e) If V_{BE} changes by -2.2 mv per degree centigrade, and is 0.22 v at 25°C, find the change in I_C resulting from the change in V_{BE} if the temperature increases from 25°C to 30°C.

(f) If β is reduced to 0.9 of its nominal value, what is the corresponding change in I_C?

(g) For the conditions of (d), what is the change in I_C between 25°C and 75°C?

(*Note*: For parts (c–f) above, use the approximate expressions for S, M, and N^*, which apply especially well to small changes.)

Solution: Refer to the basic formula of (4.6) and to Fig. 4.18 which shows the transistor collector characteristics. The formula is repeated here:

$$I_C = \frac{\dfrac{\beta}{1+\beta}\,(kV_{CC} - V_{BE}) + I_{CBO}\,(R_E + R_{eq})}{R_E + \dfrac{R_{eq}}{1+\beta}}. \qquad [4.6]$$

Now determine the numerical values of the parameters:

$$k = \frac{R_2}{R_1 + R_2} = \frac{1380}{3650 + 1380} = 0.274, \qquad R_{eq} = \frac{R_1 R_2}{R_1 + R_2} = \frac{1380 \times 3650}{5030} = 1000\ \Omega,$$

$$R_E = 50, \qquad R_E + R_{eq} = 1050\ \Omega, \qquad V_{CC} = 5\ \text{v}, \qquad kV_{CC} = 1.370\ \text{v}.$$

Fig. 4.17 Common-emitter amplifier with voltage divider providing base bias voltage.

Fig. 4.18 Common-emitter output characteristics at 25°C and 70°C with superimposed load line.

(a) On Fig. 4.18, draw a load line. The resistance which determines the slope of the load line is the sum of R_L and R_E (since $I_C \cong I_E$). Estimate the approximate voltage at point A of Fig. 4.17 as

$$V_A = 5 \times \frac{1380}{3650 + 1380} = 1.37 \text{ v}.$$

From Fig. 4.2, $V_{BE} = 0.22$ v; therefore the voltage at point B is $1.37 - 0.22 = 1.15$ v. For $R_E = 50 \, \Omega$, $I_E = 1.15/50 = 23$ ma. This establishes the operating point at P_1 (Fig. 4.18) where $I_B \cong 0.125$ ma (by interpolation) and $V_{CE} = 1.6$ v, and

$$\beta_{DC} = \frac{23}{0.125} = 184 \text{ (the d-c value } h_{FE}, \text{ not } h_{fe}).$$

Having determined the approximate operating point, using (4.6),

$$I_C = \frac{184}{185} \frac{(1.37 - 0.22) + (3 \times 10^{-6})(1050)}{50 + \dfrac{1000}{185}} = 20.8 \text{ ma}.$$

This corresponds to point P_2 where $I_B = 0.12$ ma.

(b) At P_2, $V_{CE} = 1.85$ v.

(c) The sensitivity formulae are

$$S \cong 1 + \frac{R_{eq}}{R_E} = 1 + \frac{1000}{50} = 21, \qquad [4.16]$$

$$M \cong \frac{-1}{R_E} = \frac{-1}{50} \cong -0.02 \text{ ma/mv}, \qquad [4.17]$$

$$N^* = \frac{S I_Q}{\alpha} = 21 \times \frac{20.8}{0.9946} = 0.44 \text{ a}, \qquad [4.18]$$

since

$$\alpha = \frac{\beta}{1 + \beta} = \frac{184}{185} = 0.9946.$$

(d) At 25°C, $I_{CBO} = 3 \, \mu$a. From Fig. 4.1, for a germanium transistor, I_{CBO} increases to 4.4 μa at 30°C. Therefore $\Delta I_{CBO} = 1.4 \, \mu$a and

$$\Delta I_C = S \Delta I_{CBO} = 21 \times 1.4 = 29 \, \mu\text{a}.$$

(e) Since, from 25°C to 30°C, $\Delta V_{BE} = -11$ mv,

$$\Delta I_C = -\frac{1}{R_E} \Delta V_{BE} = -0.02 \times \Delta V_{BE} = +0.22 \text{ ma}.$$

(f) The effect of a small reduction in β is easily estimated from N^* determined above:

$$\text{Nominal } \beta = 184, \qquad \alpha = \frac{184}{185} = 0.9946,$$

$$\text{Reduced } \beta = 0.9 \times 184 = 164, \qquad \alpha = \frac{164}{165} = 0.9939,$$

$$\Delta I_C = N^* \Delta \alpha = -0.0007 \times 0.44 = -0.31 \text{ ma}.$$

(g) From Fig. 4.1, I_{CBO} is 22 times greater at 70°C than at 25°C:

$$\Delta I_{CBO} = 3(22 - 1) = 63 \, \mu\text{a},$$

$$\Delta I_C \cong S \Delta I_{CO} = 21 \times 63 = 1.32 \text{ ma}.$$

Note that a more accurate calculation can be obtained by using (4.6). An example comparing the use of the fundamental bias equation with the simple approximation above is provided in Prob. 4.14.

(a)

PROBLEM 4.13 Figure 4.19a shows a *very general configuration* of a bias circuit, in which the collector-base feedback is incorporated for improved stability. Show that this circuit can be reduced in special cases to a simpler configuration by the following procedure:

(a) Draw the equivalent tee-circuit for Fig. 4.19a.
(b) Derive an expression for I_C including leakage current.
(c) Derive expressions for

$$S = \frac{\partial I_C}{\partial I_{CO}}, \qquad M = \frac{\partial I_C}{\partial V_{BE}}, \qquad N^* = \frac{\partial I_C}{\partial a}.$$

(d) Develop simple approximations to the above expressions.

Solution: (a) Figure 4.19b shows the equivalent tee-circuit sketched in accordance with the principles previously developed in Chaps. 1 and 3. The collector resistance r_D is assumed to be infinite.

(b) Write the basic circuit equations for Fig. 4.19b:

$$V_{CC} = I_B R_E + V_{BE} + I_D R_1 + (I_D + I_C) R_L. \tag{4.19}$$

$$V_{BE} + I_B R_E = (I_D - I_B) R_2. \tag{4.20a}$$

$$I_C = \beta I_B + (\beta + 1) I_{CBO}. \tag{4.2}$$

$$I_C = I_E - I_B. \tag{4.20b}$$

Combining (4.2) and (4.20b), solve for I_B:

$$I_B = \frac{I_E}{\beta + 1} - I_{CBO}. \tag{4.21}$$

Substitute (4.21) into (4.20a):

$$I_E R_E + V_{BE} - I_D R_2 = \left(\frac{-I_E}{\beta + 1} + I_{CBO} \right) R_2. \tag{4.22}$$

Now substitute (4.21) into (4.20b) and simplify:

$$I_C = I_E - I_B$$
$$= I_E \left(\frac{\beta}{\beta + 1} \right) + I_{CBO}. \tag{4.23}$$

Then solve (4.23) for I_E, and (4.22) for $I_D R_2$:

$$I_E = (I_C - I_{CBO}) \frac{\beta + 1}{\beta}.$$

$$I_D R_2 = I_E \left(R_E + \frac{R_2}{\beta + 1} \right) + V_{BE} - I_{CBO} R_2. \tag{4.24}$$

Substitute the expression for I_D from (4.24) and for I_C from (4.23) into (4.19) to obtain an equation in terms of I_E:

$$V_{CC} - V_{BE} = I_E R_E + I_E R_L \left(\frac{\beta}{1 + \beta} \right) + I_{CBO} R_L$$

$$+ (R_1 + R_L) \left[\frac{I_E}{R_2} \left(R_E + \frac{R_2}{\beta + 1} \right) + \frac{V_{BE}}{R_2} - I_{CBO} \right].$$


(b)
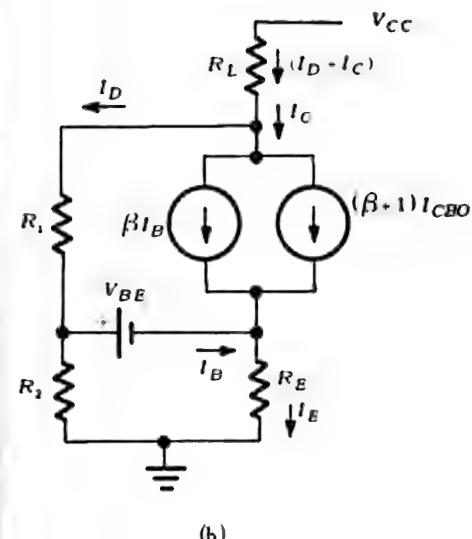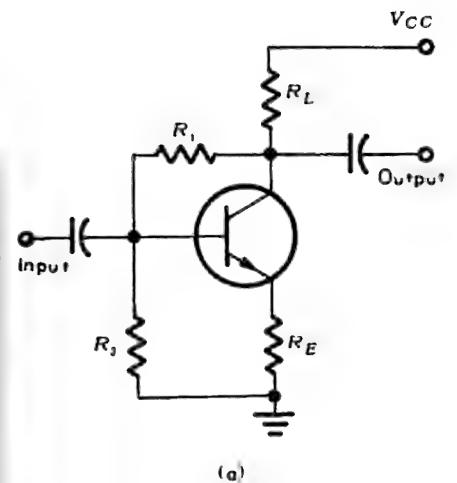
Fig. 4.19 (a) Generalized bias circuit incorporating feedback from collector to base for increased stability. (b) Simplified equivalent circuit.

Simplify by separating out terms in I_E:

$$V_{CC} - V_{BE} + I_{CBO} R_1 - \frac{V_{BE}}{R_2} (R_1 + R_L) = I_E \left[R_E + \frac{R_L \beta}{1 + \beta} + \left(\frac{R_1 + R_L}{R_2} \right) \left(R_E + \frac{R_2}{1 + \beta} \right) \right].$$

Solve the above expression for I_E and substitute in (4.23). This leads to an expression for I_C:

$$I_C = I_{CBO} + \frac{\beta}{1 + \beta} \left[\frac{V_{CC} - V_{BE} + I_{CBO} R_1 - \frac{V_{BE}}{R_2} (R_1 + R_L)}{R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) + R_L \left(\frac{\beta}{1 + \beta} + \frac{1}{1 + \beta} \right) + \frac{R_1}{1 + \beta}} \right]. \quad (4.25)$$

Combine terms (4.25) and simplify to obtain a final general expression for I_C:

$$I_C = \frac{\frac{\beta}{1 + \beta} \left[V_{CC} - V_{BE} \left(1 + \frac{R_1 + R_L}{R_2} \right) \right] + I_{CBO} \left[R_1 + R_L + R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) \right]}{R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) + R_L + \frac{R_1}{1 + \beta}}. \quad (4.26)$$

This is the required expression for I_C.

(c) By partial differentiation of (4.26), $S = \partial I_C / \partial I_{CBO}$ is obtained:

$$S = \frac{\partial I_C}{\partial I_{CBO}} = \frac{R_1 + R_L + R_E \left(1 + \frac{R_1 + R_L}{R_2} \right)}{R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) + R_L + \frac{R_1}{1 + \beta}}. \quad (4.27)$$

Similarly,

$$M = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\frac{\beta}{1 + \beta} \left(1 + \frac{R_1 + R_L}{R_2} \right)}{R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) + R_L + \frac{R_1}{1 + \beta}}. \quad (4.28)$$

Remembering that $\alpha = \beta / (1 + \beta)$ and $1 + \beta = 1/(1 - \alpha)$, substitute in (4.26):

$$I_C = \frac{\alpha \left[V_{CC} - V_{BE} \left(1 + \frac{R_1 + R_L}{R_2} \right) \right] + I_{CBO} \left[R_1 + R_L + R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) \right]}{R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) + R_L + (1 - \alpha) R_1}. \quad (4.29)$$

Differentiating with respect to α,

$$N^* = \frac{\partial I_C}{\partial \alpha} = \frac{\left[V_{CC} - V_{BE} \left(1 + \frac{R_1 + R_L}{R_2} \right) \right] + I_{CBO} R_1 \left[R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) + R_1 + R_L \right]}{\left[R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) + R_L + R_1 (1 - \alpha) \right]^2}. \quad (4.30)$$

By comparing (4.27) and (4.30), the following simplification is obtained:

$$N^* = \frac{V_{CC} - V_{BE} \left(1 + \frac{R_1 + R_L}{R_2} \right)}{R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) + R_L + R_1 (1 - \alpha)} S$$

$$+ I_{CBO} R_1 \frac{S}{R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) + R_2 + R_1 (1 - \alpha)}. \quad (4.31)$$

(d) Examine the expression for I_C in (4.29) for the case where I_{CBO} at room temperature is small compared with I_C. For this condition,

$$I_Q \cong \frac{\alpha \left[V_{CC} - V_{BE} \left(1 + \frac{R_1 + R_L}{R_2} \right) \right]}{R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) + R_L + R_1 (1 - \alpha)}. \tag{4.32}$$

Comparing this expression with the value of N^* in (4.31) for $I_{CBO} \cong 0$,

$$N^* = \frac{I_Q S}{\alpha}. \tag{4.33}$$

This last expression again demonstrates that S is a good measure of quiescent point stability, even with respect to changes in α.

Further approximations may be introduced:

$$\beta \gg 1,$$

$$\frac{R_1}{1 + \beta} \ll R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) + R_L.$$

Substituting in the expressions for S, M, and N^*,

$$S \cong 1 + \frac{R_1}{R_E \left(1 + \frac{R_1 + R_L}{R_2} \right) + R_L}, \tag{4.34}$$

$$M \cong \frac{-1}{R_E + \frac{R_L}{1 + \frac{R_1 + R_L}{R_2}}}, \tag{4.35}$$

$$N^* \cong \frac{S I_Q}{\alpha}. \tag{4.36}$$

Now let us apply the above formulae to a numerical example.

PROBLEM 4.14 Solve the circuit of Fig. 4.20, for the following quantities:

(a) The operating point (I_C, V_{CE}).

(b) The sensitivity formulae S, M, and N^*.

(c) Using the results of (b), compute I_C at 70°C. Assume β increases 1.5 times, I_{CBO} goes from 3 μa to 66 μa, and V_{BE} changes from 0.22 v to 0.12 v.

(d) Repeat (c) using the exact bias formula.

Use the output characteristics of Fig. 4.21.

Solution: (a) As a first approximation, assume I_L and I_E are equal (a perfectly realistic assumption), and draw a load line on the characteristics curve of Fig. 4.21. Assume further that $I_B \ll I_D$, $I_D \ll I_C$, and therefore, $I_C \cong I_E$. Then,

$$(V_{CC} - I_E R_L) \frac{R_2}{R_1 + R_2} = I_E R_E + 0.22.$$

Substituting numerical values,

$$(5 - 100 I_E)(0.455) = 50 I_E + 0.22.$$

Solve for I_E:

$$I_E = 21.5 \text{ ma} \cong I_C.$$

This operating point is shown as P_1 on Fig. 4.21. Note $I_B = 0.12$ ma and $V_{CE} = 1.8$ v.
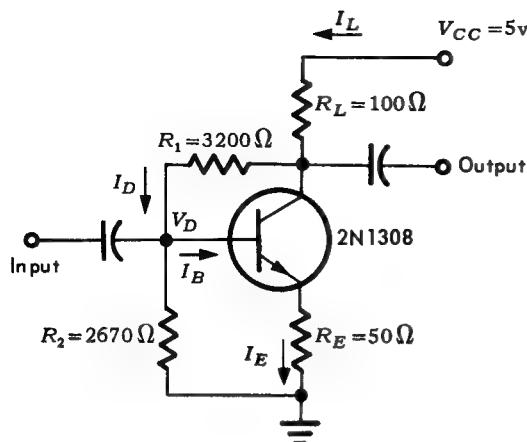
Fig. 4.20 Bias circuit incorporating
collector-base feedback.
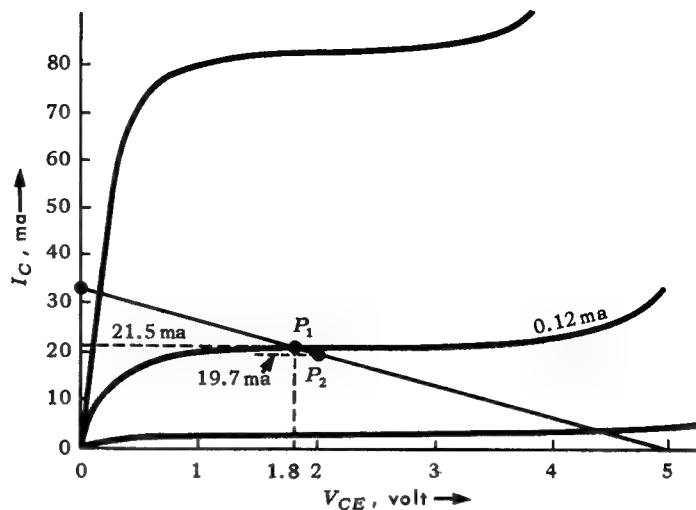
Fig. 4.21 Collector characteristics with superim-
posed load line for Prob. 4.14.

Hence,

$$\beta_{DC} = \text{d-c current gain} = \frac{21.5}{0.12} = 179.$$

This preliminary calculation has given us an approximate result, in particular, an approximate value for β_{DC}. This value, together with the circuit parameters of Fig. 4.20, permit a more accurate calculation of I_C. For convenience, (4.26) is repeated here:

$$I_C = \frac{\dfrac{\beta}{1+\beta}\left[V_{CC} - V_{BE}\left(1 + \dfrac{R_1 + R_L}{R_2}\right)\right] + I_{CBO}\left[R_1 + R_L + R_E\left(1 + \dfrac{R_1 + R_L}{R_2}\right)\right]}{R_E\left(1 + \dfrac{R_1 + R_L}{R_2}\right) + R_L + \dfrac{R_1}{1+\beta}}. \quad [4.26]$$

The numerical values to be substituted are

$$\beta = 179, \qquad R_1 = 3200 \ \Omega, \qquad R_2 = 2670 \ \Omega, \qquad R_L = 100 \ \Omega,$$

$$R_E = 50 \ \Omega, \qquad I_{CBO} = 3 \times 10^{-6} \ a, \qquad V_{BE} = 0.22 \ v, \qquad V_{CC} = 5 \ v.$$

Now make the substitutions:

$$I_C = \frac{\dfrac{179}{180}\left[5 - 0.22\left(1 + \dfrac{3300}{2670}\right)\right] + (3 \times 10^{-6})(3200 + 100 + 112)}{112 + 100 + \dfrac{3200}{180}}$$

$$= 19.7 \ ma.$$

This gives point P_2 on Fig. 4.21. Since this is in the close vicinity of P_1 in an essentially linear region, the value of β may be assumed as unchanged. At P_2, $V_{CE} = 2.02$ v.

(b) The sensitivity formulae are

$$S \cong 1 + \frac{R_1}{R_E\left(1 + \dfrac{R_1 + R_L}{R_2}\right) + R_L} = 1 + \frac{3200}{112 + 100} = 16, \qquad [4.34]$$

$$M \cong \frac{-1}{R_E + \dfrac{R_L}{1 + \dfrac{R_1 + R_L}{R_2}}} = \frac{-1}{50 + \dfrac{100}{1 + \dfrac{3300}{2670}}} = -0.0105. \qquad [4.35]$$

From (4.33), assuming low I_{CBO} at room temperature,

$$N^* \cong \frac{S}{\alpha} I_Q = \frac{16}{0.9944} \times 19.7 \times 10^{-3} = 0.316.$$

(c) By definition, $\Delta I_C = S\Delta I_{CBO} + M\Delta V_{BE} + N^*\Delta \alpha$. The given data is

$$\Delta I_{CBO} = +63 \times 10^{-6}, \quad \Delta V_{BE} = -0.1 \text{ v}, \quad \Delta\alpha = 0.0019.$$

Note that at $\beta = 1.5 \times 179 = 269$, $\alpha = 0.9963$. For $\beta = 179$, $\alpha = 0.9944$. Therefore $\Delta\alpha = 0.0019$. Now substituting numerical values,

$$\Delta I_C = 16 \times 63 \times 10^{-6} + (-0.0105)(-0.1) + 0.316 \times 0.0019$$
$$= 1.01 \times 10^{-3} + 1.05 \times 10^{-3} + 0.60 \times 10^{-3}$$
$$= 2.66 \text{ ma.}$$

At room temperature, I_C was 19.7 ma. At 70° C, $I_C = 19.7 + 2.66 = 22.4$ ma..

(d) The collector current is

$$I_C = \frac{\dfrac{269}{270}\left[5 - 0.12\left(1 + \dfrac{3300}{2670}\right)\right] + (66 \times 10^{-6})(3200 + 100 + 112)}{112 + 100\dfrac{3200}{270}}$$
$$= 22.1 \times 10^{-3} \text{ a}$$
$$= 22.1 \text{ ma.}$$

The excellent correlation between approximate and exact results demonstrates the validity of the approximation.

4.6 Emitter Bias Circuit

The emitter bias circuit of Fig. 4.22 is an especially useful configuration that may be analyzed by straight-forward circuit methods as illustrated in the following examples.

PROBLEM 4.15 Referring to Fig. 4.22, determine the following: I_C, S, M, and N^*.

Solution: Calculate I_C, using the previously developed fundamental relations:

$$I_C = \beta I_B + (\beta + 1) I_{CBO}, \qquad [4.2]$$
$$I_B = I_E - I_C.$$

Therefore,

$$V_{EE} - V_{BE} = I_E R_E + I_B R_1 = I_E R_E + I_E R_1 - I_C R_1,$$
$$I_C = \beta I_E - \beta I_C + (\beta + 1) I_{CBO},$$
$$I_E = \frac{V_{EE} - V_{BE} + I_C R_1}{R_E + R_1}.$$
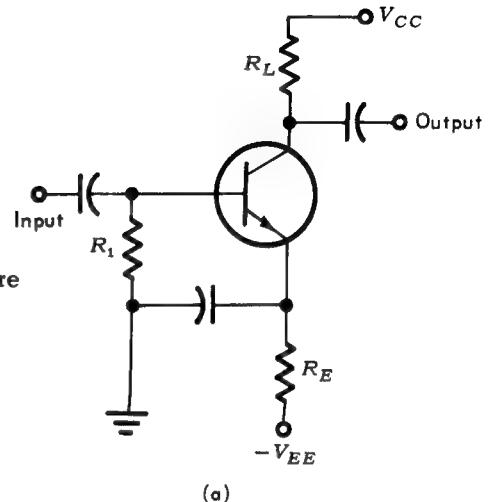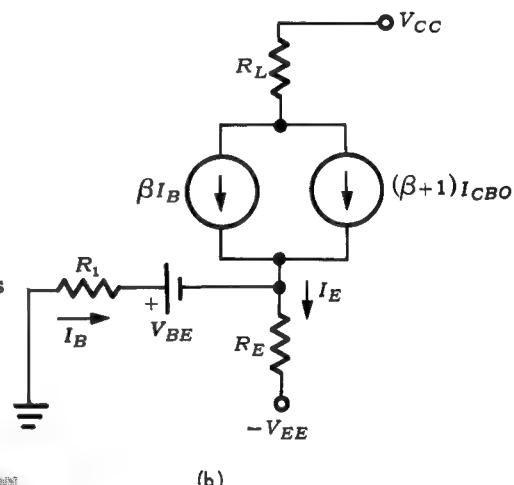
Fig. 4.22 (a) Bias circuit using a separate source of emitter bias voltage. (b) Simplified tee-equivalent circuit.

Combining equations and solving,

$$(\beta + 1)I_C = \frac{\beta I_C R_1 + \beta V_{EE} - \beta V_{BE} + (\beta + 1)I_{CBO}(R_E + R_1)}{R_E + R_1}.$$

The last expression may be simplified and solved for I_C:

$$I_C = \frac{\dfrac{\beta}{\beta + 1}(V_{EE} - V_{BE}) + I_{CBO}(R_E + R_1)}{R_E + \dfrac{R_1}{1 + \beta}}. \qquad (4.37)$$

Equation (4.37) for the emitter bias configuration is the same as (4.6) with $R_1 R_2/(R_1 + R_2) \cong R$ and $V_{CC}[R_2/(R_1 + R_2)] \cong V_{EE}$. Therefore all formulae dealing with the circuit of Fig. 4.16 can be applied to Fig. 4.22 as shown below:

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{R_E + R_1}{R_E + \dfrac{R_1}{1 + \beta}}, \qquad (4.38)$$

$$M = \frac{\partial I_C}{\partial V_{BE}} = -\frac{\dfrac{\beta}{\beta + 1}}{R_E + \dfrac{R_1}{1 + \beta}} = -\frac{\beta}{R_E(1 + \beta) + R_1}, \qquad (4.39)$$

$$N^* = \frac{V_{EE} - V_{BE}}{R_E + \dfrac{R_1}{1 + \beta}} S + \frac{I_{CBO} R_1}{R_E + \dfrac{R_1}{1 + \beta}} S. \qquad (4.40)$$

As before, if I_{CBO} at the quiescent point is essentially negligible,

$$N^* \cong \frac{I_Q S}{\alpha}.$$

Fig. 4.23 Emitter bias circuit for Prob. 4.16.

PROBLEM 4.16 For the circuit of Fig. 4.23, calculate the values of I_C and S.

Solution: Examine the collector characteristics of Fig. 4.18. Observe that $V_{EE} + V_{CC} = 5$ v is applied to R_E and R_L in essentially a series circuit. As previously described (Prob. 4.12), we get an estimated $I_C = 23$ ma, and a preliminary value of β of 184. More accurately, using (4.37),

$$I_Q = I_C = \frac{\dfrac{\beta}{1 + \beta}(V_{EE} - V_{BE}) + I_{CBO}(R_E + R_1)}{R_E + \dfrac{R_1}{1 + \beta}} = \frac{\dfrac{184}{185}(1.37 - 0.22) + 3 \times 10^{-6}(1050)}{50 + \dfrac{1000}{185}}$$

$$= 20.8 \text{ ma},$$

From (4.38),

$$S = \frac{R_E + R_1}{R_E + \dfrac{R_1}{1 + \beta}} = \frac{1050}{55.4} = 19.$$

The emitter bias circuit is particularly advantageous when the base is driven by an input transformer. Bias is, of course, adjusted by choosing V_{EE} and R_E, while the base is essentially at ground potential with respect to d-c. With $R_B \cong 0$, the stability factor is unity, a theoretically optimum condition:

$$N^* \cong \frac{I_Q}{\alpha} \qquad S \cong I_Q.$$

This leads to a desirable low value of N^*. There is no particular improvement in M.

4.7 Bias Compensation

When a particular circuit configuration is selected, it is possible to improve stability by using the nonlinear and temperature-sensitive characteristics of auxiliary diodes and transistors. Some of these compensation methods are now illustrated in the following examples.

PROBLEM 4.17 For a common-emitter circuit with an n-p-n transistor, show how to use a diode to compensate for the effects of temperature change on V_{BE}.

Solution: Figure 4.24 shows a circuit using diode compensation. The current I is adjusted so that V_D (the forward diode drop) equals V_{BE} (thus cancelling one another). The values of R_1 and R_2 are adjusted for the required bias.

The cancellation occurs over a wide temperature range because the diode and transistor junctions follow identical laws. The circuit becomes equivalent to that of Fig. 4.16 but with $V_{BE} = 0$ over the whole temperature range.

PROBLEM 4.18 The circuit of Fig. 4.25 shows a method of compensating for the effects of temperature on I_{CBO}. Analyze the circuit's performance.

Solution: Leakage current I_{CBO} flows in transistors Q_1 and Q_2. If the transistors are matched, the leakage currents should be equal over the temperature range. The I_{CBO} drawn from the base circuit of Q_1 by Q_2 results in a reduction of βI_{CBO} in the collector current of Q_1. As the component of I_{C_1} corresponding to leakage current is $I_{CBO}(1 + \beta)$, the effective collector leakage is reduced from $(\beta + 1)I_{CBO}$ to I_{CBO}, thereby providing the required compensation.

Both compensation techniques described above can be used simultaneously, but are not required very often. Circuits are generally designed for good bias stability with passive elements, and relatively complex compensation methods are thus avoided. It is both difficult to match transistors and to hold junctions at equal temperatures. Compensation with diodes and transistors is used only in special cases.

4.8 Self-Heating

Transistor parameters must correspond to *actual junction temperatures* for accurate analysis of transistor performance. The junction temperature is the *sum of ambient temperature T_a plus a temperature rise resulting from power dissipation* at the junction. For small-signal amplifiers, junction dissipation is almost entirely due to bias currents. Since $I_C \cong I_E$, the total power dissipation at the *two* junctions of a transistor is essentially $V_{CE}I_C$. (Situations in which this is not the case will be discussed elsewhere.)

The junction temperature is

$$T_j = T_a + (\theta_{j-a})I_C V_{CE}, \qquad (4.41)$$

where θ_{j-a} is the *thermal resistance* from the junctions to the ambient environment expressed in °C/watt. Thermal resistance θ_{j-a} is normally given on transistor data sheets for specific recommended mountings (heat sinks) in free air.
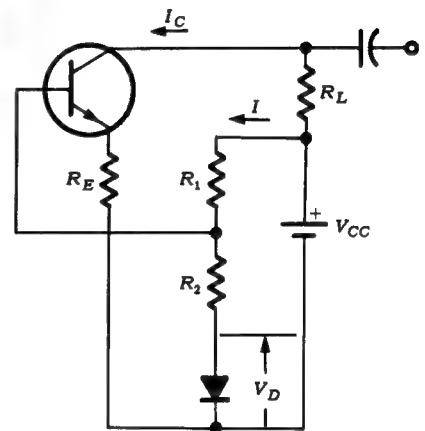
Fig. 4.24 Circuit with diode bias compensation.
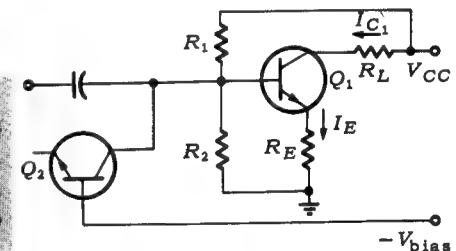
Fig. 4.25 Method of compensation for the effect of temperature on I_{CBO}.

The problem of including temperature rise in transistor calculations results from the fact that I_C *must be evaluated at the final junction temperature*, which is unknown at the start of calculations. *Iterative procedures* are suggested, but are rarely warranted.

PROBLEM 4.19 For the circuit of Fig. 4.26 at an ambient temperature of 70°C, calculate I_C. Include the effect of junction temperature rise due to power dissipation. Assume $\theta_{j-a} = 200°C/w$, and that β is independent of temperature.

Solution: The circuit is identical to that of Fig. 4.17 in Prob. 4.12. We therefore use the results of that problem as an initial approximation:

$$I_C \text{ at } 25°C = 20.8 \text{ ma},$$

$$\Delta I_{C_1} \text{ (due to change in } I_{CBO}) = 1.32 \text{ ma (for } 70°C),$$

$$M = -0.02 \text{ ma/mv}.$$

Since we are evaluating operation at 70°C,

$$\Delta T = 70°C - 25°C = 45°C,$$

$$\Delta V_{BE} = -45 \times 2.2 = -99 \text{ mv},$$

$$\Delta I_{C_2} = M \Delta V_{BE} = \left(-0.02 \frac{ma}{mv}\right)(-99 \text{ mv}) \cong 2 \text{ ma}.$$

The increased collector current at 70°C can be estimated as

$$I_{C(70°C)} = I_{C(25°C)} + \Delta I_{C_1} + \Delta I_{C_2} = 20.8 + 1.3 + 2 \cong 24 \text{ ma}.$$
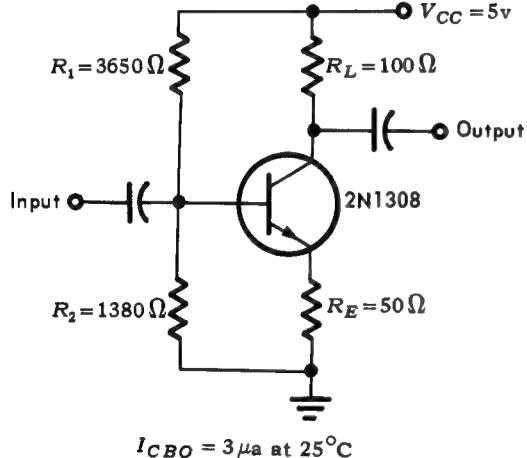
Fig. 4.26 Circuit for self-heating calculation.
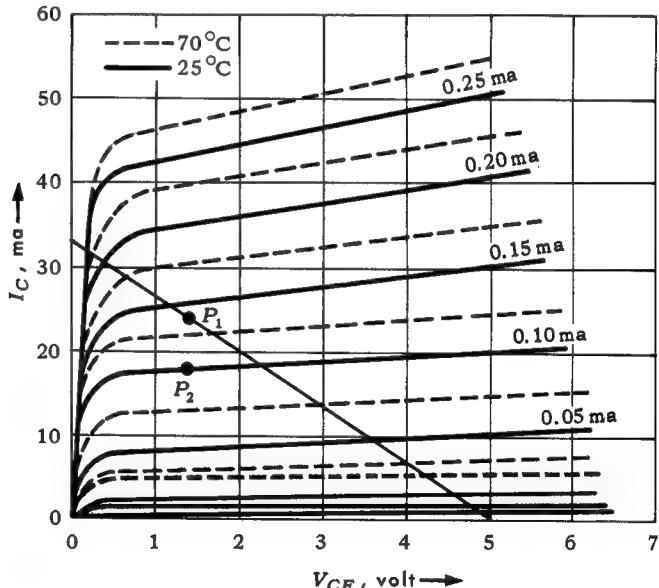
Fig. 4.27 Collector characteristics of the 2N1308 transistor with superimposed load line.

From the load line (Fig. 4.27), the operating point P_1 is at $I_C = 24$ ma, $V_{CE} = 1.4$ v. Therefore,

$$T_j = T_a + \theta_{j-a}(I_C V_{CE}) = 70 + 200(0.024 \times 1.4) = 76.7°C.$$

Since it is assumed that β does not vary with temperature, a value which does not include an I_{CBO} component is required. This is obtained, for all practical

purposes, from the room temperature characteristics in which I_{CBO} is a very small percentage of I_C. From point P_2 on the characteristic curves,

$$I_C = 17.5 \text{ ma},$$

$$I_B = 0.1 \text{ ma},$$

$$\beta = \frac{I_C}{I_B} = 175.$$

Using the high temperature value of I_{CBO}, I_{CBO} (at 76.7°C) $= 35 \times I_{CBO}$ at 25°C (see Fig. 4.1). Now substituting the numerical values in (4.6),

$$I_C = \frac{\dfrac{175}{176}\left(5 \times \dfrac{1380}{5030} - 0.12\right) + (3 \times 35 \times 10^{-6})(50 + 1000)}{50 + 5.7} = 24.3 \text{ ma}.$$

This value is close enough to the previously calculated 24 ma so as not to require an improved approximation.

PROBLEM 4.20 In the circuit of Fig. 4.28, calculate I_C at an ambient temperature of 45°C. Assume that $I_{CBO} = 3\ \mu a$ at 25°C is the specified maximum leakage, and $\theta_{j-a} = 100°C/w$. Use the characteristic curves of Figs. 4.2-3. The diode is adjusted for the same voltage drop as V_{BE} at its operating point.

Solution: As a first approximation, the voltage at A is

$$V_A \cong 5\left(\frac{20}{930}\right) + V_D = 0.108 + V_D.$$

Since $V_D = V_{BE}$, the voltage across R_E is

$$V_E = V_A - V_{BE} = 0.108 + V_D - V_{BE} = 0.108,$$

$$I_E = \frac{V_E}{R_E} = \frac{0.108}{2} = 54 \text{ ma} \cong I_C.$$
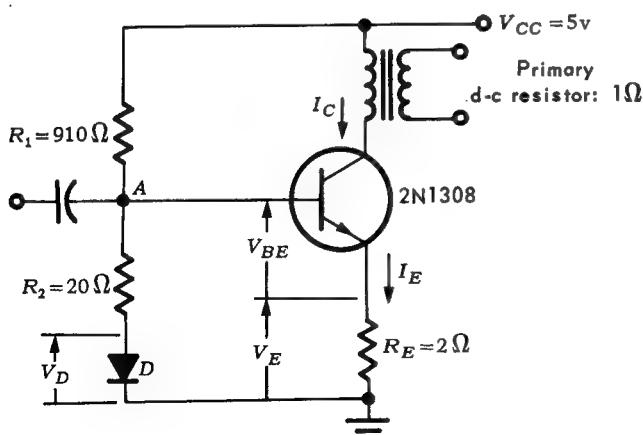
Fig. 4.28 Amplifier circuit with bias compensation for temperature variation of V_{BE}.
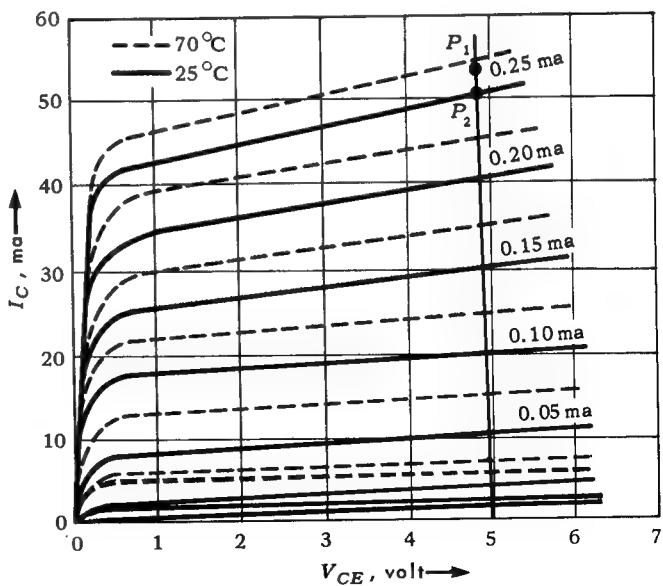

Fig. 4.29 Collector characteristics of the 2N1308 transistor with superimposed load line.

Now consider junction temperature effects. Power dissipation = 0.054 V_{CE}. On Fig. 4.29, draw a load line for $R_L + R_E = 3\,\Omega$. At 54 ma or point P_1, $V_{CE} = 4.84$ v ($V_{CE} = V_{CC} - R_L I_C - R_E I_E$). This gives

Power dissipation = $P_j = 0.054 \times 4.84 = 0.262$ w,

Junction temperature = $T_j = T_a + \theta_{j-a}(I_C V_{CE}) = 45 + (0.262 \times 100) = 71\,°C$.

Use this estimated operating temperature for a more accurate calculation of I_C by means of (4.6). Since V_{BE} and the diode forward voltage drops are always equal, they may *both* be ignored with no sacrifice of accuracy.

In the region of interest, β can be obtained from Fig. 4.29. It is the d-c β, excluding any I_{CBO} component, which may therefore be taken from the 25°C curves (as before). At point P_2, $I_C = 50.5$ ma, $I_B = 0.25$ ma, $\beta = 50.5/0.25 = 202$. From Fig. 4.1, $I_{CBO} = I_{CBO}\,(25°C) \times 22 = 66\,\mu a$. Substituting in (4.6),

$$I_C = \frac{\dfrac{202}{203}\left(5 \times \dfrac{20}{930}\right) + 66 \times 10^{-6}(2 + 19.6)}{2 + 0.097} = 52 \text{ ma},$$

$$T_j = 45 + (100 \times 4.84 \times 52 \times 10^{-3}) = 70.2\,°C.$$

This is close enough to the first approximation so as not to warrant an additional computation.

PROBLEM 4.21 If the diode D of Fig. 4.28 is omitted and R_2 is increased to $65\,\Omega$, calculate I_C at an ambient temperature $T_a = 45°C$. Assume I_{CBO} is negligible at room temperature. Also assume, as before, a thermal resistance of 100°C/w junction dissipation.

Solution: Calculate V_A:

$$V_A = \frac{65}{975} \times 5 = 0.33 \text{ v}$$

(approximately, neglecting base current drawn from the voltage divider).
From Fig. 4.2, $V_{BE} = 0.22$; $I_{CBO} \cong 3\,\mu a$ (assumed negligible). Hence,

$$V_E = V_A - V_{BE} = 0.33 - 0.22 = 0.11 \text{ v},$$

$$I_E = \frac{V_E}{R_E} = \frac{0.11}{2} = 55 \text{ ma}.$$

For a more accurate value of I_C, using $\beta \cong 202$, from Prob. 4.20, and substituting in (4.6),

$$I_C = \frac{\dfrac{202}{203}(0.33 - 0.22) + 0}{2 + 0.3} = 48 \text{ ma}.$$

Using this value of collector current, estimate the junction temperature T_j. Let $P_j = I_C V_{CE}$ = approximate junction dissipation.
Then,

$$P_j = I_C V_{CE} = \frac{48}{1000}\,[5 - 3\,(0.048)] = 0.233 \text{ w}.$$

$$T_j = T_a + \theta_{j-a} P_j = 45 + 100\,(0.233) = 68.3\,°C.$$

At this high junction temperature, leakage current increases markedly, and must be included in a more accurate temperature estimate. From Fig. 4.1, at 68.3°C, $I_{CBO} = 63 \times 10^{-6}$ a. From Fig. 4.2, $V_{BE} = 0.12$ v. Substituting in (4.6),

$$I_C = \frac{\dfrac{202}{203}(0.33 - 0.12) + 63 \times 10^{-6}(2 + 60.5)}{2 + \dfrac{60.5}{203}} = 93 \text{ ma}.$$

Therefore,

$$V_{CE} = 5 - \frac{93 \times 3}{1000} = 4.72$$

and

$$T_j = 45 + 100\left(\frac{93}{1000}\right)(4.72) = 89°C.$$

The temperature at the junction has increased sufficiently above the previous estimates to warrent a third approximation.

Assume now a junction temperature of 89°C. At this temperature,

$$V_{BE} = 0.12 - (19 \times 2.2 \times 10^{-3}) = 0.078 \text{ v}.$$

(Note that $V_{BE} = 0.12$ at 70°C, and changes -2.2 mv/°C.) From Fig. 4.1, I_{CBO} increases one hundred fold over the value at 25°C. Again using (4.6), it is found that $I_C = 117$ ma and

$$V_{CE} = 5 - 0.117(3) = 4.65 \text{ v}.$$

Hence,

$$T_j = 45 + (100 \times 0.117 \times 4.65) = 99.5°C.$$

Note that once again the previous calculation was inaccurate, and a try at a closer approximation is indicated.

At 99.5°C, $V_{BE} = 0.12 - (29.5 \times 2.2 \times 10^{-3}) = 0.055$ v; $I_{CBO} = 180$ times the room temperature value, or 0.540 ma, and $I_C = 130$ ma.

This successive approximation process could be continued until the series of values of I_C converges, if it ever does. Because a germanium transistor cannot operate above a junction temperature of about 100°C, the calculations become academic; the transistor will eventually be destroyed. This process, resulting from the reduction in V_{BE} with increasing temperature, can be avoided by bias compensation.

4.9 Thermal Runaway

There is another type of thermal destruction generally called *thermal runaway*. This is caused by a *regenerative increase in* I_{CBO}. Increasing temperature leads to increasing I_{CBO} with its associated increase in dissipation, in turn leading to further heating, and a continuation of the process. Leakage current I_{CBO} increases until it is limited by the external circuit, or until the transistor is destroyed. This section presents an approximate analysis of thermal runaway.

There are *three* basic equations required for the analysis of thermal runaway in the circuit of Fig. 4.30:

$$T_j = T_a + \theta_{j-a}P_j, \tag{4.42}$$

$$P_j \cong I_C V_{CE}, \tag{4.43}$$

$$V_{CE} \cong V_{CC} - I_C(R_E + R_L). \tag{4.44}$$

These expressions may be combined and differentiated to arrive at the thermal runaway condition in which the increase in I_{CBO} due to an increase in tempera-
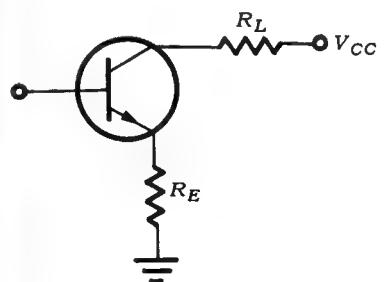
Fig. 4.30 Simplified circuit for analysis of thermal runaway.

ture leads in turn to a further increase in I_{CBO} and corresponding futher increase in temperature, etc., until runaway occurs.

PROBLEM 4.22 Using the above equations and the circuit of Fig. 4.30 as a starting point, establish the condition for thermal runaway.

Solution: Combining (4.42) and (4.43),

$$T_j = T_a + \theta_{j-a} V_{CE} I_C. \qquad [4.41]$$

Differentiating (4.41) with respect to T_j,

$$\frac{dT_j}{dT_j} = \left[\frac{\partial I_C}{\partial T_j} V_{CE} + \frac{\partial V_{CE}}{\partial T_j} I_C \right] \theta_{j-a} = 1. \qquad (4.45)$$

Also,

$$\frac{\partial I_C}{\partial T_j} = \frac{\partial I_C}{\partial I_{CBO}} \times \frac{\partial I_{CBO}}{\partial T_j}.$$

From (4.44),

$$\frac{dV_{CE}}{\partial T_j} = -(R_E + R_L) \frac{\partial I_C}{\partial I_{CBO}} \times \frac{\partial I_{CBO}}{\partial T_j}.$$

Substituting in (4.45),

$$\frac{1}{\theta_{j-a}} = \frac{\partial I_C}{\partial I_{CBO}} \times \frac{\partial I_{CBO}}{\partial T_j} [V_{CC} - I_C (R_E + R_L)] + (-I_C)(R_E + R_L) \frac{\partial I_C}{\partial I_{CBO}} \times \frac{\partial I_{CBO}}{\partial T_j}.$$

Simplifying, and recalling that $\partial I_C / \partial I_{CBO} = S$,

$$\frac{1}{\theta_{j-a}} = S \frac{\partial I_{CBO}}{\partial T_j} [V_{CC} - 2 I_C (R_E + R_L)]. \qquad (4.46)$$

This expression represents an equilibrium condition, wherein the increased I_{CBO} and dissipation at high temperature are compared to the associated temperature rise for the increased I_{CBO}. Thermal runaway occurs when either S or θ_{j-a} is increased, upsetting the equality of (4.46).

Thus, the condition for stability is

$$\frac{1}{\theta_{j-a} \cdot S} > \frac{\partial I_{CBO}}{\partial T_j} [V_{CC} - 2 I_C (R_E + R_L)]. \qquad (4.47)$$

PROBLEM 4.23 Remembering that I_{CBO} for germanium approximately doubles for every 10°C rise in temperature, modify (4.47) by substituting an appropriate expression for $\partial I_{CBO} / \partial T_j$.

Solution: Let I_{CBO} = leakage current at a reference operating point and temperature. Let temperature increase from T_{jQ} to T_j. Then,

$$I_{CBO} = I_{CBOQ} \times 2^{\frac{T_j - T_{jQ}}{10}},$$

$$\ln I_{CBO} = \ln I_{CBOQ} + \left(\frac{T_j - T_{jQ}}{10} \right) \ln 2.$$

Differentiating,

$$\frac{dI_{CBO}}{I_{CBO}} = \frac{\ln 2}{10} dT_j,$$

or

$$\frac{dI_{CBO}}{dT_j} = 0.0695 \, I_{CBO} \cong 0.07 \, I_{CBO} \,. \tag{4.48}$$

Substitute (4.48) into (4.47):

$$\frac{1}{\theta_{j-a} S} > 0.07 \, I_{CBO} \, [V_{CC} - 2I_C \, (R_E + R_L)]. \tag{4.49}$$

This expression applies to germanium transistors. Silicon transistors almost never exhibit thermal runaway due to their low leakage. The values of I_C and I_{CBO} must correspond to the highest design value of junction temperature. Because of the approximate nature of the analysis, large safety factors are suggested in design to avoid thermal runaway.

PROBLEM 4.24 (a) For the circuit of Fig. 4.28, calculate the stability factor S at 70°C. (b) Determine whether thermal runaway occurs at 70°C. Use the collector characteristics of Fig. 4.3. For this particular transistor, θ_{j-a} is 100°C/w. Assume that $I_{CBO} = 200 \, \mu a$ at 70°C, the poorest case condition. At 70°C, $V_{BE} = 0.12$ v, but is compensated by diode D. Thus, variation of V_{BE} with temperature does not aggravate the thermal stability problem.

Solution: (a) The stability factor is given by the expression

$$S = \frac{R_E + \dfrac{R_1 R_2}{R_1 + R_2}}{R_E + \dfrac{R_1 R_2}{R_1 + R_2} \dfrac{1}{1 + \beta}} \,. \tag{4.16}$$

Calculations are to be carried out at 70°C. First, calculate the approximate emitter current:

$$V_A = 5 \times \frac{20}{20 + 910} = 0.108 \text{ v}$$

(since $V_{BE} = V_D$).

Therefore, the drop across the $2\,\Omega$ emitter resistor equals the drop across the $R_2 = 20\,\Omega$ resistor:

$$I_E = \frac{V_E}{R_E} = \frac{0.108}{2} = 0.054 \text{ a.}$$

Refer to Fig. 4.31. Draw the load line, locate point P, and determine β in this region. This has been done in Prob. 4.20, in which $\beta = 202$, so that we will use this value to determine S:

$$S = \frac{2 + \dfrac{20 \times 910}{930}}{2 + \dfrac{20 \times 910}{930} \dfrac{1}{203}} = 10.3.$$

From (4.49),

$$\frac{1}{S\theta_{j-a}} > 0.0695 \, (200 \times 10^{-6}) \, [5 - (0.108)(3)] = 65 \times 10^{-6},$$

$$\frac{1}{S\theta_{j-a}} = \frac{1}{10.3 \times 100} = 970 \times 10^{-6} > 65 \times 10^{-6}.$$
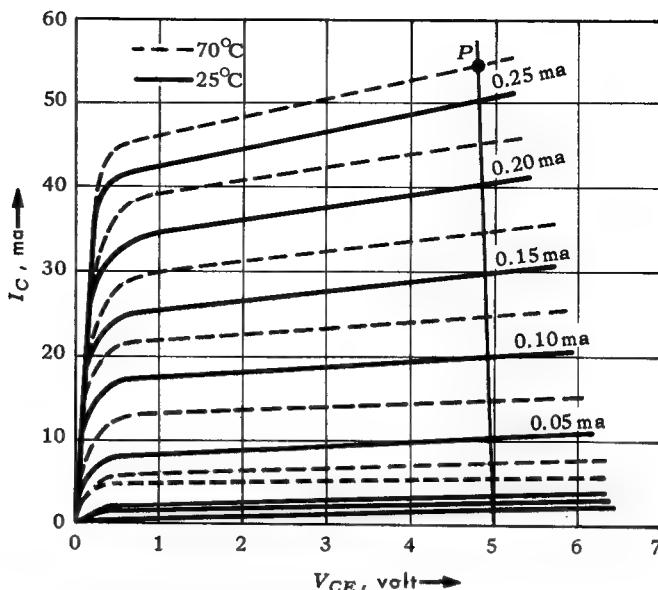
Fig. 4.31 Collector characteristics of the 2N1308 transistor with superimposed load line.
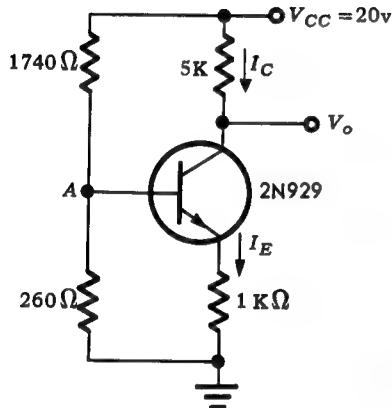
Fig. 4.32 Evaluating V_o by an approximate analysis.

Fig. 4.33 Evaluating I_C by an approximate analysis.

This represents a stable system and thermal runaway will not occur. Again, due to the approximate knowledge of I_{CBO}, θ_{j-a}, and therefore T_j, it is important to calculate for the worst possible conditions using ample safety factors.

Experimentally, T_j is determined from V_{BE}. Either the manufacturers' data on V_{BE} are used, or, if greater accuracy is required, V_{CE} vs. temperature for a fixed value of I_E may be determined experimentally.

4.10 Approximation Techniques

The analytical techniques developed above provide accurate circuit solutions. However, it is important to start out with approximate operating points, so that preliminary calculations can be accomplished quickly. The examples below illustrate methods for rapidly approximating the operating point of transistor circuits. These methods are also of value in setting up bias conditions in the initial stages of circuit design. The following simplifications apply:

$$I_E \cong I_C,$$

$$V_{BE} \cong \begin{cases} 0.2 \text{ for germanium} \\ 0.6 \text{ v for silicon} \end{cases},$$

$r_c = \infty$, $r_e = 0$, and $r_b = 0$ in the equivalent tee-circuit.

Except where specifically called out in the problem, I_{CBO} is neglected.

PROBLEM 4.25   In the circuit of Fig. 4.32, find V_o.

Solution: The potential at point A is $(260 \times 20)/(1740 + 260) = 2.6$ v. For a silicon transistor, $V_{BE} = 0.6$ v, so that the drop across the $1\text{K}\Omega$ resistor is 2 v. Since $I_E \cong 2 \text{ma} \cong I_C$,

$$V_o = V_{CC} - I_C R_L = 20 - 0.002(5000) = 10 \text{ v}.$$

PROBLEM 4.26   Referring to Fig. 4.33, estimate I_C.

Solution: Assume $I_{CBO} = 0$:

$$V_{EE} - 0.6 = (10,000 + 2,000)\,I_E - 10,000\,I_C,$$

$$I_C = \alpha\,I_E = 0.996\,I_E,$$

$$3.4 = 12,000\,I_E - 9960\,I_E = 2040\,I_E,$$

$$I_E = \frac{3.4}{2040} = 1.67\ \text{ma},$$

$$I_C = 1.67 \times 0.996 = 1.66\ \text{ma}.$$

PROBLEM 4.27 (a) For the circuit of Fig. 4.34a, when switch Sw is open, find I_C and V_o. (b) With Sw closed, find I_C and V_o.

Solution: (a) With the switch Sw open,

$$I_C = (1 + h_{FE})I_{CBO} = (101) \times 10 \times 10^{-6} \cong 1\ \text{ma},$$

$$V_o = 20\ \text{v} - I_C(1000) = 19\ \text{v}.$$

(b) With switch Sw closed, refer to Fig. 4.34b. At first, disregard I_{CBO}. This figure shows a simplified circuit for calculation. The equations for this circuit are

$$2.6 - 0.6 = 10,300\,I_B + 300\,I_C, \quad I_C = h_{FE}I_B.$$

Substituting for I_C,

$$2\ \text{v} = 10,300\,I_B + 30,000\,I_B = 40,300\,I_B, \quad I_B = 50\ \mu\text{a}, \quad I_C = 5\ \text{ma}.$$

Now include an additional I_C component due to I_{CBO}. Recall that

$$\frac{\Delta I_C}{\Delta I_{CBO}} = S.$$

Approximately $\Delta I_C = S\,\Delta I_{CBO}$.
The stability factor must be calculated:

$$S = \frac{R_E + R_B}{R_E + \dfrac{R_B}{\beta + 1}} = \frac{10,300}{300 + \dfrac{10,000}{100}} \cong 25.$$

Thus,

$$I_C\ (\text{due to } I_{CBO}) \cong 25 \times (10 \times 10^{-6}) = 0.25\ \text{ma}.$$

Therefore,

$$I_C\ (\text{total}) = 5\ \text{ma} + 0.25\ \text{ma} = 5.25\ \text{ma}$$

and

$$V_o = 20 - (5.25) = 14.75\ \text{v}.$$

PROBLEM 4.28 For the circuit of Fig. 4.35, $I_{CBO} = 10\ \mu\text{a}$, $h_{FE} = 100$. Estimate I_C and V_o.

Solution: Initially, neglect the leakage component. Replace the resistance divider bias circuit by its Thevenin's equivalent source:

$$V_{eq} = 30 \times \frac{45}{135} = 10\ \text{v},$$

$$R_{eq} = 90\ \text{K} \,\|\, 45\ \text{K}\Omega = 30\ \text{K}\Omega = R_B.$$

This bias circuit feeds the input impedance R_{in} of the transistor. Using the approximate formula (see Table 5.1), R_{in} is easily calculated:
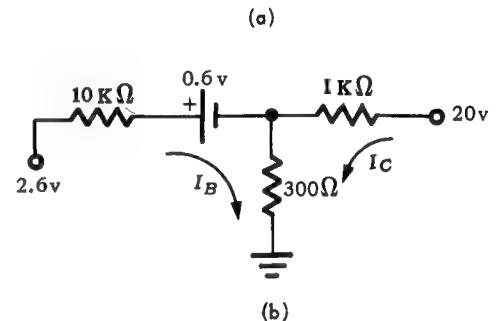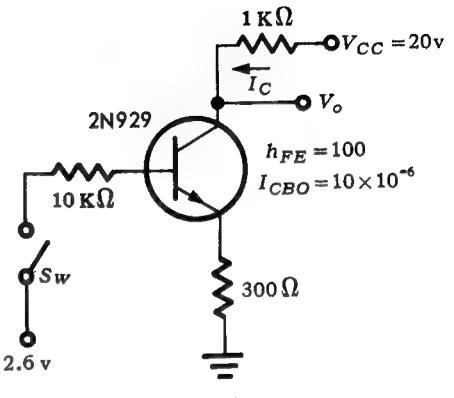
Fig. 4.34 Transistor bias circuit for Prob. 4.27.
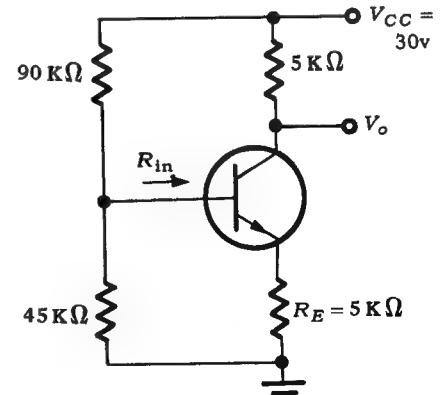
Fig. 4.35 Transistor bias circuit for Prob. 4.28.

$$R_{in} = R_E (1 + \beta_{DC}) = 5000 (1 + 100) \cong 500,000 \ \Omega.$$

At the base, the voltage is

$$10 \ \text{v} \times \frac{500,000}{530,000} = 9.45 \ \text{v}.$$

Since $V_{BE} \cong 0.6$ v,

$$V_E = 9.45 - 0.6 = 8.85 \ \text{v}$$

and

$$I_E = \frac{8.85}{5000} = 1.77 \ \text{ma} \cong I_C.$$

Now calculate the current component due to I_{CBO} by setting $R_1 = R_B$ and using the stability factor S derived in (4.38):

$$S = \frac{R_B + R_E}{\dfrac{R_B}{1 + \beta_{DC}} + R_E} = \frac{30 \ \text{K}\Omega + 5 \ \text{K}\Omega}{\dfrac{30 \ \text{K}\Omega}{101} + 5 \ \text{K}\Omega} \cong 7.$$

The current component due to leakage is $7 \times 10 = 70 \ \mu\text{a}$. Thus, the total collector current is

$$I_C = 1.77 + 0.07 = 1.84 \ \text{ma}$$

and

$$V_o = 30 - (1.84)(5) = 20.8 \ \text{v}.$$

PROBLEM 4.29 Referring to Fig. 4.36, determine the values of the resistors such that $I_C = 5$ ma, $V_{CE} = 8$ v, $V_E = 6$ v, and $S = 10$.

Solution: Use the previously discussed approximation techniques:

$$I_E \cong I_C = 5 \ \text{ma},$$

$$V_E = 6 \ \text{v},$$

$$R_E = \frac{6}{0.005} = 1,200 \ \Omega,$$

$$R_{in} \cong 240 \ \text{K}\Omega.$$

Using (4.38) for $S = 10$,

$$S = \frac{R_E + R_B}{R_E + \dfrac{R_B}{1 + h_{FE}}} = \frac{1200 + R_B}{1200 + \dfrac{R_B}{201}} = 10.$$

Solving, $R_B = 11,400 \ \Omega$. This must equal the equivalent source resistance of R_1 and R_2 in parallel:

$$R_{eq} = R_B = \frac{R_1 R_2}{R_1 + R_2} = 11,400.$$

Refer to the Thevenin equivalent circuit, Fig. 4.36b. Note that $V_A = 6.6$ v to account for the transistor base-emitter drop. Solving for V_{eq},

$$V_{eq} = \frac{6}{240,000} \ 11,400 + 6.6 \cong 0.9 \ \text{v}.$$
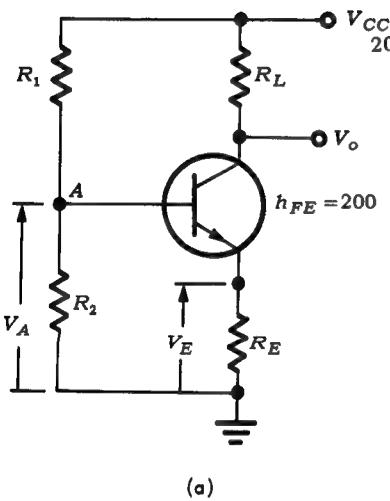
(a)
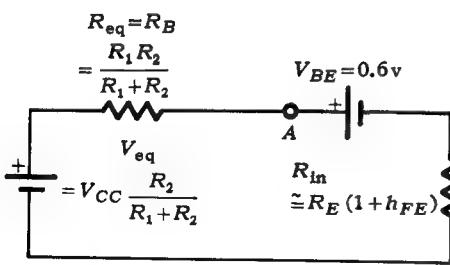
(b)

Fig. 4.36 Analysis of the transistor bias circuit of Prob. 4.29.

Equate this to the Thevenin expression for V_{eq}:

$$V_{eq} = \frac{R_2 \times 20}{R_1 + R_2} = 6.9 \text{ v.}$$

Combine with the previously developed expression for R_{eq}:

$$6.9 \, R_1 = 20 \, \frac{R_1 R_2}{R_1 + R_2} = 20 \, (11{,}400) = 228{,}800;$$

hence,

$$R_1 \cong \frac{228{,}800}{6.9} = 33{,}000 \, \Omega.$$

Substituting and solving for R_2,

$$R_2 \cong 17{,}400 \, \Omega.$$

For $V_{CE} = 8$ v, $V_o = 6 + 8 = 14$ v. The drop across R_L must equal 6 v at 5 ma, for $R_L = 1200 \, \Omega$.

PROBLEM 4.30 For the emitter-follower of Fig. 4.37a, what value resistors are required for a quiescent operating (Q) point of $I_C = 1$ ma, $V_{CE} = 10$ v, and $S = 5$?

Solution: If $V_{CE} = 10$ v, then $V_E = R_E I_E = 10$ v. Since $I_E = 1$ ma, $R_E = 10{,}000 \, \Omega$. Determine I_B from (4.2):

$$I_B = \frac{1}{\beta_{DC}} [I_C - (\beta_{DC} + 1) I_{CBO}] = \frac{1}{100} - \frac{101}{100} (0.005) \cong 0.005 \text{ ma.}$$

Refer to Fig. 4.37b. It is necessary to determine $R_B = R_{eq}$, which can be established from the approximate expression for S:

$$S = \frac{R_E + R_B}{R_E + \dfrac{R_B}{\beta_{DC} + 1}}.$$

Substitute $R_E = 10{,}000$, $\beta_{DC} = 100$, $S = 5$, and solve for R_B: $R_B = 42{,}000 \, \Omega$.
Referring again to Fig. 4.37b,

$$V_{eq} = 10.2 + R_B I_B = 10.2 + (42{,}000)(5 \times 10^{-6}) = 10.4 \text{ v.}$$

This leads to the following relationships:

$$\frac{R_2}{R_1 + R_2} = \frac{10.4}{20} = 0.52, \qquad \frac{R_1 R_2}{R_1 + R_2} = R_B = 42{,}000 \, \Omega.$$

Solving, $R_1 = 81{,}000 \, \Omega$ and $R_2 = 87{,}500 \, \Omega$.

PROBLEM 4.31 In the circuit of Fig. 4.38a, estimate the power dissipation in the transistor.

Solution: Referring to Fig. 4.38b, the equivalent bias network, it is seen that

$$I_B = \frac{9.4 \text{ v}}{0.5 \times 10^6 \, \Omega} = 18.8 \text{ } \mu\text{a,}$$

$$I_C = \beta_{DC} I_B + (\beta_{DC} + 1) I_{CBO}, \qquad [4.2]$$

$$I_C = 1.88 + 0.50 = 2.38 \text{ ma,}$$

$$V_o = V_{CC} - R_L I_C = 20 - (5000)(0.00238) = 8.1 \text{ v,}$$

$$V_{CE} = 8.1 \text{ v.}$$
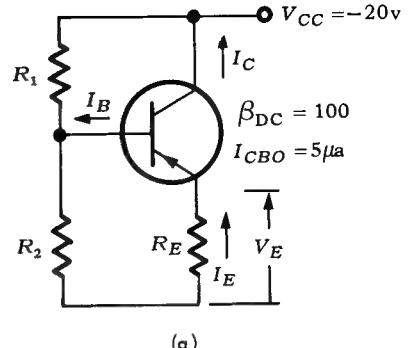
(a)
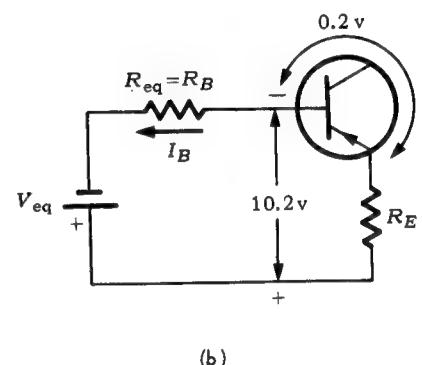
(b)

Fig. 4.37 Calculation of quiescent operating point by estimation.
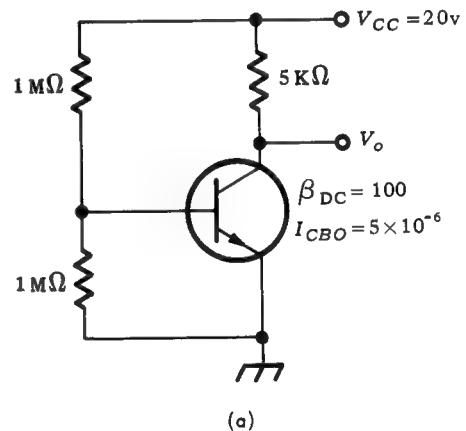
(a)
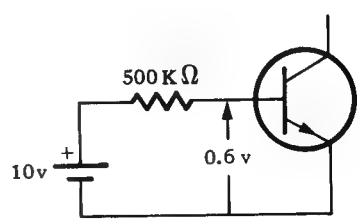
(b)

Fig. 4.38 Estimating power dissipation.

Therefore,

$$\text{Power dissipation} = I_C V_{CE}$$
$$= 0.00238 \times 8.1 \equiv 19.2 \text{ mw.}$$

PROBLEM 4.32   In Fig. 4.39, estimate I_C.

Solution: Since

$$I_E = \frac{10 - 0.6}{10,000} = 0.94 \text{ ma,}$$

the collector current is

$$I_C = 0.99 \, I_E + I_{CBO} = 0.93 + 0.1 = 1.03 \text{ ma.}$$

$\alpha = 0.99$

$I_{CBO} = 100 \, \mu a$
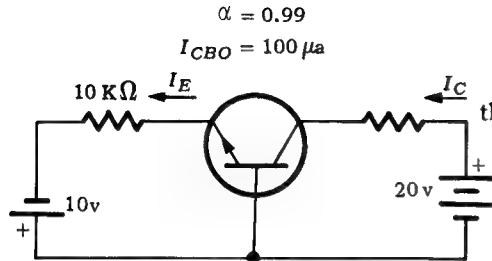
Fig. 4.39 Estimating collector current in a common-base circuit.

4.11 Supplementary Problems

PROBLEM 4.33   If $R_B = 100 \, \Omega$ in Fig. 4.10, does the current increase with temperature?

PROBLEM 4.34   Determine whether the stability factor should be large or small for best stability.

PROBLEM 4.35   Define the factors S, M, and N.

PROBLEM 4.36   In the circuit of Fig. 4.17, how can a reduction of gain at audio frequencies due to the resistor R_E be avoided?

PROBLEM 4.37   (a) Determine the effect on S of a large resistance in the base lead in the circuit of Fig. 4.17.   (b) What is the effect of a large resistance on stability?

PROBLEM 4.38   Does temperature effect V_{BE}?

PROBLEM 4.39   Determine if the static characteristics of a transistor vary with temperature.

PROBLEM 4.40   If $R_1 = 1800 \, \Omega$, $R_2 = 680 \, \Omega$, $R_L = 56 \, \Omega$, and $R_E = 68 \, \Omega$ in Fig. 4.17, find (a) S,   (b) I_C at 25°C and 70°C when $I_{CBO} = 1 \, \mu a$ at 25°C.

PROBLEM 4.41   Describe thermal run-away and its mechanism.

PROBLEM 4.42   In the circuit of Fig. 4.38a, estimate the power dissipation in the transistor when a 5-KΩ resistor is replaced with a 10-KΩ resistor.

SINGLE-STAGE AMPLIFIERS

5.1 Introduction

The performance of the *single-stage audio amplifier* will be calculated for *small-signal* conditions. It is assumed that bias voltages are set to establish a suitable operating point, and that the parameters corresponding to the operating point are known or available. The equivalent circuit techniques developed in Chap. 3 are directly applicable. Complete calculation procedures are presented for each of the basic transistor configurations, and a tabular summary of formulae is provided in Table 5.1 on p. 113.

The problem under investigation is defined in Fig. 5.1. A single-stage amplifier is energized by a small-signal a-c generator v_g with an internal resistance R_g. The load resistance is R_L. The items to be calculated are *input* and *output impedances*, and *voltage, current,* and *power gains*, the calculation of which leads to methods of achieving desired circuit performance features.
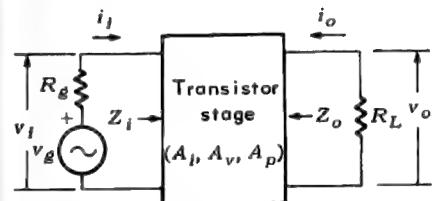
Fig. 5.1 Single-stage amplifier connected to input generator and output load resistance.

5.2 Common-Emitter Circuit

Figure 5.2 illustrates the common-emitter circuit adapted to the analysis of small a-c signals. Bias resistors are not included, since their effect on a-c performance is taken into account by combining them with the equivalent generator and load resistors, using conventional network theory. Also blocking capacitors are ignored, since it is assumed that their impedances are negligible at the a-c frequencies in question. Their effect on amplifier bandwidth will be considered later.

The a-c amplifier is most conveniently analyzed using the hybrid equivalent circuit discussed in Chap. 3. Note that for the common-emitter connection, $i_i = i_b$, and $i_o = i_c$.

PROBLEM 5.1 The *h*-parameter equivalent circuit of the common-emitter amplifier of Fig. 5.2 is shown in Fig. 5.3. Derive the following:

Z_i, Input impedance,*

Z_o, Output impedance,*

A_i, Current gain,

A_v, Voltage gain,

A_p, Power gain.

Solution: Set up the basic equations for the circuit of Fig. 5.3:

Fig. 5.2 Simplified common-emitter circuit for small-signal a-c analysis.

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* Since reactances are neglected at low- and mid-frequencies, we can also speak of *input* and *output resistances*.

$$v_g = i_i R_g + i_i h_{ie} + v_o h_{re}. \tag{5.1}$$

$$h_{fe} i_i = - v_o h_{oe} - \frac{v_o}{R_L}. \tag{5.2}$$

Solve (5.2) for output voltage, v_o:

$$v_o = - \frac{R_L h_{fe} i_i}{h_{oe} R_L + 1}. \tag{5.3}$$

Substitute this expression in (5.1) and simplify:

$$v_g = i_i \left(R_g + h_{ie} - \frac{R_L h_{fe} h_{re}}{1 + h_{oe} R_L} \right). \tag{5.4}$$

Since

$$v_g = i_i R_g + v_i,$$

from (5.4),

$$v_i = i_i \left(h_{ie} - \frac{R_L h_{fe} h_{re}}{1 + h_{oe} R_L} \right). \tag{5.5}$$

This expression gives Z_i directly:

$$Z_i = \frac{v_i}{i_i} = h_{ie} - \frac{R_L h_{fe} h_{re}}{1 + h_{oe} R_L}. \tag{5.6}$$

From Ohm's law,

$$i_o = \frac{- v_o}{R_L}.$$

The current gain is easily determined by substituting in (5.3) and simplifying:

$$A_i = \frac{i_o}{i_i} = \frac{\dfrac{- v_o}{R_L}}{i_i}$$

$$= \frac{h_{fe}}{1 + h_{oe} R_L}. \tag{5.7}$$

Voltage gain is determined by combining previous results with the following fundamental relationship:

$$A_v = \frac{v_o}{v_i} = \frac{- i_o}{i_i} \times \frac{R_L}{Z_i}$$

$$= \frac{- h_{fe}}{1 + R_L h_{oe}} \left(\frac{R_L}{h_{ie} - \dfrac{R_L h_{fe} h_{re}}{1 + h_{oe} R_L}} \right)$$

$$= \frac{- h_{fe} R_L}{h_{ie} (1 + h_{oe} R_L) - R_L h_{fe} h_{re}}. \tag{5.8}$$

It remains only to calculate output impedance, Z_o. This is done by short-circuiting v_g, and *applying* a voltage v_o across the output terminals. The current flow in the output circuit equals the applied voltage times the output resistance.

Refer to Fig. 5.4. The current i_o is determined from the equation

$$i_o = h_{fe} i_i + v_o h_{oe},$$

while i_i is determined from

$$v_o h_{re} = - i_i (h_{ie} + R_g).$$

Fig. 5.3 The *h*-parameter equivalent circuit for the common-emitter connection.

Fig. 5.4 Determining the small-signal output impedance of the common-emitter transistor circuit.

Combine these two equations, and solve for $Z_o = v_o/i_o$:

$$Z_o = \frac{v_o}{i_o} = \frac{1}{h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_g}}. \tag{5.9}$$

Power gain A_p is simply the product of voltage gain A_v and current gain A_i.

PROBLEM 5.2 Determine Z_i, Z_o, A_v, and A_i for a common-emitter amplifier using the 2N929 transistor, biased so that $I_c = 4$ ma and $V_{CE} = 12$ v. Assume $R_L = 5000\ \Omega$ and $R_g = 500\ \Omega$. Use the hybrid parameters for the above circuit derived in Chap. 3:

$$h_{ie} = 2200\ \Omega,$$

$$h_{re} = 2 \times 10^{-4},$$

$$h_{fe} = 290,$$

$$h_{oe} = 30 \times 10^{-6} \text{ mhos.}$$

Solution: Find Z_i by substituting in (5.6):

$$Z_i = h_{ie} - \frac{R_L\, h_{fe}\, h_{re}}{1 + h_{oe}\, R_L}$$

$$= 2200 - \frac{(5000)\,(290)\,(2 \times 10^{-4})}{1 + (30 \times 10^{-6})\,(5000)}$$

$$= 1950\ \Omega.$$

This impedance is not substantially different from h_{ie}.

Similarly, calculate Z_o by substituting in (5.9):

$$Z_o = \frac{1}{h_{oe} - \frac{h_{fe}\, h_{re}}{h_{ie} + R_g}}$$

$$= \frac{1}{30 \times 10^{-6} - \frac{(290)\,(2 \times 10^{-4})}{2200 + 500}}$$

$$= 118{,}000\ \Omega.$$

Voltage gain is given by

$$A_v = \frac{-h_{fe}\, R_L}{h_{ie}\,(1 + h_{oe}\, R_L) - R_L\, h_{fe}\, h_{re}}. \tag{5.8}$$

Substitute the given values:

$$A_v = \frac{-290 \times 5000}{2200\,(1 + 30 \times 10^{-6} \times 5000) - (5000)\,(290)\, 2 \times 10^{-4}}$$

$$= \frac{-290 \times 5000}{2200\,(1.15) - 290} = -647.$$

Current gain from (5.7) is

$$A_i = \frac{h_{fe}}{1 + h_{oe}\, R_L} = \frac{290}{1 + 30 \times 10^{-6} \times 5000} = 252.$$

PROBLEM 5.3 Describe qualitatively the effect a varying R_L has on the input impedance of a common-emitter circuit.

Solution: Refer to (5.6):

$$Z_i = h_{ie} - \frac{R_L h_{fe} h_{re}}{1 + h_{oe} R_L}.$$

[5.6]

For R_L very small (output short-circuited),

$$Z_i \cong h_{ie}.$$

(5.10)

For R_L very large,

$$Z_i \cong h_{ie} - \frac{h_{fe} h_{re}}{h_{oe}}.$$

(5.11)

The input impedance decreases between the limits of (5.10) and (5.11) as R_L increases.

PROBLEM 5.4   For the circuit conditions of Prob. 5.2, determine Z_i as R_L varies from 0 to ∞.

Solution: Substitute numerical values in (5.6) to determine Z_i vs. R_L:

$$Z_i = 2200 - \frac{580 \times 10^{-4} R_L}{1 + (30 \times 10^{-6}) R_L}.$$

Values have already been found in Probs. 5.2–3 for $R_L = 0$ and 5000 Ω. Now $R_L = 100,000$ Ω and 1 MΩ. Then for $R_L = 100,000$,

$$Z_i = 2200 - \frac{580 \times 10^{-4} \times 10^5}{1 + 3}$$

$$= 2200 - 1450 = 750 \ \Omega.$$

For $R_L = 1,000,000$,

$$Z_i = 2200 - \frac{580 \times 10^{-4} \times 10^6}{1 + 30}$$

$$= 2200 - 1870 = 330 \ \Omega.$$

At $R_L = \infty$, substitute in (5.11):

$$Z_i = 2200 - \frac{290 \times 2 \times 10^{-4}}{30 \times 10^{-6}} = 265 \ \Omega.$$

The values of input impedance vs. R_L determined thus far are tabulated below:

R_L, Ω	Z_i, Ω
0	2200
5000	1950
100,000	750
1,000,000	330
∞	265

Figure 5.5 shows Z_i vs. R_L plotted on semi-logarithmic coordinates, since this method provides the most convenient presentation over the complete wide range. For high β transistors, R_L is rarely above 10,000 Ω. Thus, for all practical purposes, Z_i will not vary significantly with R_L.

PROBLEM 5.5   For the circuit conditions of Prob. 5.2, determine Z_o for $R_g = 0$, 500 Ω, 10,000 Ω, and ∞.
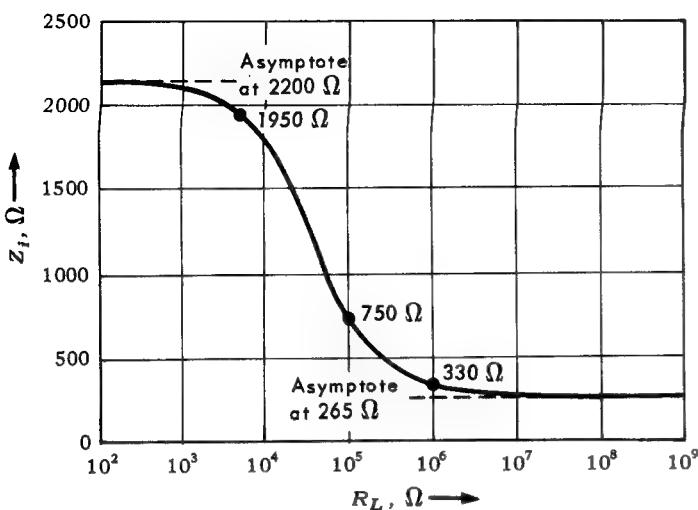
Fig. 5.5 Variation of input impedance with load resistance for a common-emitter circuit.
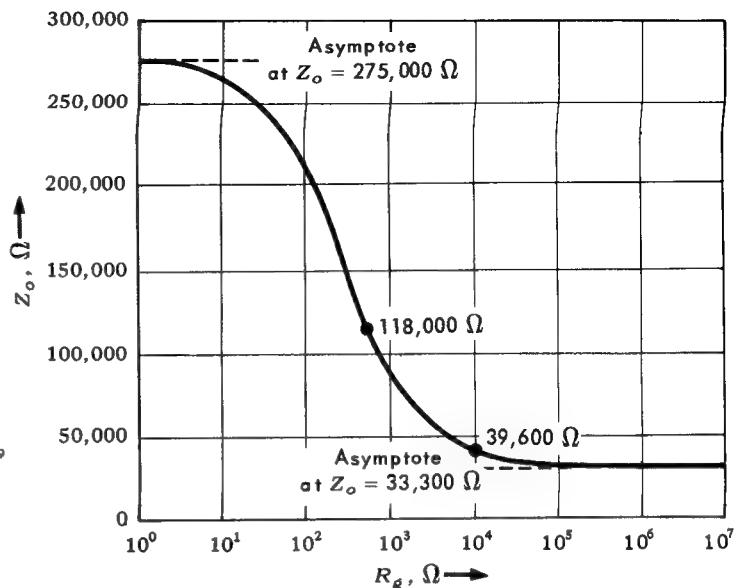
Fig. 5.6 Variation of output impedance with generator resistance for a common-emitter circuit.

Solution: Use (5.9) which was previously derived for output impedance:

$$Z_o = \cfrac{1}{h_{oe} - \cfrac{h_{fe} h_{re}}{h_{ie} + R_g}} = \cfrac{1}{30 \times 10^{-6} - \cfrac{290 \times 2 \times 10^{-4}}{2200 + R_g}}.$$

It is easy to determine Z_o for the extreme values of $R_g = 0$ and ∞. At $R_g = 0$,

$$Z_o = \cfrac{1}{30 \times 10^{-6} - \cfrac{580}{22} \times 10^{-6}} = 275,000 \ \Omega.$$

At $R_g = \infty$,

$$Z_o = \frac{1}{30 \times 10^{-6}} = 33,300 \ \Omega.$$

Now substitute $R_g = 500 \ \Omega$:

$$Z_o = \cfrac{1}{30 \times 10^{-6} - \cfrac{580 \times 10^{-4}}{2700}} = 118,000 \ \Omega.$$

For $R_g = 10,000 \ \Omega$,

$$Z_o = \cfrac{1}{30 \times 10^{-6} - \cfrac{580 \times 10^{-4}}{12,200}} = 39,600 \ \Omega.$$

Tabulate the values determined thus far:

R_g, Ω	Z_o, Ω
0	275,000
500	118,000
10,000	39,600
∞	33,300

Output impedance Z_o vs. R_g is sketched on Fig. 5.6.

PROBLEM 5.6 For the circuit conditions of Prob. 5.2, determine A_i and A_v for $R_L = 0$, $100\ \Omega$, $1000\ \Omega$, $10^4\ \Omega$, $10^5\ \Omega$, $10^6\ \Omega$, and ∞.

Solution: Substitute the hybrid parameters of Prob. 5.2 in (5.7) and (5.8):

$$A_i = \frac{h_{fe}}{1 + h_{oe}\,R_L}$$

$$= \frac{290}{1 + 30 \times 10^{-6}\,R_L},$$

$$A_v = \frac{-h_{fe}\,R_L}{h_{ie}\,(1 + h_{oe}\,R_L) - R_L\,h_{fe}\,h_{re}}$$

$$= \frac{-290\,R_L}{2200\,(1 + 30 \times 10^{-6}\,R_L) - 290 \times 2 \times 10^{-4}\,R_L}$$

$$= \frac{-290\,R_L}{2200 + 0.008\,R_L}$$

$$= \frac{-0.132\,R_L}{1 + 3.64 \times 10^{-6}\,R_L}.$$

The values of gain, as determined by direct numerical substitution of values of R_L, are listed below. Although not indicated, A_v is negative in all cases.

R_L, Ω	A_i	A_v
0	290	0
100	289	13.2
1000	282	131
10,000	223	1272
100,000	72.5	9670
1,000,000	9.36	28,400
∞	0	36,200

For the normally used values of R_L (under around 10,000 Ω), current gain is relatively constant, while voltage gain is about proportional to R_L. The change in voltage gain is largely due to the changing impedance of R_L for a constant input current. The circuit is best described as a *current* amplifier, rather than a *voltage* amplifier.

If a resistance R_E is added to the emitter circuit (see Fig. 5.7a), input impedance is increased substantially, but the resistor is not by-passed. This circuit is most conveniently studied using the tee-equivalent circuit of Fig. 5.7b.

(a)

(b)
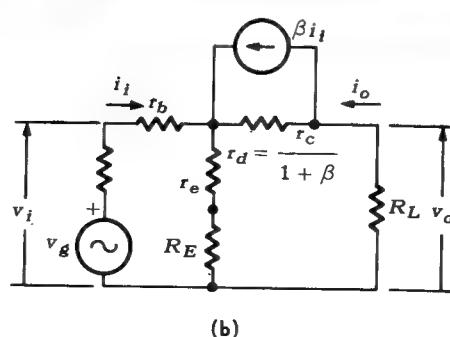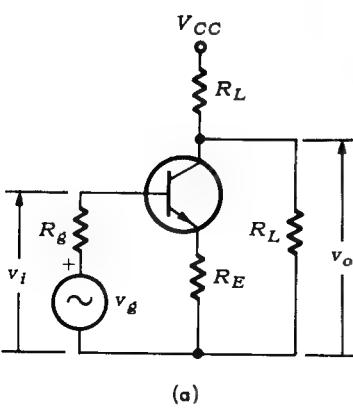
Fig. 5.7 (a) Common-emitter circuit with feedback resistor in the emitter circuit. (b) Tee-equivalent circuit of (a).
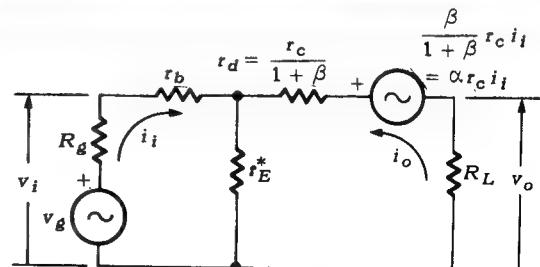
Fig. 5.8 Common-emitter circuit with total resistance r_E^* in the emitter circuit. The usual parallel current source in the collector circuit is replaced by a series voltage source to simplify calculations. [See Fig. 5.7(b).]

PROBLEM 5.7 A resistor R_E is inserted in the emitter circuit of the common-emitter amplifier analyzed in the previous problems. Calculate, for this modified common-emitter circuit, the following performance parameters:

Z_i, Input impedance,

Z_o, Output impedance,

A_i, Current gain,

A_v, Voltage gain.

Solution: The tee-equivalent circuit is shown in Figs. 5.7b and 5.8. In Fig. 5.8, set $r_E^* = r_e + R_E$, and replace the parallel current source in the collector circuit of Fig. 5.7b with a more convenient series voltage source. The use of the tee-equivalent circuit provides convenient formulas in terms of tee-parameters, which are then available for other applications.

The basic circuit equations applicable to Fig. 5.8 are

$$v_g = (R_g + r_b + r_E^*) i_i + r_E^* i_o.$$

$$\alpha r_c i_i = r_E^* i_i + \left(R_L + \frac{r_c}{1 + \beta} + r_E^* \right) i_o.$$

Rearranging these equations and letting $1/(1 + \beta) = 1 - \alpha$,

$$v_g = (R_g + r_b + r_E^*) i_i + r_E^* i_o. \tag{5.12}$$

$$0 = (r_E^* - \alpha r_c) i_i + [R_L + r_c (1 - \alpha) + r_E^*] i_o. \tag{5.13}$$

Solving these equations for i_i and i_o, using determinants.

$$i_i = \frac{1}{\Delta} \begin{vmatrix} v_g & r_E^* \\ 0 & [R_L + r_c (1 - \alpha) + r_E^*] \end{vmatrix} = \frac{v_g [R_L + r_c (1 - \alpha) + r_E^*]}{\Delta}.$$

$$i_o = \frac{1}{\Delta} \begin{vmatrix} (R_g + r_b + r_E^*) & v_g \\ r_E^* - \alpha r_c & 0 \end{vmatrix} = \frac{- v_g (r_E^* - \alpha r_c)}{\Delta}.$$

where

Δ = determinant of system

$$= \begin{vmatrix} R_g + r_b + r_E^* & r_E^* \\ r_E^* - \alpha r_c & R_L + r_c (1 - \alpha) + r_E^* \end{vmatrix}$$

$$= (R_g + r_b + r_E^*) [R_L + r_c (1 - \alpha) + r_E^*] - r_E^* (r_E^* - \alpha r_c). \tag{5.14}$$

Current gain is immediately determined from the ratio of i_o to i_i:

$$A_i = \frac{i_o}{i_i} = \frac{- (r_E^* - \alpha r_c)}{R_L + r_c (1 + \alpha) + r_E^*} = \frac{\alpha r_c - r_E^*}{R_L + r_c (1 - \alpha) + r_E^*}. \tag{5.15}$$

This last expression can be simplified, recalling that $r_d = r_c/(1 + \beta) = r_c (1 - \alpha)$ is much greater than r_E^*. Thus,

$$A_i \cong \frac{\dfrac{\alpha}{1 - \alpha}}{\dfrac{R_L}{r_c (1 - \alpha)} + 1} = \frac{\beta}{1 + \dfrac{R_L}{r_d}}. \tag{5.16}$$

To find the input impedance Z_i, for the moment substitute v_i for v_g and let $R_g = 0$ in (5.12). Then solve for i_i, using (5.14) for the system determinant Δ:

$$i_i = \frac{v_i [R_L + r_c (1 - \alpha) + r_E^*]}{\Delta},$$

$$Z_i = \frac{v_i}{i_i} = \frac{(r_b + r_E^*)[R_L + r_c(1-\alpha) + r_E^*] - r_E^*(r_E^* - \alpha r_o)}{R_L + r_c(1-\alpha) + r_E^*}$$

$$= r_b + r_E^* - \frac{r_E^*(r_E^* - \alpha r_o)}{R_L + r_c(1-\alpha) + r_E^*}$$

$$= r_b + r_E^* \left[1 - \frac{r_E^* - \alpha r_o}{R_L + r_c(1-\alpha) + r_E^*} \right]$$

$$= r_b + r_E^* \left[\frac{R_L + r_c - \alpha r_o + r_E^* - r_E^* + \alpha r_o}{R_L + r_c(1-\alpha) + r_E^*} \right]$$

$$= r_b + r_E^* \left[\frac{R_L + r_c}{R_L + r_c(1-\alpha) + r_E^*} \right] \tag{5.17a}$$

$$= r_b + r_E^*(1+\beta) \frac{1 + \dfrac{R_L}{r_d(1+\beta)}}{1 + \dfrac{R_L + r_E^*}{r_d}} . \tag{5.17b}$$

Since $R_L + r_E^* \ll r_c(1-\alpha)$, and $1/(1-\alpha) = 1 + \beta$.

$$Z_i \cong r_b + r_E^*(1+\beta). \tag{5.18}$$

It is now easy to find voltage gain, A_v:

$$A_v = \frac{v_o}{v_i} = \frac{-i_o}{i_i} \frac{R_L}{Z_i} = -A_i \frac{R_L}{Z_i} .$$

Substitute (5.15) and (5.17) for A_i and Z_i, respectively:

$$A_v = \frac{\alpha r_c - r_E^*}{R_L + r_c(1-\alpha) + r_E^*} \times \frac{-R_L}{r_b + r_E^* \left[\dfrac{R_L + r_c}{R_L + r_c(1-\alpha) + r_E^*} \right]}$$

$$= \frac{-(\alpha r_c - r_E^*)R_L}{r_b[R_L + r_c(1-\alpha) + r_E^*] + r_E^*(R_L + r_c)}$$

$$= -\frac{\dfrac{R_L}{r_E^*}\left(\alpha - \dfrac{r_E^*}{r_o}\right)}{1 + \dfrac{R_L}{r_c} + \dfrac{r_b}{r_E^*}\left[(1-\alpha) + \left(\dfrac{r_E^* + R_L}{r_c}\right)\right]} . \tag{5.19a}$$

In terms of the appropriate equivalent tee-parameters,

$$A_v = -\frac{\dfrac{R_L}{r_E^*}\left[\dfrac{\beta}{\beta+1} - \dfrac{r_E^*}{r_d(\beta+1)} \right]}{\dfrac{r_b}{r_E^*}\left[\dfrac{1}{\beta+1} + \dfrac{r_E^* + R_L}{r_d(\beta+1)} \right] + 1 + \dfrac{R_L}{r_d(\beta+1)}} . \tag{5.19b}$$

Using the usual approximations in (5.19),

$$A_v \cong -\frac{R_L}{r_E^*}. \tag{5.19c}$$

The error in this approximation is estimated in Prob. 5.8.

The last formula to be derived is an expression for output impedance. Set up the original equations (5.12) and (5.13) with $v_g = 0$, and R_L replaced by a voltage v_o applied to the output terminals:

$$0 = (R_g + r_b + r_E^*)i_i + r_E^* i_o . \tag{5.20}$$

$$v_o = (r_E^* - \alpha\, r_c)\, i_i + [r_c\, (1 - \alpha) + r_E^*]\, i_o. \qquad (5.21)$$

Solve (5.20) for i_i:

$$i_i = \frac{-r_E^*\, i_o}{R_g + r_b + r_E^*}. \qquad (5.22)$$

Substitute (5.22) in (5.21), and solve for $Z_o = v_o/i_o$:

$$Z_o = \frac{v_o}{i_o} = \frac{(\alpha\, r_c - r_E^*)\, r_E^*}{R_g + r_b + r_E^*} + r_c\,(1 - \alpha) + r_E^*$$

$$= r_d + r_E^* + \frac{(\beta\, r_d - r_E^*)\, r_E^*}{R_g + r_b + r_E^*}$$

$$= r_d \left[1 + \frac{r_E^*}{r_d} + \frac{\beta - \dfrac{r_E^*}{r_d}}{1 + \dfrac{R_g + r_b}{r_E^*}} \right].$$

For $r_E^*/r_d \ll 1$,

$$Z_o \approx r_d \left[1 + \frac{\beta}{1 + \dfrac{R_g + r_b}{r_E^*}} \right]. \qquad (5.23)$$

PROBLEM 5.8 Check the approximate formula (5.19c) against the exact formula (5.19a) for the voltage gain of the common-emitter amplifier with resistance R_E in the emitter circuit. Use the 2N929 transistor at the previously defined operating point, with the following parameters:

$$r_e = 6.6 \ \Omega\,,$$

$$r_b = 260 \ \Omega,$$

$$r_d = 34.5 \ \text{k}\,\Omega,$$

$$\beta = 290 \ \text{for} \ R_L = 5000 \ \Omega,$$

$$r_E^* = 100 \ \Omega,$$

$$\alpha = 0.9966\,,$$

$$r_c = 10^7.$$

Solution: In the exact formula, $-R_L/r_E^*$ is multiplied by the following factor:

$$\frac{0.966 - \dfrac{100}{10^7}}{1 + \dfrac{5000}{10^7} + \dfrac{260}{100}\left(\dfrac{1}{291} + \dfrac{5100}{10^7}\right)} = 0.986.$$

The approximate formula, $A_v = -R_L/r_E^*$, is inaccurate by only 1.4%. Thus, an unby-passed emitter resistor provides excellent stabilization of voltage gain. This is a special type of feedback which will be described in more detail in Chap. 8.

PROBLEM 5.9 Calculate Z_i, Z_o, A_v, and A_i for the circuit of Fig. 5.9. Assume that bias is set so that $I_C = 4$ ma and $V_{CE} = 12$ v, corresponding to the operating point of the previous problem.

Solution: For the operating point of this circuit, the 2N929 transistor has the following tee-parameters:
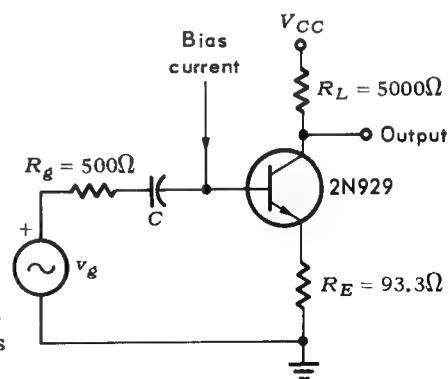
Fig. 5.9 Single-stage transistor amplifier with an emitter resistor for stabilization.

$$r_e = 6.6\ \Omega\,,$$

$$R_E = 93.4\ \Omega\,,$$

$$r_E^* = r_e + R_E = 100\ \Omega\,,$$

$$r_c = 10\ \text{meg}\,,$$

$$r_b = 260\ \Omega\,,$$

$$\alpha = 0.9966\,,$$

$$\beta \approx 290.$$

These parameters are substituted directly in the appropriate formulae to calculate the required performance characteristics:

$$A_v = \frac{-R_L}{r_b\left(\dfrac{1}{\beta} + \dfrac{r_E^* + R_L}{r_c}\right) + r_E^*}$$

$$= \frac{-5000}{260\left(\dfrac{1}{290} + \dfrac{5100}{10^7}\right) + 100} = -49.$$

This is just 2% less than the approximate value of $R_L/r_E^* = 50$.
  Calculate input impedance:

$$Z_i = r_b + r_E^*\,(1 + \beta)\,\frac{1 + \dfrac{R_L}{r_d\,(1 + \beta)}}{1 + \dfrac{R_L + r_E^*}{r_d}}$$

$$= 260 + 100\,(291)\,\frac{1 + 5 \times 10^{-4}}{1 + \dfrac{5100}{3.45 \times 10^4}} = 25{,}660\ \Omega\,.$$

Note that the significant component of input impedance is the $r_E^*\,(1 + \beta)$ term, which in itself gives a fair approximation. Compare the input impedance with the much lower value of 1950 Ω in Prob. 5.2 for the same circuit, but with $R_E = 0$.
  Now determine output impedance:

$$Z_o \cong r_d\left(1 + \frac{\beta}{1 + \dfrac{R_g + r_b}{r_E^*}}\right)$$

$$= 34{,}500\left(1 + \frac{290}{1 + \dfrac{760}{100}}\right) = 1.2\ \text{M}\Omega\,.$$

It remains only to calculate current gain:

$$A_i = \frac{\beta}{1 + \dfrac{R_L + r_E^*}{r_d}}$$

$$= \frac{290}{1 + \dfrac{5100}{34{,}500}} = 251.$$

PROBLEM 5.10 By comparing the results of calculations on the circuits of Fig. 5.9 (Prob. 5.8) and Fig. 5.2 (Prob. 5.2) differing only in the presence of R_E in Fig. 5.9, comment on the effect of R_E on the principal amplifier characteristics.

Solution: The amplifier characteristics are summarized in the following tabulation:

	Fig. 5.2	Fig. 5.9
Z_i	1950 Ω	25,660 Ω
Z_o	118,000 Ω	1.2×10^6 Ω
A_i	252	251
A_v	-647	-49

The addition of R_E increases the input impedance to nearly $r_E^* (\beta + 1)$, reduces voltage gain to about R_L/r_E^*, and increases output impedance substantially. Current gain is essentially unchanged. The performance of the amplifier is stabilized since voltage gain becomes nearly independent of β.

5.3 Common-Base Circuit

The performance parameters of the common-base circuit, namely *input* and *output impedances*, and *current* and *voltage gains*, are derived in a similar manner to the derivation of the common-emitter parameters of the preceding section. Using the hybrid equivalent circuit, Figs. 5.1 and 5.3 apply exactly, except that the subscript *b* (common-base) is used instead of the subscript *e* (common-emitter).

PROBLEM 5.11 Derive formulas for Z_i, Z_o, A_i, and A_v for the common-base amplifier circuit.

Solution: Modifying the previously derived common-emitter equations (5.6), (5.9), (5.7), and (5.8) where the subscript *b* is used instead of *e*,

$$Z_i = h_{ib} - \frac{R_L h_{fb} h_{rb}}{1 + h_{ob} R_L} = h_{ib} - \frac{h_{fb} h_{rb}}{h_{ob} + \dfrac{1}{R_L}}, \tag{5.24}$$

$$Z_o = \frac{1}{h_{ob} - \dfrac{h_{fb} h_{rb}}{h_{ib} + R_s}}, \tag{5.25}$$

$$A_i = \frac{h_{fb}}{1 + h_{ob} R_L}, \tag{5.26}$$

$$A_v = \frac{-h_{fb} R_L}{h_{ib}(1 + h_{ob} R_L) - R_L h_{fb} h_{rb}}. \tag{5.27}$$

PROBLEM 5.12 A 2N929 transistor is operated in the common-base configuration at a bias point where $V_{CB} = 12$ v and $I_C = 4$ ma. For $R_s = 10$ Ω and $R_L = 5$ KΩ, calculate (a) Z_i, (b) Z_o, (c) A_v, and (d) A_i. The h-parameters for this operating point have already been derived in Chap. 3:

$$h_{ib} = 7.57 \ \Omega,$$

$$h_{rb} = 0.27 \times 10^{-4},$$

$$h_{fb} = -0.996,$$

$$h_{ob} = 0.103 \times 10^{-6} \text{ mhos}.$$

(a) Z_i vs. load resistance

(b) Z_o vs. R_g
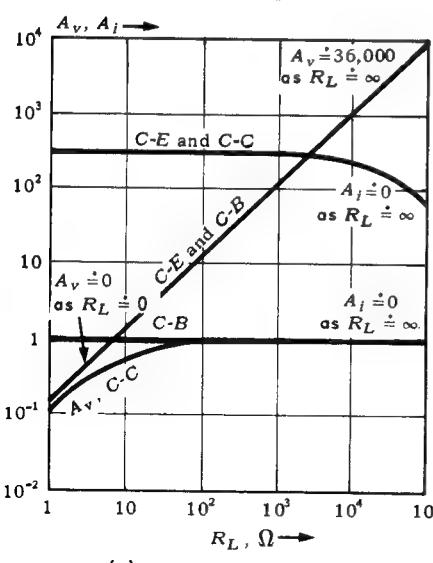
(c) A_i and A_v vs. R_L

Fig. 5.10 Typical performance characteristics of single-stage audio amplifier.

Solution: (a) To determine input impedance, substitute the above parameters in (5.24):

$$Z_i = h_{ib} - \frac{h_{fb} \, h_{rb}}{h_{ob} + \dfrac{1}{R_L}} = 7.57 + \frac{0.996 \times 0.27 \times 10^{-4}}{2 \times 10^{-4} + 0.001 \times 10^{-4}} = 7.7 \; \Omega.$$

(b) Similarly, calculate Z_o by substituting in (5.25):

$$Z_o = \frac{1}{h_{ob} - \dfrac{h_{fb} \, h_{rb}}{h_{ib} + R_g}} = \frac{1}{0.103 \times 10^{-6} + \dfrac{(0.996)(0.27 \times 10^{-4})}{7.57 + 10}}$$

$$= 614{,}000 \; \Omega.$$

(c) Substituting in (5.27),

$$A_v = 639 \; \text{(voltage gain)}.$$

(d) Substituting in (5.26),

$$A_i = -0.996 \; \text{(current gain)}.$$

PROBLEM 5.13 For the 2N929 transistor of Prob. 5.12 with the same operating point and parameters, calculate and plot Z_i as R_L varies from 0 to ∞.

Solution: Use (5.24):

$$Z_i = h_{ib} - \frac{h_{fb} \, h_{rb}}{h_{ob} + \dfrac{1}{R_L}}.$$

The general nature of the input impedance variation is self-evident from this equation. Letting $R_L = 0$, $1/R_L$ becomes infinite, so that the second term in (5.24) vanishes, and

$$Z_i = h_{ib}.$$

Similarly, when $R_L = \infty$,

$$Z_i = h_{ib} - \frac{h_{fb} \, h_{rb}}{h_{ob}},$$

and when $1/R_L = h_{ob}$,

$$Z_i = h_{ib} - \frac{h_{fb} \, h_{rb}}{2 h_{ob}}.$$

This last impedance value is the average of the values for $R_L = 0$ and $R_L = \infty$. The $R_L \cong 0$ and $R_L \cong \infty$ conditions define asymptotes, which make it an easy matter to sketch curves showing how Z_i varies with R_L.

Substituting numerical values of the common-base h-parameters,

$$Z_i = 7.57 + \frac{0.996 (0.27 \times 10^{-4})}{1.03 \times 10^{-7} + \dfrac{1}{R_L}}.$$

Figure 5.10 shows a plot on logarithmic coordinates of Z_i vs. R_L. Note that R_L has minor influence on Z_i, until it exceeds about 100 KΩ. Since such high values are usually not practical, $Z_i \cong h_{ib}$ is a constant value in this common-base connection. For the tee-equivalent circuit, $Z_i \cong r_e + r_b (1 - \alpha)$.

PROBLEM 5.14 For the common-base connection and the operating point of Prob. 5.12, determine the variation of Z_o vs. R_g.

Solution: Use the common-base *h*-parameters of Prob. 5.12:

$$Z_o = \frac{1}{h_{ob} - \dfrac{h_{fb} h_{rb}}{h_{ib} + R_g}}. \qquad [5.25]$$

As an aid to plotting, determine the limiting values where $R_g = 0$ and $R_g = \infty$. At $R_g = 0$,

$$Z_o = \frac{1}{h_{ob} - \dfrac{h_{fb} h_{rb}}{h_{ib}}}.$$

At $R_g = \infty$.

$$Z_o = \frac{1}{h_{ob}}.$$

Substitute numerical values:

$$Z_o = \frac{1}{0.103 \times 10^{-6} - \left(\dfrac{-0.996 \times 0.27 \times 10^{-4}}{7.57 + R_g} \right)},$$

and Z_o is plotted vs. R_g on Fig. 5.10. (Note that at $R_g \doteq \infty$, $Z_o \doteq r_c$ of the tee-equivalent circuit.)

Although Z_o varies sharply with R_g in the useful region where R_g is of the same order as h_{ib}, Z_o generally is not critical in circuit calculations. Thus the variation shown typically in Fig. 5.10 is not too troublesome.

PROBLEM 5.15 For the common-base connection and the operating point of Prob. 5.12, determine the variations in A_v and A_i vs. R_L.

Solution: Use the same common-base *h*-parameters of Prob. 5.12:

$$A_i = \frac{h_{fb}}{1 + h_{ob} R_L}$$

$$= \frac{-0.996}{1 + 1.03 \times 10^{-7} R_L},$$

$$A_v = \frac{-h_{fb}}{\dfrac{h_{ib}}{R_L} + h_{ib} h_{ob} - h_{fb} h_{rb}}$$

$$= \frac{0.996}{\dfrac{7.57}{R_L} + 7.57 (1.03 \times 10^{-7}) + 0.996 (0.27 \times 10^{-4})}.$$

Current and voltage gains are plotted in Fig. 5.10. Note that current gain is almost independent of R_L. Voltage gain, on the other hand, is very much a function of load, as might be expected.

5.4 Common-Collector Circuit (Emitter-Follower)

Proceeding as in the previous section, formulae for the common-collector single-stage amplifier configuration (emitter-follower) are derived simply by applying suitable subscripts to the hybrid parameters.

PROBLEM 5.16 Using the methods of Prob. 5.11, develop formulas for Z_o, Z_i, A_i, and A_v for the common-collector configuration.

Solution: It is only necessary to change the subscripts of the h-parameters as indicated below:

$$Z_i = h_{ic} - \frac{h_{ic} h_{rc}}{h_{oc} + \frac{1}{R_L}}, \tag{5.28}$$

$$Z_o = \frac{1}{h_{oc} - \frac{h_{ic} h_{rc}}{h_{ic} + R_g}}, \tag{5.29}$$

$$A_i = \frac{h_{ic}}{1 + h_{oc} R_L}, \tag{5.30}$$

$$A_v = \frac{-h_{ic} R_L}{h_{ic}(1 + h_{oc} R_L) - R_L h_{ic} h_{rc}}. \tag{5.31}$$

PROBLEM 5.17 Using the h-parameter formulae for the common-collector connection, determine Z_i as a function of R_L. Use the same operating point as in Prob. 5.12, and the corresponding numerical value of the h-parameters developed in Chap. 3:

$$h_{ic} = 2200 \ \Omega,$$

$$h_{rc} = 0.9999,$$

$$h_{ic} = -291,$$

$$h_{oc} = 30 \times 10^{-6} \ \text{mhos}.$$

Solution: Substituting the given values in (5.28),

$$Z_i = 2200 - \frac{(-291)(0.9999)}{30 \times 10^{-6} + \frac{1}{R_L}}.$$

Note that the asymptotes for $R_L = 0$ and $R_L = \infty$ described in Prob. 5.13 apply here, and are important plotting aids.

At $R_L = 0$,

$$Z_i = 2200 = h_{ic}.$$

At $R_L = \infty$,

$$Z_i = 2200 + \frac{291}{30 \times 10^{-6}} = 9.7 \ \text{M}\Omega.$$

Substituting additional values for R_L and calculating Z_i, the required variation of Z_i with R_L is derived (see Fig. 5.10).

For the practical range of R_L, the expression for Z_i may be simplified:

$$Z_i = h_{ic} - h_{ic} R_L.$$

In terms of other familiar units,

$$Z_i \cong h_{ie} + (\beta + 1) R_L,$$

since $h_{ic} \cong h_{ie}$ and $h_{ic} \cong -(1 + \beta)$.

Input impedance obviously depends almost directly on R_L in the useful range of operation. From the tee-equivalent circuit, $Z_i \cong h_{ic} - h_{fc}/h_{oc}$ and $Z_i \cong r_c$ as $R_L \doteq \infty$. Therefore, r_c constitutes a theoretical upper limit to input impedance.

PROBLEM 5.18 Proceeding as in Prob. 5.17, and using the same operating point and equivalent h-parameters, determine Z_o as a function of R_g.

Solution: The applicable formula is

$$Z_o = \frac{1}{h_{oc} - \dfrac{h_{ic} h_{rc}}{h_{ic} + R_g}}. \qquad [5.29]$$

Substituting numerical values and locating the $R_g \doteq \infty$ asymptote, Z_o is conveniently plotted in Fig. 5.10. A good practical approximation to Z_o is

$$Z_o \cong -\frac{R_g + h_{ic}}{h_{fc}}$$

or

$$Z_o \cong \frac{R_g + h_{ic}}{1 + \beta};$$

Z_o can never exceed r_e of the tee-equivalent circuit and depends strongly on R_g in the normal range of application.

PROBLEM 5.19 Proceeding as in Prob. 5.17, and using the same operating point and equivalent h-parameters, determine A_v as a function of R_L.

Solution: The applicable formula is

$$A_v = \frac{-h_{fc} R_L}{h_{ic}(1 + h_{oc} R_L) - R_L h_{fc} h_{rc}}. \qquad [5.31]$$

Rewrite this expression:

$$A_v = \frac{1}{h_{rc} - \dfrac{h_{ic}}{h_{fc}}\left(h_{oc} + \dfrac{1}{R_L}\right)}.$$

Since h_{rc} is the major term of the denominator, its more accurate value is required:

$$h_{rc} = 1 - h_{re}$$

(see Fig. 3.26c). Substituting,

$$A_v = \frac{1}{1 - h_{re} - \dfrac{h_{ic}}{h_{fc}}(h_{oc}) - \dfrac{h_{ic}}{h_{fc} R_L}}.$$

Using the h-parameters for the common-collector circuit, and $h_{re} = 2 \times 10^{-4}$,

$$A_v = \frac{1}{1 - 2 \times 10^{-4} + \dfrac{(30 \times 10^{-6})(2200)}{291} + \dfrac{2200}{291 R_L}} = \frac{1}{1.00002 + \dfrac{7.57}{R_L}}.$$

Observe that for $R_L \gg h_{ic}/h_{fc} = h_{ib}$, $A_v \cong 1$. As a matter of fact, the gain is very nearly unity over a wide and practical range of values of R_L. It is therefore convenient to calculate the *percent deviation from unity* for values of gain approximately equal to unity:

$$\text{Percent deviation} = (1 - A_v) \times 100.$$

Percent deviation from unity is plotted in Fig. 5.11 as R_L varies from 0 to ∞. Note that when R_L exceeds 100 h_{ib}, the deviation is less than 1%. This uniformity of gain of the common-collector or *emitter-follower* circuit is of great practical value. More will be said of this later.

PROBLEM 5.20　Proceeding as in Prob. 5.17, and using the same operating point and equivalent h-parameters, determine A_i as a function of R_L.

Solution:　The applicable formula is

$$A_i = \frac{h_{fc}}{1 + h_{oc} R_L}. \qquad [5.30]$$

Substituting numerical values,

$$A_i = \frac{h_{fc}}{1 + h_{oc} R_L} = \frac{-291}{1 + 30 \times 10^{-6} R_L}.$$

Figure 5.12 shows A_i vs. R_L, as required.
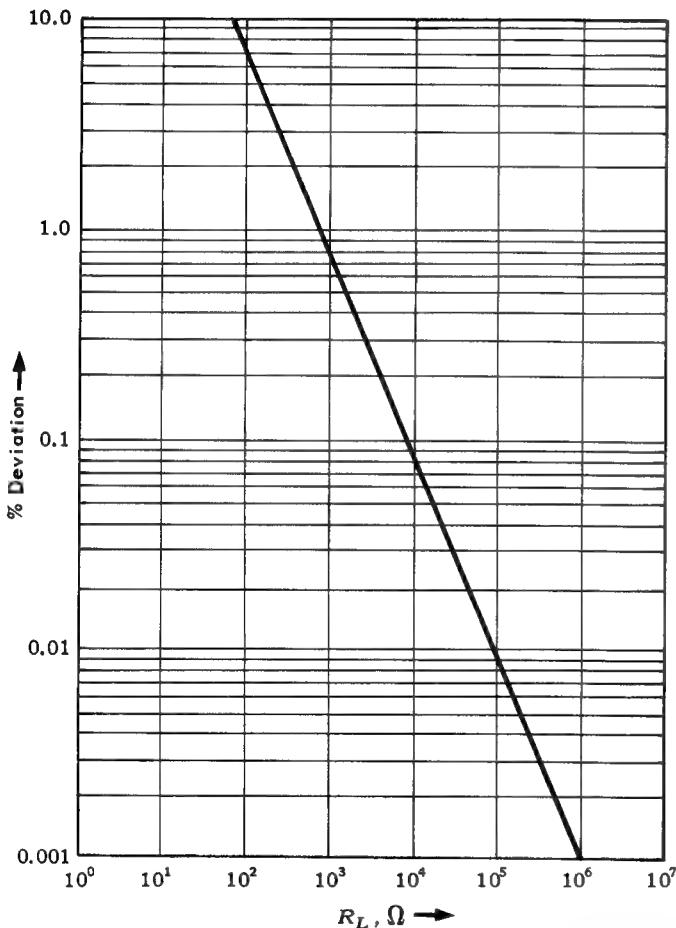
Fig. 5.11　Deviation from unity of voltage gain of common-collector amplifier with load resistor R_L.
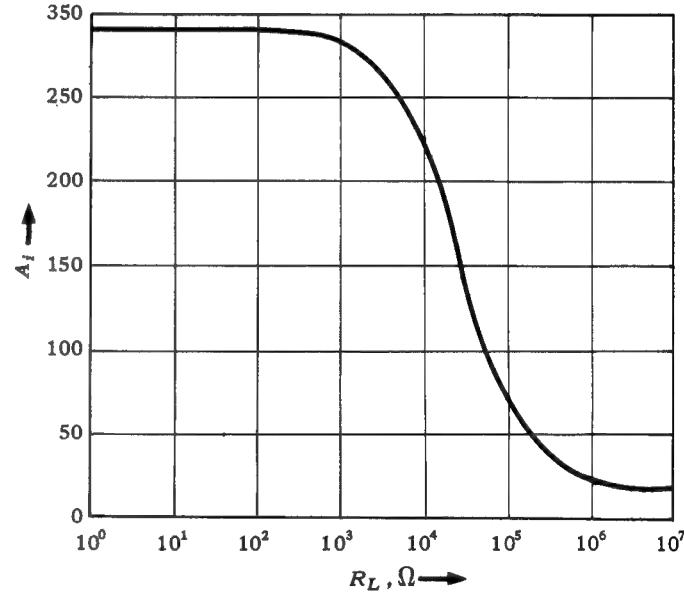

Fig. 5.12　Variation of A_i with R_L in common-collector amplifier.

As a convenience in carrying out analyses similar to the ones in this chapter, Table 5.1 summarizes the formulae for the performance factors of the single-stage audio amplifier.

TABLE 5.1 Single-Stage Amplifier Formulae

	$R_i = \dfrac{v_i}{i_i}$	$R_o = \dfrac{v_o}{i_o}$	$A_i = \dfrac{i_o}{i_i}$	$A_v = \dfrac{v_o}{v_i}$
h-parameters (Second subscript omitted)	$h_i - \dfrac{h_f h_r}{\dfrac{1}{R_L} + h_o}$	$\dfrac{1}{h_o - \dfrac{h_f h_r}{h_i + R_g}}$	$\dfrac{h_f}{1 + h_o R_L}$	$\dfrac{-R_L h_f}{h_i\left[1 + R_L\left(h_o - \dfrac{h_f h_r}{h_i}\right)\right]}$
Common-base tee-equivalent circuit (see Fig. 2.31)	$r_e + r_b(1-\alpha) + r_b\,\dfrac{\alpha\dfrac{R_L}{r_c} + (1-\alpha)\dfrac{r_b}{r_c}}{1 + \dfrac{R_L + r_b}{r_c}}$ $\cong r_e + r_b(1-\alpha),$ $\dfrac{r_b}{r_c} \ll \beta \quad \dfrac{R_L}{r_d} \ll 1$	$r_c + r_b - \dfrac{\alpha r_c + r_b}{1 + \dfrac{r_e + R_g}{r_b}}$	$\dfrac{\alpha + \dfrac{r_b}{r_c}}{1 + \dfrac{r_b + R_L}{r_c}} \cong \alpha,$ $\dfrac{r_b + R_L}{r_c} \ll 1$	$\dfrac{\left(\alpha + \dfrac{r_b}{r_c}\right)R_L}{r_c\left(1 + \dfrac{r_b + R_L}{r_c}\right) + r_b\left(1 - \alpha + \dfrac{R_L}{r_c}\right)}$ $\cong \dfrac{\alpha R_L}{r_c + r_b\left(1 - \alpha + \dfrac{R_L}{r_c}\right)}, \quad \dfrac{r_b + R_L}{r_c} \ll 1$
Common-emitter tee-equivalent circuit (see Fig. 2.31) **Note:** $r_e^* = r_e + R_g$; R_g = circuit resistance in emitter	$r_b + r_e^*(1+\beta)\,\dfrac{1 + \dfrac{R_L}{r_d(1+\beta)}}{1 + \dfrac{R_L + r_e^*}{r_d}}$ $\cong r_b + r_e^*(1+\beta),$ $R_L + r_e^* \ll r_d$	$r_d\left[1 + \dfrac{r_e^*}{r_d} + \dfrac{\beta - \dfrac{r_e^*}{r_d}}{1 + \dfrac{R_g + r_b}{r_e^*}}\right]$ $\cong r_d\left[1 + \dfrac{\beta}{1 + \dfrac{R_g + r_b}{r_e^*}}\right]$ $\dfrac{r_e^*}{r_d} \ll 1$	$\dfrac{\beta - \dfrac{r_e^*}{r_d}}{1 + \dfrac{R_L + r_e^*}{r_d}}$ $\cong \dfrac{\beta}{1 + \dfrac{R_L}{r_d}}$ $r_e^* \ll r_d$	$\dfrac{R_L}{r_e^*} \times \dfrac{\dfrac{\beta}{\beta+1} - \dfrac{r_e^*}{r_d'(\beta+1)}}{1 + \dfrac{R_L}{r_d(\beta+1)} + \dfrac{r_b}{r_e^*(1+\beta)}\left(1 + \dfrac{r_e^* + R_L}{r_d}\right)}$ $\cong -\dfrac{R_L}{r_e^*},$ $r_e^* \ll r_d, \quad \beta \gg 1, \quad R_L \ll r_d$
Common-collector tee-equivalent circuit (see Fig. 2.31)	$r_b + \dfrac{(R_L + r_e)(\beta+1)}{1 + \dfrac{(R_L + r_e)(\beta+1)}{r_c}}$ $\cong r_b + (R_L + r_e)(\beta+1),$ $r_c \gg (R_L + r_e)(\beta+1)$	$r_e + \dfrac{R_g + r_b}{1+\beta} \times \dfrac{1}{1 + \dfrac{R_g + r_b}{r_d(1+\beta)}}$ $\cong r_e + \dfrac{R_g + r_b}{1+\beta},$ $R_g \ll r_c$	$(1+\beta)\,\dfrac{1}{1 + \dfrac{r_e + R_L}{r_d}}$ $\cong 1 + \beta,$ $r_e + R_L \ll r_d$	$\dfrac{1}{1 + \dfrac{r_b}{r_c} + \left[r_e\left(1 + \dfrac{r_b}{r_c}\right) + \dfrac{r_b}{1+\beta}\right]\dfrac{1}{R_L}}$ $\cong \dfrac{1}{1 + \left(r_e + \dfrac{r_b}{1+\beta}\right)\dfrac{1}{R_L}} = \dfrac{1}{1 + \dfrac{h_{ib}}{R_L}},$ $r_b \ll r_c$

5.5 High-Frequency Performance

In this section, we will consider the behavior of the transistor at high frequencies, at which point transistor parameters become complex. In the border-line region where frequency effects just begin to appear, it is sufficient to use a complex forward current gain. For a useful representation satisfactory over a very wide frequency range, the hybrid-π circuit is easily the most convenient.

Consider the h-parameter common-base equivalent circuit with complex forward current gain. Let h_{fbo} be the low-frequency value of h_{fb}. The following approximate relationship based on intrinsic solid-state properties of the transistor holds at intermediate frequencies:

$$h_{fb} = \frac{h_{fbo}}{1 + j\dfrac{f}{f_{hfb}}}, \tag{5.32}$$

in which f_{hfb} is the α (or h_{fb}) *cut-off frequency* where the absolute value of current gain declines to 0.707 of its low-frequency value.

Now determine the complex forward current gain for the common-emitter configuration:

$$h_{fe} = \frac{-h_{fb}}{1 + h_{fb}}. \tag{5.33}$$
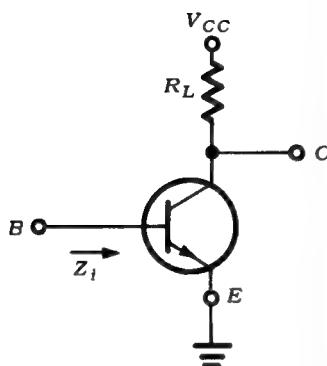
Fig. 5.13 Single common-emitter circuit.
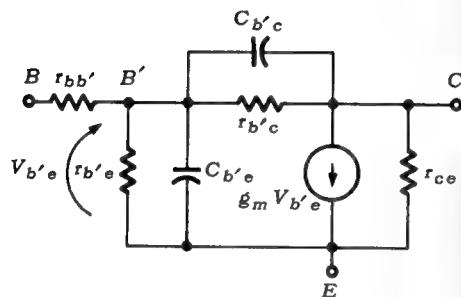
Substituting the complex expression for h_{fb} in (5.33) and simplifying,

$$h_{fe} = \frac{\dfrac{-h_{fbo}}{1 + h_{fbo}}}{1 + \dfrac{jf}{f_{hfb}(1 + h_{fbo})}}, \qquad (5.34)$$

If we let $f_{hfb}(1 + h_{fbo}) = f_{hfe}$, the frequency where h_{fe} (or β) is down to 0.707 of its low-frequency value (the β cut-off frequency), then

$$h_{fe} = \frac{h_{feo}}{1 + j\dfrac{f}{f_{hfe}}}, \qquad (5.35)$$

where h_{feo} is the low-frequency value of h_{fe}.

The cut-off frequencies give a reasonably good idea where frequency effects start to become important. However, they are only a very approximate indication of a transistor's high-frequency capability. From (5.34), we see that the common-emitter configuration has a bandwidth smaller by a factor of $1 + h_{fbo}$ than the common-base configuration. (Recall that h_{fbo} is negative and nearly unity, so that $1 + h_{fbo}$ is a very small number.)

Fig. 5.14 Hybrid-π equivalent circuit for common-emitter connection.

5.6 Hybrid-π Circuit

The hybrid-π circuit is superior to other high-frequency equivalent circuits, in that its parameters are relatively independent of frequency over a very wide range. Furthermore, we can measure all parameters directly at high frequencies.

Figure 5.13 is the simple common-emitter circuit, represented for small signals by the hybrid-π model of Fig. 5.14. The low-frequency conversion formulae from h-parameters are given by Table 3.1, with $r_{bb'}$ arbitrarily chosen. Table 5.2 presents a concise procedure for direct measurement of the hybrid-π parameters.

We now proceed to applications of the hybrid-π model, calculating input impedance Z_i, current gain A_i, and voltage gain A_v for given load conditions. Although the derived results are general, only a few simple cases will be investigated numerically, because of the extreme complexity of the computations.
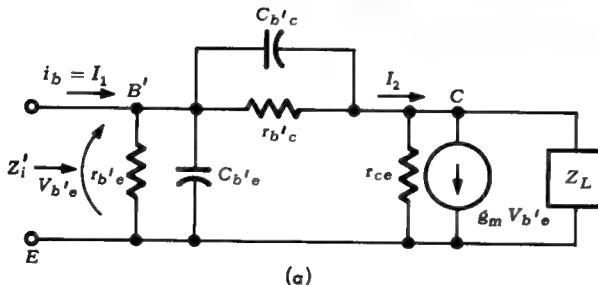

Fig. 5.15 (a) Hybrid-π equivalent circuit set-up for calculating input impedance. (b) Substitution of complex impedances.
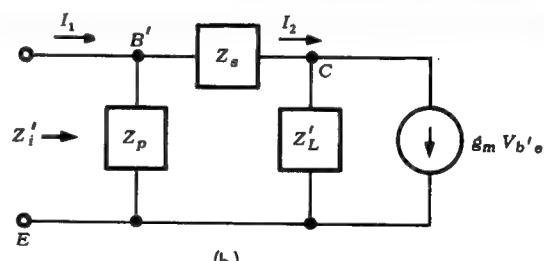
Refer to Fig. 5.15a, and the somewhat simplified representation of Fig. 5.15b. For convenience, we replace the resistance-capacitance combinations with complex impedances. The base-spreading resistance $r_{bb'}$ is initially neglected. The current source is replaced by a more familiar equivalent voltage source in Fig. 5.16a. The mesh equations are*

*Note that in the remainder of this Chapter, rms values are used rather than instantaneous values.

$$V_{b'e} = Z_p I_1 - Z_p I_2 = Z_p (I_1 - I_2),$$

$$g_m V_{b'e} Z_L' = -Z_p I_1 + (Z_p + Z_s + Z_L') I_2 = g_m Z_p Z_L' (I_1 - I_2).$$
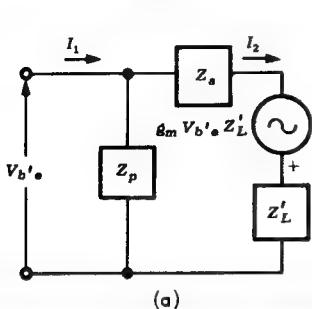
(a)
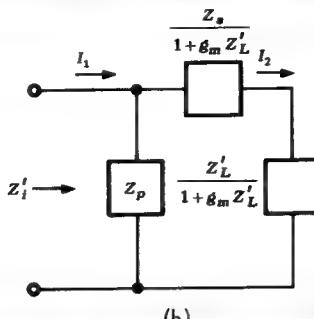
(b)
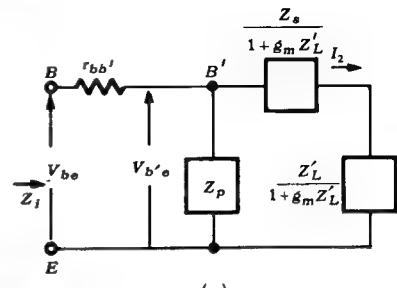
(c)

Rearranging the second equation,

$$0 = -Z_p [1 + g_m Z_L'] I_1 + [Z_p (1 + g_m Z_L') + (Z_L' + Z_s)] I_2.$$

Dividing the above equation by $1 + g_m Z_L'$, the set of equations becomes

$$V_{b'e} = Z_p I_1 - Z_p I_2, \qquad (5.36)$$

$$0 = -Z_p I_1 + \left(Z_p + \frac{Z_L' + Z_s}{1 + g_m Z_L'} \right) I_2 \qquad (5.37)$$

Figure 5.16b shows the equivalent circuit representation of these equations. The validity of the equivalent circuit may be demonstrated by writing its mesh equations and comparing with those derived above.

An obvious extension of Fig. 5.16b, in which $r_{bb'}$ is added to give an exact value of Z_i without dependent sources, is shown in Fig. 5.16c. In Fig. 5.16d, the generalized complex impedances are separated into resistive and capacitive components. The real number A is introduced to simplify calculations. This circuit can be used to compute $V_{b'e}$ and I_2, which are required to determine performance characteristics of the amplifier stage. To determine I_c and V_{ce}, use the output circuit of Fig. 5.17b, which is derived from Fig. 5.15a.

$$A = \text{real number} = 1 + g_m \frac{Z_L r_{ce}}{Z_L + r_{ce}}$$

(d)

Fig. 5.16 (a) Replacing the current source of Fig. 5.15 (b) by an equivalent voltage source. (b) Further simplification of input impedance circuit with only passive elements. (c) Extension of (b) to include $r_{bb'}$. (d) Circuit of (c) in which complex impedances are replaced by resistance-capacitance equivalents.

PROBLEM 5.21 Referring to the output circuit of Fig. 5.17b, where

$$I_2 = j10^{-4} \text{a},$$

$$V_{b'e} = 10^{-2} \text{v},$$

$$r_{ce} = 10^5 \text{ }\Omega,$$

$$Z_L = 5 \times 10^3 \text{ }\Omega,$$

$$g_m = 0.1 \text{ mho},$$

calculate I_c and V_{ce}.

Solution: Establish the current source:

$$g_m V_{b'e} = 10^{-1} \times 10^{-2} = 10^{-3} \text{ a} \equiv 1 \text{ ma}.$$

The currents may be summed at the node:

$$I_2 + I_c - \frac{V_{ce}}{r_{ce}} = g_m V_{b'e},$$

where the current through r_{ce} has the direction shown in Fig. 5.17b. Since $I_c = -V_{ce}/R_L$, V_{ce} is the only unknown in the above expression. Substituting numerical values and solving,

$$V_{ce} = -4.76 (1 - 0.1j) \text{ v}, \qquad |V_{ce}| = 4.8 \text{ v}.$$

(a)

(b)

Fig. 5.17 (a) Output portion of hybrid-π equivalent circuit. (b) Expansion of (a).

TABLE 5.2 Direct measurement of Hybrid-π parameters. (Refer to the hybrid-π equivalent circuit of Fig. 5.14.)

1. Refer to Fig. (a). Capacitors C_1 and C_2 are effective short-circuits to a-c test signals. Set R_L and R_B for the desired operating (Q) point. The value of $R_B \gg Z_i$, so that bias current to the base is essentially constant. With the short-circuit from the collector to the emitter (due to C_2), $C_{b'e}$ and $C_{b'c}$ are essentially in parallel with $r_{b'e}$. Apply a sufficiently high frequency (say 5 times f_{hfe}) from base to emitter, so that B' is effectively short-circuited to ground. Measure i_i and v_{be} to determine $r_{bb'}$. More accurately, we can measure the resistive component of Z_i with a suitable impedance bridge. (Note that since $r_{b'c} \gg r_{b'e}$, there is negligible error in neglecting $r_{b'c}$ at the frequency in question.)

2. Compute the remaining low-frequency hybrid-π parameters from the previously derived formulae:

$$r_{b'e} = \frac{h_{ie} - r_{bb'}}{1 - h_{re}} \cong h_{ie} - r_{bb'} , \qquad [3.61]$$

$$r_{b'c} = \frac{h_{ie} - r_{bb'}}{h_{re}} , \qquad [3.60]$$

$$\frac{1}{r_{ce}} = h_{oe} - h_{re} \frac{1 + h_{feo} - h_{re}}{h_{ie} - r_{bb'}} \cong h_{oe} , \qquad [3.63]$$

$$g_m = \frac{h_{feo}}{h_{ie} - r_{bb'}} . \qquad [3.56]$$

3. The circuit of Fig. (b) is used for measuring $C_{b'c}$. The emitter impedance is sufficiently large so as to present an essentially open emitter to a-c. Resistance R_L is high enough so as not to shunt the collector-base capacitance too heavily. Using a capacitance bridge between points B and C, measure C_{ob}, the output capacity for the common-base configuration with emitter open. The measurement is to be made at a frequency such that the reactance of $C_{b'c}$ is much greater than $r_{bb'}$ and much less than $r_{b'c}$. In performing the capacitance measurement, note that the dissipation factor is small, confirming that the test frequency has been properly selected. Output capacity C_{ob}, thus measured, approximately equals $C_{b'c}$.
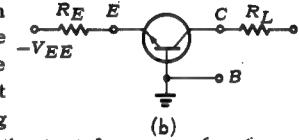
The measurement outlined here establishes the value of $C_{ob} \cong C_{b'c}$, plus lead capacities, and the so-called *overlap-diode capacity*, which is the capacity between electrodes outside the active transistor region. These must be subtracted from the measured capacitance. Unfortunately, an accurate determination of $C_{b'c}$ is not easy. Conveniently, however, C_{ob} is usually specified by the manufacturer for high-frequency transistors.

4. To measure $C_{b'e}$, refer to Fig. (c). Capacitance C is a short-circuit at the test frequency. Resistance R is a small resistor, chosen to measure current i_c by its drop $v_R = i_c R$. The value $R_g \gg h_{ie}$, so that i_b is essentially a constant base current, $i_b = v_g / R_g$. Since R is a very small resistance value, $v_{ce} \cong 0$, so that from the point of view of input impedance, $C_{b'c}$ is effectively in parallel with $C_{b'e}$. Also $r_{b'c} \gg r_{b'e}$.

For these conditions, the hybrid-π circuit corresponding to Fig. (c) is approximately as shown in Fig. (d). The following expressions apply to the circuit of this figure,*

$$V_R = i_c R = R g_m V_{b'e},$$

$$= R g_m \frac{V_g}{R_g} \frac{r_{b'e} [1/j\omega(C_{b'e} + C_{b'c})]}{r_{b'e} + [1/j\omega(C_{b'e} + C_{b'c})]} .$$
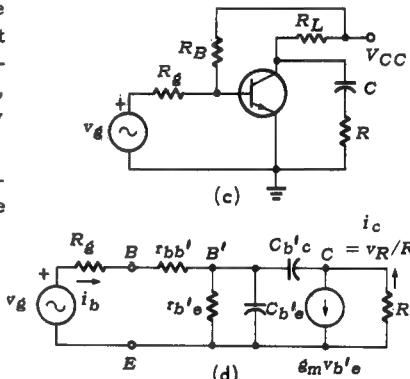
By measuring V_R at low frequency, say 1000 cps, and at the much higher frequency where V_R has dropped to 0.707 of V_R at low frequency, we determine f_{hfe} where

$$r_{b'e} = \frac{1}{2\pi f_{hfe}(C_{b'e} + C_{b'c})} .$$

Thus, since $C_{b'c}$ is known from the preceding step,

$$C_{b'e} + C_{b'c} = \frac{1}{2\pi f_{hfe} r_{b'e}}, \qquad \text{or} \qquad C_{b'e} = \frac{1}{2\pi f_{hfe} r_{b'e}} - C_{b'c} .$$

Manufacturer specification sheets usually give f_{hfe}. Sometimes the transistor manufacturer gives $f_T = h_{feo} f_{hfe}$, a *gain bandwidth product*. In this instance, the α cut-off frequency is

$$f_T = h_{feo} f_{hfe} \cong (1 + h_{feo}) f_{hfe} = f_{hfb}.$$

───
*Note the use of rms vectors rather than instantaneous values in the following equations.

Solving for $I_c = -V_{ce}/R_L$,

$$I_c = 0.95 \times 10^{-3}\,(1 - 0.1j)\ \text{a}; \quad |I_c| = 0.96\ \text{ma}.$$

To complete the representation of the hybrid-π by separate passive input and output circuits, we now derive an equivalent *output circuit* containing no dependent sources. Figure 5.18a shows the output circuit with the input terminated in a generator impedance, Z_g. For convenience, complex impedances are used to represent capacitor-resistor combinations. Impedances Z_p' and Z_o' are defined on the figure. Referring to the simplified configuration of Fig. 5.18b, the circuit equations are

$$g_m V_{b'e} = I_1 + I_2,$$
$$V_{b'e} = -I_2 Z_p'.$$

Combining,

$$-I_2 Z_p' g_m = I_1 + I_2.$$

Solving for I_1,

$$I_1 = -I_2\,(1 + Z_p' g_m).$$

Since $V_{ce} = -I_2\,(Z_s + Z_p')$,

$$Z_o' = \frac{V_{ce}}{I_1} = \frac{-I_2\,(Z_s + Z_p')}{-I_2\,(1 + Z_p' g_m)} = \frac{Z_s + Z_p'}{1 + Z_p' g_m}. \tag{5.38}$$

Adding r_{ce}, we derive the simple form for the output circuit of Fig. 5.18c.
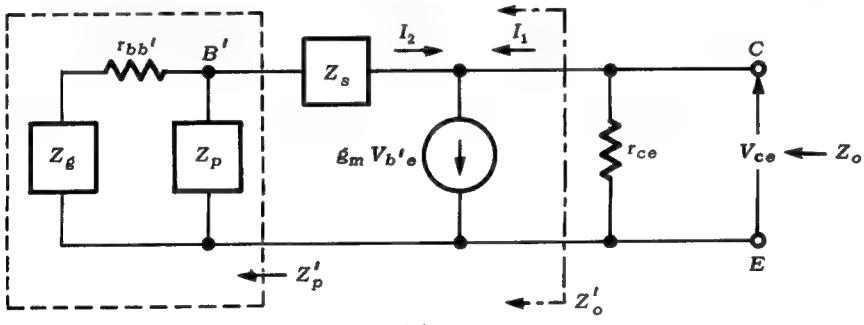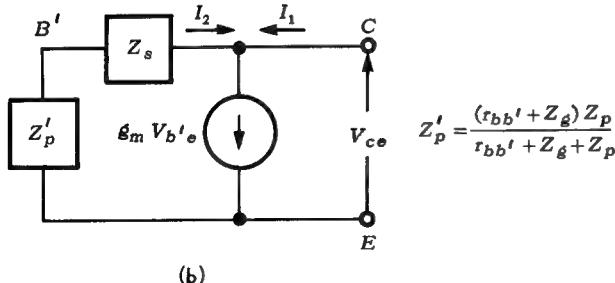
$$Z_p' = \frac{(r_{bb'} + Z_g)Z_p}{r_{bb'} + Z_g + Z_p}$$
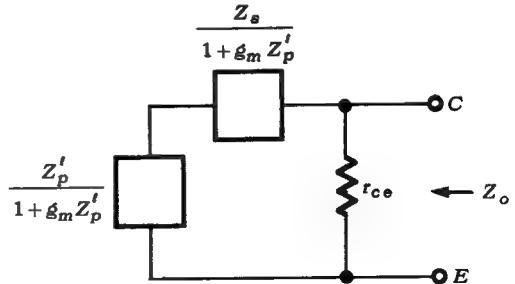
Fig. 5.18 (a) Hybrid-π equivalent output circuit. (b) Simplified equivalent of (a). (c) Final simplified representation.

PROBLEM 5.22 Develop the input impedance network representation of the common-emitter amplifier circuit of Fig. 5.19.

Solution: The model of Fig. 5.16d is applicable and will be used for the solution to this problem. Direct substitution is all that is required:
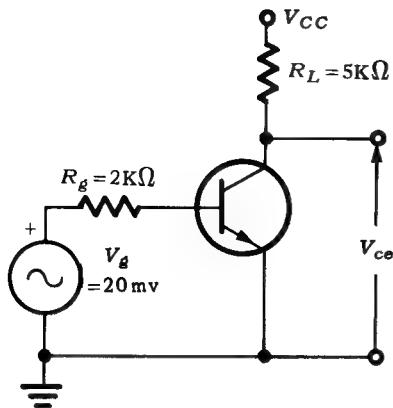
Transistor hybrid-π parameters

$$r_{bb'} = 100\,\Omega$$
$$\mathscr{g}_m = 0.138 \text{ mho}$$
$$r_{b'c} = 10^7\,\Omega$$
$$r_{b'e} = 2100\,\Omega$$
$$r_{ce} = 435\,K\Omega$$
$$C_{b'c} = 5\,\mu\mu f$$
$$C_{b'e} = 250\,\mu\mu f$$

Fig. 5.19 Common-emitter circuit with parameters corresponding to Prob. 5.22.

$$A = 1 + \mathscr{g}_m \frac{R_L \, r_{ce}}{R_L + r_{ce}}.$$

Substituting numerical values from Fig. 5.19, $A = 685$. Continuing,

$$\frac{Z_L}{A} = \frac{5000}{685} = 7.3\ \Omega,$$

$$\frac{r_{ce}}{A} = \frac{435,000}{685} = 635\ \Omega,$$

$$\frac{r_{b'c}}{A} = \frac{10^7}{685} = 14,600\ \Omega,$$

$$AC_{b'c} = 685 \times 5 = 3425\ \mu\mu f.$$

These calculated results are shown on the hybrid-π circuit of Fig. 5.20. Several interesting results are evident. The 7.3 Ω effective resistance from collector to base is so low that it acts as an effective short-circuit. Point C is therefore substantially at ground potential. Thus, as far as input impedance is concerned, $AC_{b'c}$ is in parallel with $C_{b'e}$. This multiplication of capacitance, leading to a comparatively very large capacitance in shunt across the input, is known as the *Miller effect*. It is an example of the effective amplification of an impedance in an active network. Although $r_{b'c}$ is also "transformed", it is relatively so large that its effect is usually ignored.
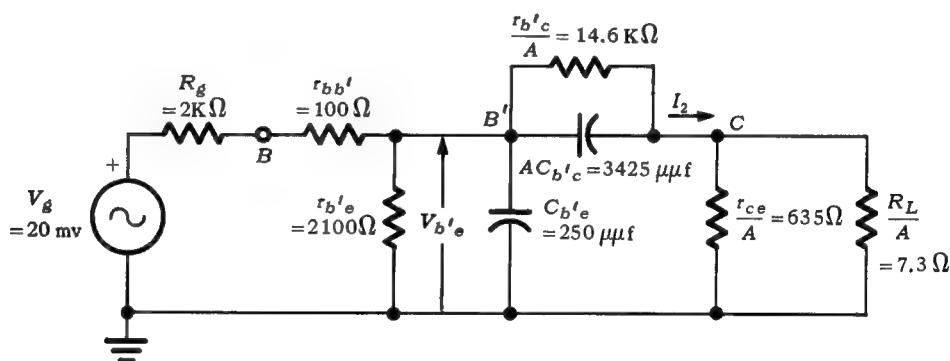
Fig. 5.20 Hybrid-π equivalent input circuit corresponding to the configuration of Fig. 5.19.

$$R_1 = \frac{r_{b'e}\, r_{b'c}/A}{r_{b'e} + r_{b'c}/A} = 1835\,\Omega$$

$$R_2 = R_g + r_{bb'} = 2100\,\Omega$$

$$C_1 = C_{b'e} + AC_{b'c} = 3675\,\mu\mu f$$
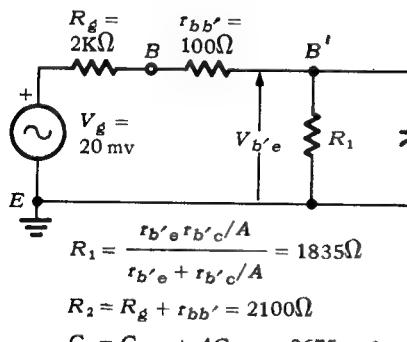
Fig. 5.21 Simplified form of the input circuit of Fig. 5.20.

PROBLEM 5.23 For the amplifier circuit of Fig. 5.19, determine the frequency where voltage gain falls to 0.707 of its low-frequency value.

Solution: The circuit of Fig. 5.20, developed in the preceding problem, still applies. Simplify as shown in Fig. 5.21 and calculate $V_{b'e}$:

$$V_{b'e} = \frac{\dfrac{R_1\left(\dfrac{1}{j\omega C_1}\right)}{R_1 + \dfrac{1}{j\omega C_1}}}{R_2 + \dfrac{R_1\left(\dfrac{1}{j\omega C_1}\right)}{R_1 + \dfrac{1}{j\omega C_1}}}\, V_g = \frac{R_1}{R_2\,(1 + j\omega\,C_1 R_1) + R_1}\, V_g. \tag{5.39}$$

Now calculate I_2, assuming that the collector is essentially at ground potential, and that $r_{b'c} \gg 1/(j\omega C_{b'c})$ in the significant frequency range. Thus, directly from Fig. 5.20,

$$I_2 = \frac{V_{b'e}}{\dfrac{1}{j\omega C_{b'c} A}}. \qquad (5.40)$$

Referring to Fig. 5.17b, with $V_{b'e}$ and I_2 known from (5.39) and (5.40), and recognizing that $r_{ce} \gg Z_L$,

$$g_m V_{b'e} = I_2 + I_c. \qquad (5.41)$$

Substituting numerical values, $V_{b'e}$ and I_2 are calculated, from which I_c is directly obtained:

$$V_{b'e} = \frac{1835}{1835 + 2100\,(1 + j\omega\,6.75 \times 10^{-6})}\,V_g,$$

$$I_2 = j\omega\,3425 \times 10^{-12}\,V_{b'e}.$$

Substituting in (5.41) and simplifying,

$$I_c = \frac{253\,(1 - 0.0248\,j\omega \times 10^{-6})}{3935\,(1 + 0.362\,j\omega \times 10^{-6})}\,V_g.$$

The frequency of interest, where the output falls to 0.707 of its low-frequency value, coincides with the 0.707 point of I_c. This frequency is where the phase shift is approximately $45°$. For simplicity, and because it is justified by the general accuracy of this type of calculation, we neglect the imaginary term in the numerator of the above expression for I_c. The required frequency occurs where

$$0.362\,\omega \times 10^{-6} = 1,$$

corresponding to

$$f = 440 \text{ K Hz.}$$

Fig. 5.22 Common-emitter amplifier circuit applicable to Prob. 5.23.

PROBLEM 5.24 Calculate the input impedance Z_i for the amplifier circuit of Fig. 5.22 at $\omega = 10^6$ radian/sec. Neglect r_{ce} and $r_{b'c}$.

Solution: Use the model of Fig. 5.16. Now,

$$A = 1 + g_m Z_L' \cong 1 + g_m Z_L.$$

Since $Z_L = j\omega L$,

$$A = 1 + g_m\,(j\omega L).$$

Substituting numerical values,

$$A = 1 + (0.138)\,(j\,5 \times 10^{-3} \times 10^6) = j\,690,$$

$$Z_s \cong \frac{1}{j\omega C_{b'c}} \text{ (at } \omega = 10^6) = -j\,2 \times 10^5,$$

$$\frac{Z_s}{A} = \frac{-j\,2 \times 10^5}{j\,690} = -290\ \Omega,$$

$$\frac{Z_L'}{A} = \frac{j\,5000}{j\,690} = 7.2\ \Omega.$$

The equivalent circuit representing input impedance is shown in Fig. 5.23. The series resistances may be added and combined with $r_{b'e}$ for an equivalent shunt

Fig. 5.23 (a) Equivalent input impedance circuit corresponding to the amplifier of Fig. 5.22. (b) Simplified equivalent of (a).

resistance of $-327\ \Omega$. Input impedance is then readily calculated as

$$Z_i = -3980 - j\,32.5.$$

The input impedance is negative, which occasionally occurs when amplified impedance is reflected back to the primary. For this condition, the amplifier will behave as an oscillator.

5.7 Supplementary Problems

PROBLEM 5.25 If $h_{ie} = 300\,\Omega$, $h_{oe} = 10^{-5}\,\Omega$, $h_{re} = 10^{-4}\,\Omega$, and $h_{ie} = 2000\,\Omega$ in the common-emitter circuit of Fig. 5.2, calculate (a) Z_i and Z_o for $R_L = R_g = 10,000\,\Omega$, (b) the current and voltage gain for $R_L = R_g = 10,000\,\Omega$, and (c) the value of R_L which yields the maximum power gain.

PROBLEM 5.26 Determine the effect of a change in R_L on the input impedance Z_i for a common-emitter circuit.

PROBLEM 5.27 Calculate the common-emitter tee-equivalent circuit for the transistor of Prob. 5.25.

PROBLEM 5.28 Find the effect on the tee-equivalent resistor of Prob. 5.27 when a resistor R_E is added in series to the emitter.

PROBLEM 5.29 A resistor $R = 100\,\Omega$ is added in series to the common-emitter circuit of Prob. 5.2. Calculate (a) Z_i, Z_o, and the current and voltage gains when $R_L = R_g = 10,000\,\Omega$, and (b) the value of R that yields the maximum power gain.

PROBLEM 5.30 Discuss the advantages and disadvantages of the tee-equivalent circuit.

PROBLEM 5.31 Derive the formulae for Z_i, Z_o, A_i, and A_v for the common-emitter circuit using (a) h-parameters and (b) tee-parameters.

PROBLEM 5.32 Why is the common-collector circuit useful? What are its main characteristics?

PROBLEM 5.33 Define β cut-off frequency.

PROBLEM 5.34 Find the gain change from 0 to 1 MHz when a transistor with a β of 300 and a β cut-off of 10 MHz is used (a) in a common-emitter configuration and (b) in a common-base configuration.

PROBLEM 5.35 In the circuit of Fig. 5.22, use a transistor whose hybrid-π parameters are given in Fig. 5.19. (a) Calculate the input impedance and voltage gain *without* neglecting r_{ce} and $r_{b'c}$. (b) Compare the results of part (a) to those of Prob. 5.24.

MULTI-STAGE AMPLIFIERS

6.1 Introduction

The techniques developed in previous chapters, particularly Chap. 5, may be applied to the analysis of multi-stage amplifiers. There are two basic analytical approaches:

1. We can replace each transistor by its equivalent circuit or model, and analyze the resulting multi-mesh network.
2. Or we can apply the formulae developed in Chap. 5 to each stage in turn, and account for the interaction between stages by using suitable input and output resistances. The effects of coupling networks can also be included in this approach.

The first of these methods is extremely tedious, except in the simplest of cases, and is generally useful only for elementary multi-stage circuits with two or three transistors. The second method, on the other hand, is practical and easy to apply to all configurations.

Consider, for example, the block diagram of a multi-stage circuit in Fig. 6.1. For each stage, the output impedance of the preceding stage is its *input* or *driving impedance*, while the input impedance of the succeeding stage is its *output* or *load impedance*.
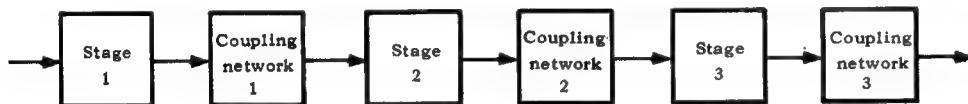
Fig. 6.1 Block diagram representation of a multi-stage amplifier.

By means of the formulae of Chap. 5, the input impedance Z_i of a stage can be calculated if the load impedance is known. As load impedance is generally specified only at the output stage, it is customary to start here. The input impedance obtained then becomes the load impedance of the preceding stage, and so forth.

Similarly, the output impedance Z_o of a stage depends on its driving impedance. As driving impedance is generally specified only at the input stage, calculations start here. In turn its output impedance becomes the driving impedance of the succeeding stage, and so forth.

PROBLEM 6.1 For the two-stage amplifier of Fig. 6.2, calculate the small-signal a-c quantities R_i, R_o, and A_v. Use the parameters for the 2N930 transistor given in Tables 6.1-2 and Appendix A.

Solution: Figure 6.2 shows an emitter-follower stage feeding an output emitter-follower stage. Our first step is to estimate the bias voltages.
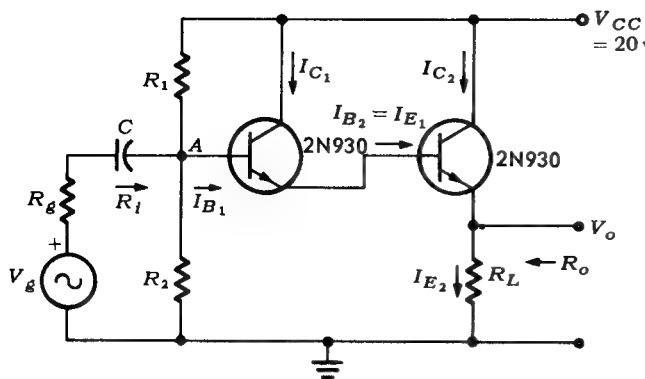
R_I, R_o = input, output resistance, respectively, of two-stage amplifier

R_{I_1}, R_{o_1} = input, output resistance, respectively, of first stage

R_{I_2}, R_{o_2} = input, output resistance, respectively, of second stage

C = coupling capacitor, assumed infinite

$R_L = 2500\,\Omega$

$R_g = 2000\,\Omega$

$R_1 = 1.78\,M\Omega$

$R_2 = 2.27\,M\Omega$

Fig. 6.2 Two-stage direct-coupled emitter-follower amplifier.

TABLE 6.1 Type No. 2N930.

Electrical Parameters	$I_C = 13\,\mu a$	$I_C = 4\,ma$	Unit
h_{ib} *	2100	17	ohm
h_{ob} *	0.045×10^{-6}	0.056×10^{-6}	mho
h_{fe} *	200	370	
h_{rb} *	1.5×10^{-4}	2.3×10^{-4}	
h_{ic} **	420,000	6300	ohm
h_{oc} **	9×10^{-6}	20.8×10^{-6}	mho
h_{fc} **	-201	-371	
h_{rc} **	1	1	

* Published data
** Derived data using conversion formulae of Chap. 3

TABLE 6.2 Type No. 2N930.

Electrical Parameters	$I_C = 1\,ma$		$I_C = 2\,ma$		$I_C = 3\,ma$		Unit
	25°C	100°C	25°C	100°C	25°C	100°C	
h_{fe}	320	460	340	480	360	500	
h_{ib}	30	36	20	24	16	20	ohm
h_{ob}	0.076×10^{-6}	0.086×10^{-6}	0.11×10^{-6}	0.13×10^{-6}	0.15×10^{-6}	0.18×10^{-6}	mho
h_{rb}	1.8×10^{-4}	2.5×10^{-4}	2.0×10^{-4}	2.8×10^{-4}	2.2×10^{-4}	3.0×10^{-4}	
$r_c = 1/h_{ob}$	13.2×10^6	11.6×10^6	9.1×10^6	7.7×10^6	6.7×10^6	5.57×10^6	ohm
$h_{ic} = h_{ib}(1 + h_{fe})$	9630	16,650	6820	11,600	5780	10,000	ohm
$h_{oc} = h_{ob}(1 + h_{fe})$	24.4×10^{-6}	39.6×10^{-6}	37.4×10^{-6}	62.5×10^{-6}	54×10^{-6}	90.5×10^{-6}	mho
$h_{re} = h_{ib}h_{ob}(1 + h_{fe}) - h_{rb}$	5.5×10^{-4}	11.7×10^{-4}	5.5×10^{-4}	12.2×10^{-4}	6.4×10^{-4}	15×10^{-4}	
$r_b = h_{ie} - r_e(1 + h_{fe})$	2230	2750	1710	2450	1330	1500	ohm
$r_e = h_{re}/h_{oe}$	23	30	15	19	12	17	ohm

To determine the d-c bias at the base of the first transistor, point A, apply Thevenin's theorem to the voltage divider consisting of R_1 and R_2. The equivalent source voltage and resistance are

$$V_{eq} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{2.27 \times 20}{1.78 + 2.27} = 11.2\,v,$$

$$R_{eq} = \frac{R_1 R_2}{R_1 + R_2} = \frac{1.78 \times 2.27}{1.78 + 2.27} = 1\,M\Omega.$$

If base current is neglected, the potential at point A is 11.2 v.

Between point A and the output V_o, there are two base-emitter drops in series. These are approximately 0.6 v each for silicon transistors at room tem-

perature. Thus the potential at R_L becomes $11.2 - 2(0.6) = 10$ v. For $R_L = 2500 \, \Omega$, the d-c bias current is $10/2500 = 4$ ma.

From Appendix A, h_{FE} at 4 ma is 300. The base current I_{B_2} is

$$I_{B_2} = \frac{4 \times 10^{-3}}{300} = 13.3 \, \mu\text{a}.$$

Base current I_{B_2} is, of course, the emitter current I_{E_1} of the first transistor. For this current, h_{FE} is approximately 150, so that

$$I_{B_1} = \frac{13.3 \times 10^{-6}}{150} \cong 0.09 \, \mu\text{a}.$$

This base current (previously assumed negligible) somewhat reduces the potential at point A. Since the Thevenin equivalent source impedance at A was calculated to be 1 MΩ, the additional drop due to I_{B_1} is about 0.09 v. The potential at A is more accurately $11.2 - 0.09 = 11.11$ v.

Again referring to Appendix A for base emitter drop, and assuming collector and emitter currents to be essentially equal,

$$V_{BE_1} \cong 0.5 \text{ v at } I_{C_1} = 13 \, \mu\text{a},$$

$$V_{BE_2} \cong 0.61 \text{ v at } I_{C_2} = 4 \text{ ma},$$

so that

$$V_{E_2} = 11.11 - 0.5 - 0.61 = 10 \text{ v}.$$

The first estimate of $V_{E_2} = 10$ v is valid, so the above calculations need not be repeated.

What we have accomplished thus far is a necessary first step in all amplifier calculations, namely, the establishment of d-c operating (quiescent) levels. We now have to determine from the transistor curves the small-signal h-parameters corresponding to these levels. For the present problem, these parameters may be obtained from Table 6.1.

Now we calculate input impedance R_{i_2} of the second stage, which is easy since the load impedance R_L is given:

$$R_{i_2} = h_{ic} - \frac{h_{fc} \, h_{rc}}{h_{oc} + \dfrac{1}{R_L}}. \qquad [5.28]$$

Substituting numerical values from Table 6.1 and Fig. 6.2:

$$R_{i_2} = 6300 - \frac{(-371)(1)}{20.8 \times 10^{-6} + 0.4 \times 10^{-3}} = 886,300 \, \Omega \,,$$

which becomes the load impedance of the first stage, thus making it possible to calculate its input impedance:

$$R_{i_1} = 420,000 - \frac{(-201)(1)}{9 \times 10^{-6} + \dfrac{1}{886,300}} \cong 20 \text{ M}\Omega \,.$$

This is the basic a-c input resistance of the first stage. It is shunted by the bias resistors, R_1 and R_2, which constitute an equivalent 1 MΩ shunt. The net input resistance of the first stage is

$$R_i = \frac{1 \times 20}{21} \text{ M}\Omega \equiv 950,000 \, \Omega \,.$$

Now calculate A_v, the gain from point A to R_L. We obtain this by calculating separately the first and second stage gains, A_{v_1} and A_{v_2}, and multiplying:

$$A_v = A_{v_1} \times A_{v_2}.$$

Again, using the formulae from Chap. 5 (after some simplification),

$$A_{v_1} = \frac{1}{1 + \dfrac{h_{ib}}{R_L}} = \frac{1}{1 + \dfrac{2100}{886,300}} = 0.9976, \qquad [5.31]$$

$$A_{v_2} = \frac{1}{1 + \dfrac{17}{2500}} = 0.993,$$

$$A_v = A_{v_1} \times A_{v_2} = 0.9976 \times 0.993 = 0.9906.$$

This figure is modified by the loading effect of R_i on the generator source impedance R_g. The loss in gain is $2000/950,000 = 0.00210$. Including this attenuation component, the overall gain becomes 0.9885.

To calculate the output impedance, proceed from the input to the output:

$$R_{o_1} = \frac{1}{h_{oc} - \dfrac{h_{fc} h_{rc}}{h_{ic} + R_g}}. \qquad [5.29]$$

Substituting numerical values applicable to the first stage,

$$R_{o_1} = \frac{1}{9 \times 10^{-6} + \dfrac{201}{0.42 \times 10^6 + 2000}} = 2060 \ \Omega.$$

The output resistance of the first stage R_{o_1} becomes the equivalent source impedance for the second stage:

$$R_{o_2} = \frac{1}{21 \times 10^{-6} + \dfrac{371}{6.3 \times 10^3 + 2.06 \times 10^3}} = 24.8 \ \Omega.$$

This is a very useful amplifier circuit, with an input impedance of about $1\ \mathrm{M}\Omega$, and a $25\ \Omega$ output impedance. Voltage gain is approximately 1.2% less than unity, making this two-stage device well suited for good isolation of source and load.

6.2 Capacitor Coupling

In previous chapters, coupling methods were essentially ignored. Coupling and by-pass capacitors were assumed to be infinite, thereby providing zero impedance to a-c signals. In actual practice, however, coupling and by-pass capacitors introduce limits to the low-frequency amplifier response. These limits are now considered.

Refer to Fig. 6.3, which shows a two-stage common-emitter amplifier using both capacitors for interstage coupling (C_1 and C_2), and by-pass capacitors (C_{E_1} and C_{E_2}). The coupling or blocking capacitors prevent undesired d-c coupling between the bias circuits of the separate stages. The by-pass capacitors allow separate adjustment of d-c and a-c circuit parameters. As an introduction to the design characteristics of coupling circuits, it will be assumed in Fig. 6.3 that all capacitors, except the interstage coupling capacitor C_2, are infinite.

PROBLEM 6.2 In Fig. 6.3, with C_{E_1}, C_{E_2}, and C_1 infinite, analyze the effect of C_2 on the *low-frequency response* of the amplifier.
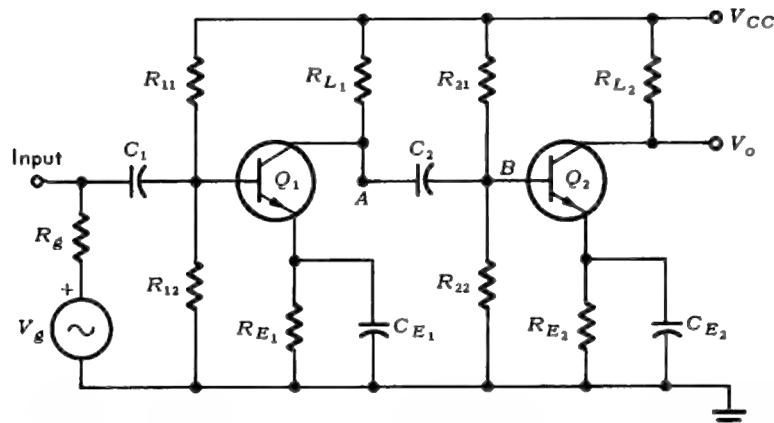
Fig. 6.3 Two-stage amplifier with coupling capacitors.
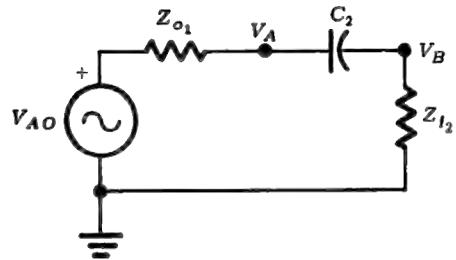
Fig. 6.4 Equivalent circuit for interstage coupling of amplifier stages of Fig. 6.3.

Solution: First calculate the output impedance Z_{o_1} of the first stage, and then obtain the input impedance Z_{i_2} of the second stage. With this information, the effect of a finite C_2 is easily found using simple circuit theory. The values of Z_{o_1} and Z_{i_2} are readily determined by the formulae of Chap. 5, following exactly the procedures set forth. In Fig. 6.3, Z_{o_1} is the output impedance seen at point A, and Z_{i_2} is the input impedance at point B.

The equivalent circuit based on the above impedances is shown in Fig. 6.4. The following relationships are evident:

$$\frac{V_B}{V_{AO}} = \frac{Z_{i_2}}{Z_{i_2} + Z_{o_1} + \dfrac{1}{j\omega C_2}}$$

$$= \frac{Z_{i_2} j\omega C_2}{(Z_{i_2} + Z_{o_1}) j\omega C_2 + 1} .$$

Since Z_{i_2} and Z_{o_1} are resistive, let $Z_{i_2} = R_{i_2}$ and $Z_{o_1} = R_{o_1}$. The time constant is

$$T_2 = (R_{i_2} + R_{o_1}) C_2 . \tag{6.1}$$

Letting $\omega_2 = \dfrac{1}{T_2}$,

$$\frac{V_B}{V_{AO}} = \frac{\dfrac{R_{i_2}}{R_{i_2} + R_{o_1}} j \dfrac{\omega}{\omega_2}}{1 + j \dfrac{\omega}{\omega_2}} .$$

This expression points up the effect of frequency variation in a particularly convenient manner. At $\omega \ll \omega_2$ (low frequency),

$$\frac{V_B}{V_{AO}} \cong j \frac{\omega}{\omega_2} \left(\frac{R_{i_2}}{R_{i_2} + R_{o_1}} \right) .$$

Recalling that $\omega_2 = 1/[(R_{i_2} + R_{o_1}) C_2]$,

$$\frac{V_B}{V_{AO}} \cong j\omega C_2 R_{i_2} .$$

At the intermediate frequency where $\omega = \omega_2$,

$$\frac{V_B}{V_{AO}} = \frac{\dfrac{R_{l_2}}{R_{l_2} + R_{o_1}} j}{1 + j} = \frac{\sqrt{2}}{2} \frac{R_{l_2}}{R_{l_2} + R_{o_1}} \angle 45°.$$

At higher frequencies, $\omega \gg \omega_2$,

$$\frac{V_B}{V_{AO}} \cong \frac{R_{l_2}}{R_{l_2} + R_{o_1}}.$$

The higher frequency characteristic corresponds to the condition where the reactance of C_2 is negligible.
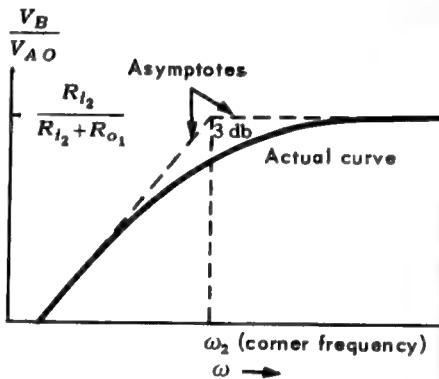

Fig. 6.5 Gain characteristic of interstage coupling network plotted very conveniently on log-log coordinates.

Figure 6.5 shows the frequency characteristic on conventional logarithmic coordinates. This *universal curve* is applicable to any coupling circuit of the configuration considered here. The corner frequency corresponds to ω_2 in the above problem.

The above analytical techniques are equally applicable in considering the effects of C_1, assuming C_2 infinite. In place of R_{o_1} and R_{l_2}, we use R_g and R_{l_1}, respectively. The voltage V_g becomes attenuated and shifted in phase at the base of Q_1 in Fig. 6.3. The effect of C_1 would be plotted as in Fig. 6.5.

However, there is a secondary effect, since a finite C_1 (acting like part of R_g) must introduce a complex component into Z_{o_1}, the complex output impedance of the first stage. This complex component must affect the behavior of the interstage coupling network, and, in effect, it propagates through the entire circuit. This inconvenient feature is unfortunately common in transistor circuits. An exact analysis of the low-frequency response of such circuits becomes extremely tedious. Thus, notwithstanding inaccuracies at frequencies in the vicinity of and lower than the corner frequency, it is most practical to consider the effects of each coupling capacitor separately, and add the separate attenuations and phase shifts as though each were independent. In the higher frequency regions ($\omega \gg \omega_2$) where the amplifier is normally used and phase angles are small, the approximation approach is very satisfactory. The exact alternative, which is extremely tedious, must be used if greater accuracy at very low frequencies is essential.

PROBLEM 6.3   Refer to Fig. 6.3 and assume the following circuit parameters:

R_{11} in parallel with $R_{12} = 1 \text{ M}\Omega$, $h_{ie} = 2200 \ \Omega$,

$R_g = 1 \text{ K}\Omega$, $h_{fe} = 290$,

$C_{E_1} = C_{E_2} = C_1 = \infty$, $h_{re} = 2 \times 10^{-4}$,

$R_{L_1} = R_{L_2} = 5 \text{ K}\Omega$, $h_{oe} = 30 \times 10^{-6}$ mhos.

What is the value of C_2 if gain is to be 3 db down at $\omega = 500$ radians/sec?

Solution: Calculate R_{l_2} and R_{o_1}, using the formulae from Table 5.1:

$$R_{l_2} = h_{ie} - \frac{h_{fe} h_{re}}{h_{oe} + \dfrac{1}{R_L}} = 2200 - \frac{290 (2 \times 10^{-4})}{30 \times 10^{-6} + 200 \times 10^{-6}} = 1950 \ \Omega.$$

Now find R_{o_1}:

$$R_{o_1} = \frac{1}{h_{oe} - \dfrac{h_{fe} h_{re}}{h_{ie} + R_g}} = \frac{1}{30 \times 10^{-6} - \dfrac{(290) 2 \times 10^{-4}}{2200 + 1000}} = 84,400 \ \Omega.$$

This is in parallel with $R_{L_1} = 5 \, K\Omega$, so that

$$R'_{o_1} = \frac{5 \times 84.4}{5 + 84.4} \cong 4.7 \, K\Omega.$$

Now examine the universal curve (Fig. 6.5), noting that the gain is down by 3 db at the corner frequency where $\omega = \omega_2$. The expression for ω_2 is

$$\omega_2 = \frac{1}{C_2(R_{l_2} + R_{o_1})}. \qquad [6.1]$$

Substituting numerical values and solving for C_2,

$$C_2 = \frac{1}{\omega_2(R_{l_2} + R_{o_1})}$$

$$= \frac{1}{500\,(1950 + 4700)}$$

$$= 0.3 \, \mu f.$$

This is a typical coupling capacitor value in a common-emitter circuit. If R_{E_2} were not by-passed, R_{l_2} would be larger and C_2 smaller, but this also results in a loss of gain.

PROBLEM 6.4 For the circuit of Fig. 6.6, find C_2, such that the low-frequency 3 db attenuation point is located at $\omega = 500$ radians/sec. Use the transistor parameters given in Fig. 6.6.

Solution: Refer to Table 5.1 for the formula for input impedance of a common-base circuit:

$$R_i = h_{ib} - \frac{h_{fb} h_{rb}}{h_{ob} + \dfrac{1}{R_L}}.$$

Substituting numerical values,

$$R_i = 7.57 + \frac{0.996 \times 0.27 \times 10^{-4}}{0.103 \times 10^{-6} + 200 \times 10^{-6}} = 7.70 \, \Omega.$$

Since $\omega_2 = \dfrac{1}{7.70 \, C_2}$,

$$C_2 = \frac{1}{500 \times 7.70} = 260 \, \mu f.$$

The low input impedance of the common-base circuit leads to an inconveniently high value of input coupling capacitor.

PROBLEM 6.5 Referring to Prob. 6.3, determine C_2 for a 3 db low-frequency attenuation at $\omega = 500$ radians/sec, omitting by-pass capacitor, C_{E_2}. Use the tee-equivalent circuit with the following parameters:

$$\beta = 290, \qquad\qquad R_{L_1} = R_{L_2} = 5 \, K\Omega,$$

$$r_e = 6.67 \, \Omega, \qquad R_{11} \| R_{12} = R_{21} \| R_{22} = 1 \, M\Omega,$$

$$r_c = 9.7 \, M\Omega, \qquad\qquad R_{\delta} = 1 \, K\Omega,$$

$$r_b = 260 \, \Omega, \qquad\qquad R_{E_2} = 1 \, K\Omega.$$

Solution: Again use Table 5.1 to determine R_{l_2}:
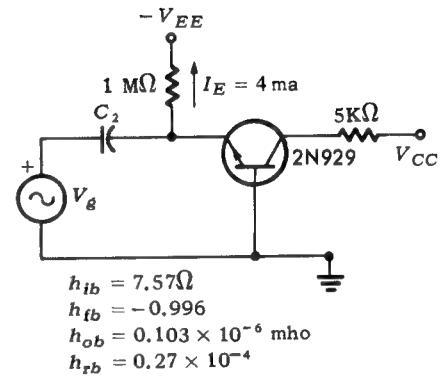
Fig. 6.6 Common-base transistor circuit fed with a constant current emitter bias.

$$h_{ib} = 7.57 \Omega$$
$$h_{fb} = -0.996$$
$$h_{ob} = 0.103 \times 10^{-6} \text{ mho}$$
$$h_{rb} = 0.27 \times 10^{-4}$$

$$R_{i_2} = r_b + r_e^*(1 + \beta) \, \frac{1 + \dfrac{R_L}{r_d(1 + \beta)}}{1 + \dfrac{R_L + r_e^*}{r_d}}.$$

Substituting numerical values,

$$R_{i_2} = 265 \text{ K}\Omega,$$

which in parallel with the equivalent bias network resistance of $1 \text{ M}\Omega$ leads to a net $R_i = 209 \text{ K}\Omega$. From Prob. 6.3,

$$R_{o_1}' = 4.7 \text{ K}\Omega.$$

Therefore,

$$\omega_2 = \frac{1}{C_2(209,000 + 4700)} = 500 \qquad\qquad [6.1]$$

$$C_2 \cong 0.0094 \ \mu\text{f}.$$

With R_{E_2} unby-passed, C_2 is conveniently small. However the second-stage gain is considerably reduced.

PROBLEM 6.6   Refer to the two-stage common-emitter amplifier of Fig. 6.7. Calculate C_2 so that low-frequency gain is 3 db down at $\omega = 500$ radians/sec. Also calculate the voltage gain from point A to V_o. Use approximate methods where applicable in order to simplify calculations.

Solution: The starting point is the calculation of R_{o_1} and R_{i_2}. We may make some simple approximations without significant loss of accuracy. Generally, for $R_L \leq 5 \text{ K}\Omega$,

$$R_{i_2} \cong r_b + (r_e + R_E)(1 + \beta).$$

Estimate the value of r_e from the d-c emitter current, I_{E_2}. The bias at point B is estimated by considering R_1 and R_2 as components of a voltage divider across V_{CC}:

$$\text{Bias at } B \cong \frac{R_2}{R_1 + R_2} \, V_{CC} = \frac{20}{80 + 20} \times 25 = 5 \text{ v}.$$

(This neglects base current in Q_2.) Assuming a 0.6 v base-to-emitter voltage drop in Q_2 (a value characteristic of silicon transistors at room temperature),

$$V_{E_2} = 5 - 0.6 = 4.4 \text{ v}.$$

Emitter current is readily found:

$$I_{E_2} = \frac{4.4}{500 + 1000} \cong 2.9 \text{ ma}.$$

From (1.11),

$$r_e = \frac{0.026}{I_E} = \frac{26}{2.9} \cong 9 \ \Omega.$$

This value may indeed be neglected when added in series with the unby-passed component of emitter resistance $R_{E_{2a}}$. Also, r_b is a negligible portion of R_{i_2}. Hence,

$$R_{i_2} \cong R_{E_{2a}}(1 + \beta) = (500)(101) = 50,500 \ \Omega.$$

For the output impedance of the first stage, it is usually safe to ignore the output impedance of the transistor entirely and let $R_{o_1} \cong R_{L_1} = 5 \text{ K}\Omega$.
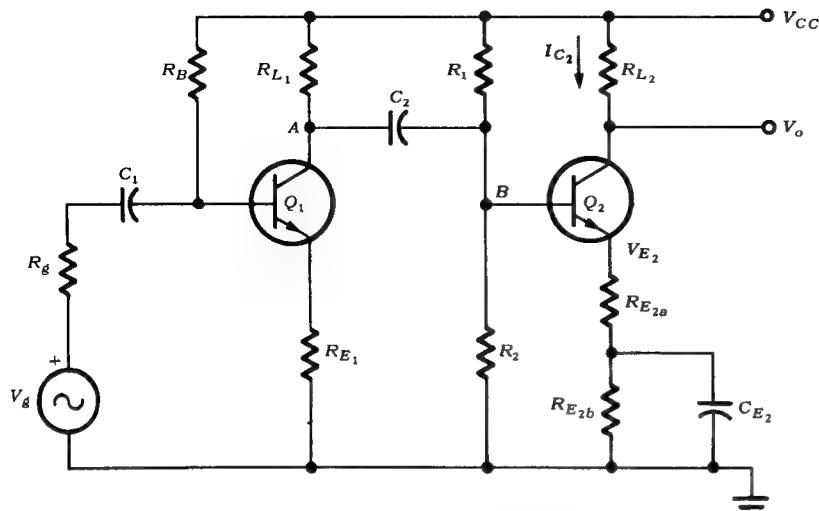
$$V_{CC} = 25\,\text{v} \qquad R_B = 680\,\text{K}\Omega$$
$$C_1 = C_{E_2} = \infty \qquad R_g = 1\,\text{K}\Omega$$
$$C_2 \text{ (to be determined)} \qquad R_{E_1} = 1.5\,\text{K}\Omega$$
$$\beta_1 = \beta_2 = 100 \qquad R_{E_{2a}} = 500\,\Omega$$
$$R_1 = 80\,\text{K}\Omega \qquad R_{E_{2b}} = 1\,\text{K}\Omega$$
$$R_2 = 20\,\text{K}\Omega \qquad R_{L_1} = R_{L_2} = 5\,\text{K}\Omega$$

Fig. 6.7 Two-stage common-emitter amplifier with emitter bias resistors only partially by-passed.

Fig. 6.8 Simplified Thevenin's equivalent of interstage coupling circuit. (See Fig. 6.7.)

The interstage equivalent circuit takes the form shown in Fig. 6.8. Note that resistor R_p represents the bias resistors R_1 and R_2 in parallel:

$$R_p = \frac{20 \times 80}{100}\,\text{K} = 16\,\text{K}\Omega.$$

This must be added in parallel with R_{l_2}:

$$\frac{16 \times 50.5}{66.5} \cong 12\,\text{K}\Omega.$$

To find the 3 db point on the low-frequency gain characteristic,

$$\omega_2 = \frac{1}{C_2(12,000 + 5000)} = 500,$$

$$C_2 = \frac{1}{17,000 \times 500} \cong 0.12\,\mu\text{f}.$$

Returning to Fig. 6.7, the next step is to calculate the voltage gain from point A to V_o. The gain from the base of Q_2 to V_o is given approximately as

$$\frac{R_L}{R_E} = \frac{5000}{500} = 10. \qquad [3.52]$$

(Note that if the second stage emitter by-pass capacitor were not "infinite" at this frequency, the input impedance would be complex, and even approximate calculations would be difficult.)

At the corner frequency ω_2, the network attenuation is $\sqrt{2}/2 = 0.707$, so that voltage gain from A to V_o is $0.707 \times 10 \cong 7$, at a leading phase angle of $45°$.

PROBLEM 6.7 For the two-stage common-emitter amplifier of Fig. 6.7, let $C_2 = \infty$ and $C_{E_2} = 5\,\mu\text{f}$. All other parameters are as in Prob. 6.6. Calculate

voltage gain from point A to V_o as a function of frequency. Specifically, calculate gain for $\omega = 300$ rad/sec, $\omega \cong 0$, and $\omega \cong \infty$. Plot on logarithmic coordinates so that the frequency response shows the characteristic low- and high-frequency asymptotes. Use approximation methods where possible to simplify calculations.

Solution: As before, the problem must be set up in terms of the output impedance of the first stage, and the input impedance of the second stage. The output impedance is approximately equal to $R_{L_1} = 5\,\mathrm{K}\Omega$, as in the previous problem. The input impedance to the second stage is approximately equal to the emitter impedance multiplied by $\beta + 1$ (see Table 5.1). The equivalent input impedance is represented in Fig. 6.9, where the relatively small emitter resistance is neglected.

Figure 6.10 shows the circuit of the interstage coupling elements. Resistance R_p is the equivalent parallel resistance of the two bias resistors. This circuit allows the calculation of base current I_{b_2} in Q_2, from which collector current and gain may be calculated.

Calculate the impedances of Fig. 6.10, and simplify. The emitter impedance of Q_2 is

Fig. 6.9 Equivalent emitter circuit impedance. (See Prob. 6.7.)

$$(1 + \beta)\left(\frac{R_{E_{2b}} \times \dfrac{1}{j\omega C_{E_2}}}{R_{E_{2b}} + \dfrac{1}{j\omega C_{E_2}}}\right) + (1 + \beta)R_{E_{2a}}.$$

This simplifies to

$$(1 + \beta)\frac{R_{E_{2b}}}{1 + j\omega C_{E_2} R_{E_{2b}}} + (1 + \beta)R_{E_{2a}}.$$

Apply Thevenin's theorem to Fig. 6.10, replacing the network driving the above impedance with a simpler equivalent series network:

$$R_{eq} = R_p \| R_{L_1} = \frac{R_p \times R_{L_1}}{R_p + R_{L_1}},$$

$$V_{eq} = V_A \frac{R_p}{R_p + R_{L_1}}.$$

Fig. 6.10 Interstage coupling circuit set up for calculation. (See Prob. 6.7.)

The current I_{b_2} is easily calculated:

$$I_{b_2} = \frac{V_{eq}}{R_{eq} + (1 + \beta)R_{E_{2a}} + (1 + \beta)\dfrac{R_{E_{2b}}}{1 + j\omega C_{E_2} R_{E_{2b}}}}$$

$$= \frac{V_{eq}(1 + j\omega C_{E_2} R_{E_{2b}})}{(1 + \beta)R_{E_{2b}} + [1 + j\omega C_{E_2} R_{E_{2b}}][R_{eq} + (1 + \beta)R_{E_{2a}}]}. \tag{6.2}$$

This can be put into a convenient standard form for plotting:

$$I_{b_2} = \frac{\dfrac{V_A R_p (1 + j\omega C_{E_2} R_{E_{2b}})}{(R_p + R_{L_1})[R_{eq} + (1 + \beta)(R_{E_{2a}} + R_{E_{2b}})]}}{1 + \left[\dfrac{R_{eq} + (1 + \beta)R_{E_{2a}}}{R_{eq} + (1 + \beta)(R_{E_{2a}} + R_{E_{2b}})}\right]j\omega C_{E_2} R_{E_{2b}}}. \tag{6.3}$$

Let

$$\omega_a = \frac{R_{eq} + (1 + \beta)(R_{E_{2a}} + R_{E_{2b}})}{[R_{eq} + (1 + \beta)R_{E_{2a}}](C_{E_2} R_{E_{2b}})}, \tag{6.4}$$

$$\omega_b = \frac{1}{C_{E_2} R_{E_{2b}}}, \tag{6.5}$$

$$B = \frac{(R_p + R_{L_1})[R_{eq} + (1 + \beta)(R_{E_{2a}} + R_{E_{2b}})]}{R_p}. \tag{6.6}$$

Substitute these new parameters in (6.3);

$$\frac{I_{B_2}}{V_A} = \frac{1}{B} \frac{1 + j\dfrac{\omega}{\omega_b}}{1 + j\dfrac{\omega}{\omega_a}}. \tag{6.7}$$

This is the desired form for plotting the frequency response of a network. Appendix C describes the plotting techniques based upon the use of asymptotes on *log-log coordinates.*

Now continue by determining V_o as a function of I_{b_2} to arrive at an expression for gain as a function of frequency. From Table 5.1,

$$I_{c_2} \cong \frac{\beta I_{b_2}}{1 + \dfrac{R_L}{r_d}} \cong \beta I_{b_2},$$

$$\frac{V_o}{V_A} = \frac{\beta I_{b_2} R_{L_2}}{V_A}. \tag{6.8}$$

Substituting (6.7) in (6.8),

$$\frac{V_o}{V_A} = \frac{\beta R_{L_2}}{B} \left(\frac{1 + j\dfrac{\omega}{\omega_b}}{1 + j\dfrac{\omega}{\omega_a}} \right). \tag{6.9}$$

This is the required expression for gain as a function of frequency.

The plot of V_o/V_A on log-log paper appears as shown in Fig. 6.11. This is a generalized plot of amplifier low-frequency gain as affected by capacitor C_{E_2}. Of course, at *very* low frequencies, the coupling capacitors of Fig. 6.7, presently assumed infinite, become significant.

Now substitute numerical values from Fig. 6.7 in the expression for gain:

$$R_p = R_1 \| R_2 = 16 \text{ K}\Omega \text{ (as determined in Prob. 6.5)},$$

$$R_{eq} = R_p \| R_{L_1} = \frac{16 \times 5}{16 + 5} = 3.81 \text{ K}\Omega,$$

$$B = \frac{(R_p + R_{L_1})}{R_p} [R_{eq} + (1 + \beta)(R_{E_{2a}} + R_{E_{2b}})]. \tag{6.6}$$

Hence,

$$B = \frac{16 + 5}{16} [3810 + (101)(1500)]$$

$$= \frac{21}{16} \times 155,300 = 204,000,$$

$$\omega_b = \frac{1}{R_{E_{2b}} C_{E_2}} = \frac{10^6}{1000 \times 5} = 200 \text{ rad/sec},$$

$$\omega_a = \frac{R_{eq} + (1 + \beta)(R_{E_{2a}} + R_{E_{2b}})}{[R_{eq} + (1 + \beta)R_{E_{2a}}]C_{E_2} R_{E_{2b}}}. \tag{6.4}$$
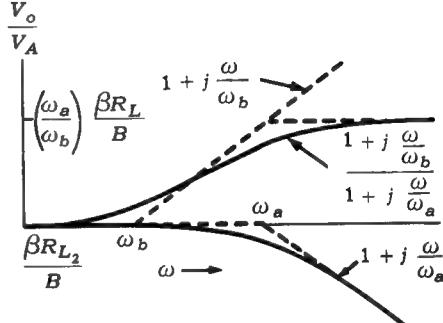

Fig. 6.11 Gain vs. ω on log-log scales. The asymptotes are shown as dashed lines; the actual curves are shown as solid lines. (See Prob. 6.7.) Note that

$$\frac{V_o}{V_A} = \frac{\beta R_{L_2}}{B} \frac{1 + j\dfrac{\omega}{\omega_b}}{1 + j\dfrac{\omega}{\omega_a}}.$$

Substituting previously determined values for the numerator and $1/(C_{E_2} R_{E_{2b}})$, the expression for ω_a becomes

$$\omega_a = \frac{155,300 \times 200}{[R_{eq} + (1 + \beta) R_{E_{2a}}]}.$$

The bracketed term in the denominator is

$$3810 + (101)(500) = 54,300.$$

Therefore,

$$\omega_a = \frac{155,300 \times 200}{54,300} = 572 \text{ rad/sec.}$$

Substituting the above values in the expression for gain,

$$\frac{V_o}{V_A} = \frac{\beta R_{L_2}}{B} \frac{1 + j \dfrac{\omega}{\omega_b}}{1 + j \dfrac{\omega}{\omega_a}} = \frac{(100)(5000)}{204,000} \frac{1 + j \dfrac{\omega}{200}}{1 + j \dfrac{\omega}{572}} \qquad [6.9]$$

$$= 2.45 \frac{1 + j \dfrac{\omega}{200}}{1 + j \dfrac{\omega}{572}}.$$

This is the final numerical expression for gain variation in the region where C_{E_2} is most sensitive to frequency change. The responses for $\omega \cong 0$, $\omega = 300$ rad/sec, and $\omega \cong \infty$ will now be calculated:

At $\omega \cong 0$,

$$\frac{V_o}{V_A} = 2.45.$$

At $\omega = 300$ rad/sec,

$$\frac{V_o}{V_A} = 2.45 \frac{1 + j \dfrac{300}{200}}{1 + j \dfrac{300}{572}},$$

$$\left| \frac{V_o}{V_A} \right| = 2.45 \times 1.6 = 3.92.$$

As $\omega \cong \infty$,

$$\frac{V_o}{V_A} \cong 2.45 \times \frac{\dfrac{1}{200}}{\dfrac{1}{572}} = 2.45 \times \frac{572}{200} = 7.0.$$

Refer to Fig. 6.11 for the plot of gain vs. frequency.

The preceding problems have shown how C_2, an interstage coupling capacitor, and C_{E_2}, an emitter resistor by-pass capacitor, individually affect frequency response. For reasons which have been previously explained, the separate effects cannot be superimposed unless the significant frequencies associated with each capacitor are widely separated. A really accurate investigation of the combined effects of two capacitors, such as C_2 and C_{E_2}, requires an equivalent circuit analysis of both stages together, taking into account all interactions.

PROBLEM 6.8 In the circuit of Fig. 6.7, if C_2 and $C_{E_2} = 5 \,\mu f$, $C_1 = 50 \,\mu f$, and all other values are unchanged, show the exact tee-equivalent circuit for determining V_o/V_g.

Solution: Figure 6.12 shows the common-emitter tee-equivalent circuit to be used for computing the gain, and the numerical values of the circuit parameters applicable to this problem.
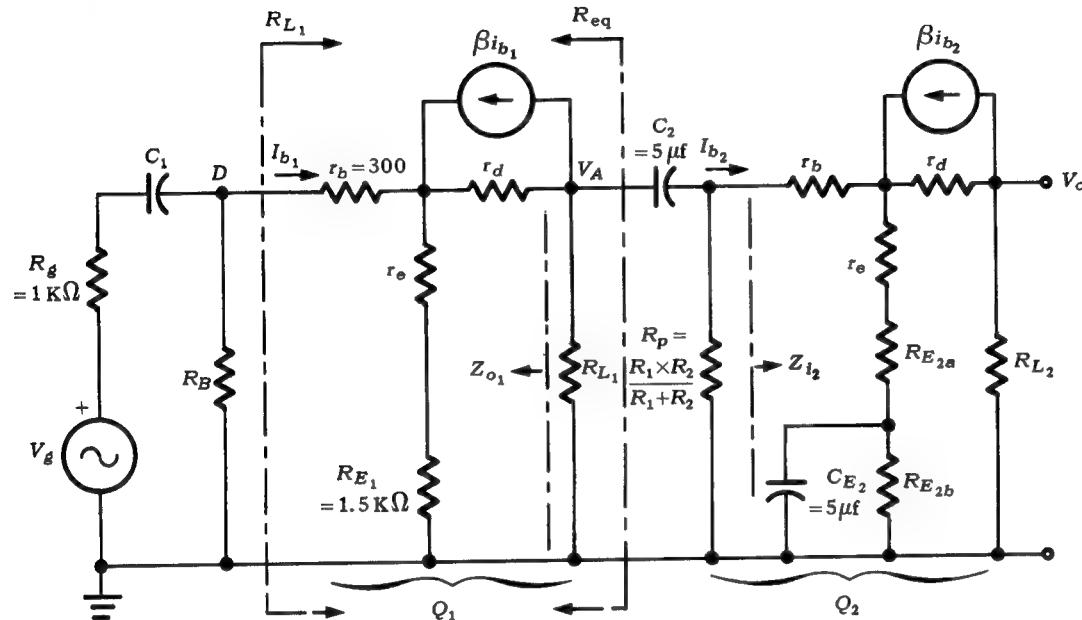
Fig. 6.12 Equivalent circuit of two-stage amplifier. (See Prob. 6.8.) Note that $r_e \ll R_E$, $r_b \ll R_i$, and $r_d \gg R_L$ so that the transistor parameters can be neglected; hence,

$$R_p = \frac{R_1 \times R_2}{R_1 + R_2} = 16 \,\text{K}\,\Omega.$$

PROBLEM 6.9 Using the circuit (Fig. 6.12) of Prob. 6.8 and formulae from Table 5.1, calculate gain V_o/V_g as a function of frequency. Make assumptions and suitable approximations where necessary to simplify calculations. Consider the frequency range from 1 cps to 10,000 cps.

Solution: Calculate the input resistance of the first stage. Neglecting loading by the second stage,

$$R_{i_1} \cong r_b + (r_e + R_{E_1})(1 + \beta) \frac{1 + \dfrac{R_L}{r_c}}{1 + \left(\dfrac{R_L + R_E + r_e}{r_c} \right)(1 + \beta)}$$

$$= 300 + (1509)(101) \frac{1 + 0.0005}{1 + 0.06} = 144 \,\text{K}\Omega.$$

Note that the terms in the expression for R_{i_1}, which include R_L, actually have less than a 6% influence on the result of the calculation. It is not necessary to know R_L to a high degree of accuracy in order to determine R_{i_1}. This is fortunate since the *effective* R_L is equivalent to R_{L_1} in parallel with the effective frequency-sensitive impedance to the right of R_{L_1} in Fig. 6.12. An exact computation would be extremely tedious.

(a)

(b)

Fig. 6.13 (a) Equivalent input circuit. (b) Thevenin's equivalent circuit for the first amplifier stage. (See Prob. 6.9.)
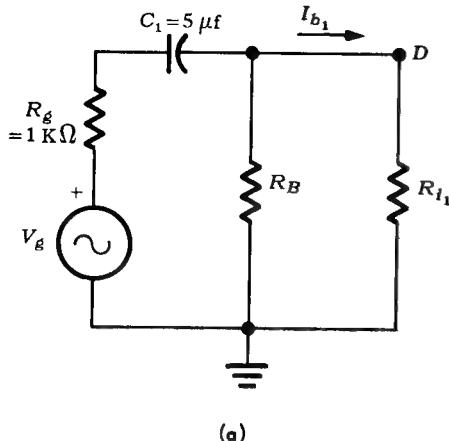
For $R_{i_1} = 144$ KΩ, we can calculate the attenuation characteristics of the first stage input circuit. Refer to the equivalent input circuit in Fig. 6.13a. The gain of this circuit falls 3 db at that frequency where the capacitive reactance equals the equivalent series resistance:

$$\frac{1}{\omega_o C_1} = R_g + \frac{R_{i_1} R_B}{R_{i_1} + R_B}.$$

Now substitute numerical values and solve:

$$\frac{1}{\omega_o C_1} = 1 + \frac{(144)(680)}{144 + 680} \approx 121 \text{ K}\Omega.$$

For $C_1 = 50$ μf, $\omega_o = 2\pi f_o = 1/6$ rad/sec and $f_o = 0.027$ Hz. At $f = 1$ Hz, the capacitive reactance is relatively small (3170 Ω). Its attenuating effect on gain is therefore negligible in the frequency range of interest.

Thevenin's theorem is readily applied, replacing the first stage by its open-circuit output voltage, V_A, and its equivalent output impedance, R_{o_1}:

$$R_{o_1} \cong r_d \left(1 + \frac{\beta}{1 + \frac{R_g + r_b}{r_e + R_E}} \right).$$

Substituting numerical values,

$$R_{o_1} \cong 100,000 \left(1 + \frac{100}{1 + \frac{1300}{1509}} \right) \cong 5.5 \text{ M}\Omega.$$

This is much greater than R_{L_1}, and the *effective* output impedance R_{eq} is therefore approximately equal to $R_{L_1} = 5$ KΩ; hence, voltage gain from (3.52) is

$$A_v = \frac{V_A}{V_D} \cong \frac{R_L}{r_e + R_{E_1}} = \frac{5000}{1509} = 3.15.$$

This figure for voltage gain must be multiplied by the attenuation of the input network to determine the over-all gain of the first stage:

$$V_D = V_{eq} \frac{R_{i_1} \| R_B}{R_{i_1} \| R_B + R_g},$$

where $R_{i_1} \| R_B$ is the equivalent parallel resistance of R_{i_1} and R_B. Therefore,

$$V_D = V_g \frac{120,000}{121,000} = 0.995 \, V_g.$$

Substituting,

$$\frac{V_A \text{ (open circuit)}}{V_g} = 3.15 \times 0.995 = 3.13.$$

The first stage can be replaced by the equivalent network shown in Fig. 6.13b.

Now calculate the input impedance of the second stage:

$$Z_{i_2} = r_b + \left(R_{E_{2a}} + R_{E_{2b}} \left\| \frac{1}{j\omega C_{E_2}} \right. \right)(1 + \beta) \left(\frac{1 + \frac{R_L}{r_c}}{1 + \frac{R_L + R_{E_{2a}} + R_{E_{2b}} \left\| \frac{1}{j\omega C_{E_2}} \right.}{\frac{r_c}{1 + \beta}}} \right).$$

The term in the last pair of brackets is

$$\frac{1 + 0.0005}{1 + \dfrac{5500 + \dfrac{R_{E_{2b}}}{1 + j\omega\, C_{E_2} \times R_{E_{2b}}}}{99,000}}.$$

The expression

$$\frac{R_{E_{2b}}}{1 + j\omega\, C_{E_2} \times R_{E_{2b}}}$$

can never exceed $R_{E_{2b}} = 1\ K\Omega$. Thus, the entire bracketed expression merely introduces an approximately 6.5 % reduction in the value of Z_{i_2}. In the interest of simplicity, this entire bracketed expression will therefore be neglected, so that

$$Z_{i_2} \cong r_b + \left(R_{E_{2a}} + R_{E_{2b}} \left\|\, \frac{1}{j\omega\, C_{E_2}} \right.\right)(1 + \beta).$$

The simplified equivalent circuit for the two-stage amplifier is shown in Fig. 6.14. The voltage at point A is the output of the first stage when loaded by the second stage. It is straightforward, though somewhat tedious, to determine I_{b_2} over the frequency range. From I_{b_2}, the output voltage V_o, and therefore the over-all voltage gain, are determined.

As a good approximation, current gain of the second stage is (Table 5.1)

$$A_i \cong \frac{\beta}{1 + \dfrac{R_{L_2}}{r_d}}$$

or

$$A_i \cong \frac{100}{1 + 0.05} = 95,$$

so that

$$\frac{V_o}{I_{b_2}} = A_i R_L = 95 \times 5000 = 475,000.$$

The frequency dependency of the multi-stage amplifier is now confined to the variation of I_{b_2}, determined from Fig. 6.14. To aid in carrying out the calculations, note the principal circuit time constants. As a first approximation, the loading of the first mesh by the high-impedance second mesh across R_p will be neglected. The first mesh time constant T_a equals $(R_{eq} + R_p)C_2 \cong 0.105$ sec. The time constant $T_b = C_{E_2} R_{E_{2b}} = 5 \times 10^{-6} \times 10^3 = 0.005$ sec.
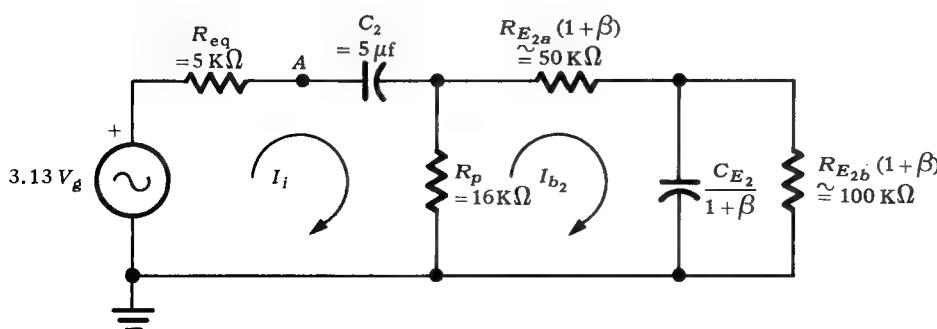

Fig. 6.14 Simplified equivalent circuit of two-stage amplifier. (See Prob. 6.9.)

The wide difference in time constants permits an analytical simplification. At very low frequencies, where T_a is in the range of interest ($\omega \cong 10$ rad/sec), the time constant associated with C_{E_2} has negligible influence. Capacitor C_{E_2} may well be considered open-circuited. At higher frequencies, where T_b is in the range of interest ($\omega \cong 200$ rad/sec), the reactance of C_2 may be considered negligible. *The circuit therefore can be treated as though it contained two separate and isolated time constants.*

The circuit of Fig. 6.14 is most easily solved by considering the various frequency ranges of interest separately. At *very* low frequencies, C_{E_2} is essentially open-circuited, and

$$I_1 \cong \frac{3.13\,V_g}{\dfrac{1}{j\omega\,C_2}} = 3.13\,j\omega\,C_2\,V_g\,,$$

$$I_{b_2} = I_1 \frac{R_p}{R_p + (R_{E_{2a}} + R_{E_{2b}})(1 + \beta)}$$

$$= \frac{3.13\,V_g\,j\omega\,C_2\,R_p}{R_p + (R_{E_{2a}} + R_{E_{2b}})(1 + \beta)}$$

$$= \frac{3.13\,V_g\,j\omega \times 16{,}000 \times 5 \times 10^{-6}}{16{,}000 + (101)(1500)}$$

$$= 1.5\,j\omega\,V_g\,\mu\mathrm{a}.$$

At a somewhat higher frequency, where C_2 is negligible while C_{E_2} is still regarded as an open-circuit, I_{b_2} is easily calculated from the all-resistive network as $I_{b_2} = 15.4\,V_g\,\mu\mathrm{a}$.

At higher frequencies, both capacitors act as short-circuits. Solving again for I_{b_2},

$$I_{b_2} = \frac{3.13\,V_g}{5000 + 16{,}000\,\|\,50{,}000} \times \frac{16}{50}$$

$$= 58.1\,V_g\,\mu\mathrm{a}.$$

Consider now the *intermediate* frequency range, where C_2 is essentially a short-circuit, while C_{E_2} is not. Apply Thevenin's theorem to eliminate the first mesh. Figure 6.15 shows the simplified form where the reactance of C_2 is taken as zero. This circuit is easy to solve for I_{b_2}. First determine the impedance of $0.05\,\mu\mathrm{f}$ in parallel with $100\,\mathrm{K}\Omega$:
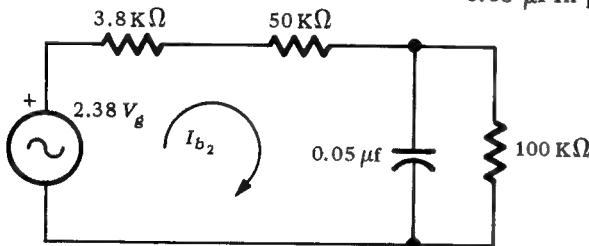
Fig. 6.15 Simplified Thevenin's equivalent circuit, with reactance of C_2 essentially zero. (See Prob. 6.9.)

$$Z_p = \frac{100{,}000 \times \dfrac{1}{j\omega\,0.05 \times 10^{-6}}}{100{,}000 + \dfrac{1}{j\omega\,0.05 \times 10^{-6}}}$$

$$= \frac{100{,}000}{1 + j\omega\,0.005}\,.$$

Now solve for I_{b_2}:

$$I_{b_2} = \frac{2.38\,V_g}{53{,}800 + \dfrac{100{,}000}{1 + j\omega\,0.005}}$$

$$= \frac{15.4\,V_g\,(1 + j\omega\,0.005)}{1 + j\omega\,0.00175}\,\mu\mathrm{a}.$$

Recalling that $V_o/I_{b_2} = 475,000$, we now have sufficient data to sketch the amplifier attenuation characteristics. This is most easily done by a plot on logarithmic coordinates as in Fig. 6.16.

Note that this problem was substantially simplified by the separation of time constants, T_a and T_b. This allowed us to consider the separate frequency regions independently. If these were not separated by about a factor of 10, more precise calculation methods based upon the formal solution of the network of Fig. 6.14 would be required. A more accurate solution is necessary only when a simplified sketch based on asymptotes and corner frequencies is insufficient. Usually, the simplified sketch is quite satisfactory.

PROBLEM 6.10 If, in the two-stage amplifier of Prob. 6.9, C_2 is changed to 0.25 μf, all other parameters remaining the same, find the attenuation characteristics of the amplifier over the region where C_2 and C_{E_2} have significant reactances.

Solution: The time constant due to C_2 has been reduced by a factor of about 20, so that both capacitors influence amplifier gain over approximately the same frequency range. An accurate loop analysis is necessary to determine the effective circuit time constants. Referring to Fig. 6.14, the mesh equations are

$$3.13 \, V_g = \left(21,000 + \frac{10^6}{0.25 \, j\omega}\right) I_1 - 16,000 \, I_{b_2},$$

$$0 = -16,000 \, I_1 + \left(66,000 + \frac{100,000}{1 + j\omega \, 0.005}\right) I_{b_2}.$$

These equations may be solved for I_{b_2} by eliminating I_1 (or with determinants), leading to the following simplified solution:

$$I_{b_2} = 0.075 \, V_g \frac{j\omega \left(1 + j \dfrac{\omega}{200}\right)}{\left(1 + j \dfrac{\omega}{192}\right)\left(1 + j \dfrac{\omega}{612}\right)} \, \mu a.$$

Calculating output voltage,

$$V_o = A_i R_L I_{b_2} = 95 \times 5000 \, I_{b_2}$$

$$= 475,000 \, I_{b_2}.$$

Substituting the expression for I_{b_2}, and solving for voltage gain,

$$A_v = \frac{V_o}{V_g}$$

$$= 0.0355 \frac{j\omega \left(1 + j \dfrac{\omega}{200}\right)}{\left(1 + j \dfrac{\omega}{192}\right)\left(1 + j \dfrac{\omega}{612}\right)}.$$

This is the required expression for gain as a function of frequency.

Certain deductions may be drawn by observing and comparing the results of Probs. 6.9-10. The high frequency gain, where capacitive reactances are negligible, is unchanged by our approximations. The approximate method of con-
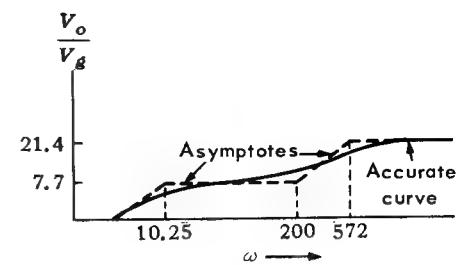
$$\frac{V_o}{V_g} = \frac{0.746 \, j\omega \left(1 + j \dfrac{\omega}{200}\right)}{\left(1 + j \dfrac{\omega}{10.25}\right)\left(1 + j \dfrac{\omega}{572}\right)}$$

Fig. 6.16 Asymptotic diagram and accurate curve of output voltage vs. frequency. (See Prob. 6.9.)

sidering corner frequencies individually, leads to somewhat erroneous values for these frequencies, but the inaccuracies are rarely important in practical amplifier design.

6.3 Transformer Coupling

Transformer coupling between the stages of a transistor amplifier offers significant advantages such as:

1. Good bias stability.
2. Simple impedance matching for optimum power gain.
3. Isolation of stages.

The disadvantages are:

1. Relative high cost.
2. Bulk and weight.
3. Limited frequency range.
4. Nonlinearity, due to nonlinear magnetic core.

The most significant advantages have to do with *impedance matching*.

The *equivalent circuit* of the transformer is a linear network which represents the transformer in a convenient manner for purposes of calculation, as illustrated in Fig. 6.17. The figure also defines all symbols for use in this section. The idealized output transformer at the output terminals of the equivalent circuit provides the required amplifier impedance matching.
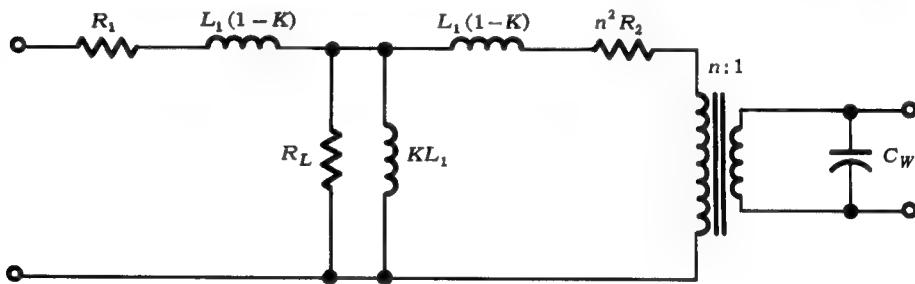

Fig. 6.17 Transformer equivalent circuit. Note that R_1 = primary d-c resistance; R_2 = secondary d-c resistance; n = primary/secondary turns ratio; L_1 = primary inductance; K = coefficient of coupling of primary to secondary; KL_1 = mutual inductance, primary to secondary; $(1-K)L_1$ = leakage inductance, primary or secondary; R_L = equivalent core loss resistor; C_w = equivalent distributed capacitance referred to secondary winding. Leakage inductance L_1 is measured with the secondary open-circuited; secondary inductance L_2 can be measured with the primary open-circuited: $L_1 = n^2L_2$; R_L is relatively independent of frequency except at frequencies in the low audio range; K is usually slightly less than unity.

PROBLEM 6.11 For the circuit of Fig. 6.18a, determine the variation of gain with frequency. (The transformer is effectively coupling a driving source R_{o_1} to an output load R_{i_2}.)

Solution: In complex problems of this type, it is most convenient to carry out separate calculations for the low- and high-frequency regions. Consider first the low-frequency region. Since $K \cong 1$ for a reasonably efficient transformer,

$$\omega L_1(1-K) \ll R_1, \ n^2 R_2$$

at very low frequencies (ω small); thus the series inductance terms may be neglected. Similarly, for very small ω, the R_L term may be ignored in comparison with the reactance of KL_1. Also, the capacitive reactance C_w becomes very large,
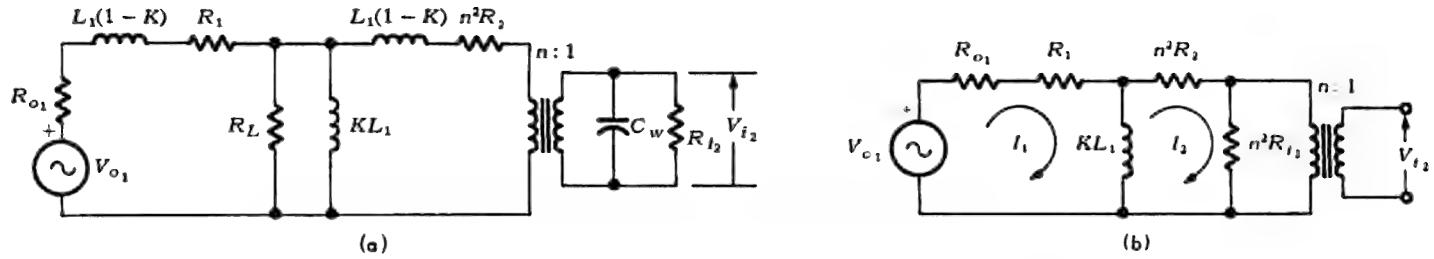
Fig. 6.18 (a) Equivalent circuit showing an interstage transformer coupling the output of one stage to the input of the next. (b) Simplified equivalent circuit for low-frequency condition.

and may therefore be neglected. The simplified equivalent circuit corresponding to low-frequency operation takes the form of Fig. 6.18b.

Now using Thevenin's theorem,

$$
\frac{V_{i_2}}{V_{o_1}} = \frac{\dfrac{jK\omega L_1}{(R_1 + R_{o_1}) + jK\omega L_1} \times n^2 R_{i_2}\left(\dfrac{1}{n}\right)}{\dfrac{(R_1 + R_{o_1})(jK\omega L_1)}{(R_1 + R_{o_1}) + jK\omega L_1} + n^2(R_2 + R_{i_2})}
$$

$$
= \frac{jK\omega L_1 n R_{i_2}}{(R_1 + R_{o_1})(jK\omega L_1) + n^2(R_2 + R_{i_2})[(R_1 + R_{o_1}) + jK\omega L_1]}
$$

$$
= \frac{jK\omega L_1 n R_{i_2}}{n^2(R_2 + R_{i_2})(R_1 + R_{o_1}) + jK\omega L_1[n^2(R_2 + R_{i_2}) + (R_1 + R_{o_1})]}
$$

$$
= \frac{\dfrac{jK\omega L_1 R_{i_2}}{n(R_2 + R_{i_2})(R_1 + R_{o_1})}}{1 + jK\omega L_1\left[\dfrac{1}{R_1 + R_{o_1}} + \dfrac{1}{n^2(R_2 + R_{i_2})}\right]}
$$

$$
= \frac{\dfrac{jK\omega L_1 R_{i_2}}{n(R_2 + R_{i_2})(R_1 + R_{o_1})}}{1 + jK\omega L_1\left[\dfrac{(R_1 + R_{o_1}) + n^2(R_2 + R_{i_2})}{(R_1 + R_{o_1})n^2(R_2 + R_{i_2})}\right]} . \tag{6.10}
$$

Equation (6.10) shows the output increasing uniformly with frequency, and then leveling off as the second term in the denominator becomes dominant. The corner frequency, where attenuation begins to level off with increasing frequency, occurs where

$$
\omega = \frac{1}{KL_1}\left[\frac{(R_1 + R_{o_1})n^2(R_2 + R_{i_2})}{(R_1 + R_{o_1}) + n^2(R_2 + R_{i_2})}\right].
$$

Above this corner frequency, the frequency-sensitive term in the denominator of (6.10) becomes dominant. In this *intermediate* or *mid-frequency* range,

$$
\frac{V_{i_2}}{V_{o_1}} = \frac{n R_{i_2}}{(R_1 + R_{o_1}) + n^2(R_2 + R_{i_2})}.
$$

The equivalent circuit for the mid-frequency range is given in Fig. 6.19, which yields V_{i_2}/V_{o_1} almost by inspection. Frequency response is flat in this region, which is generally the useful operating region of the transistor amplifier.
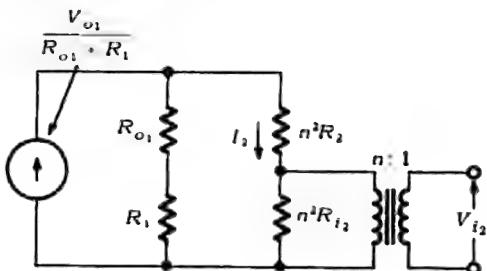
Fig. 6.19 Simplified circuit showing transformer coupling.
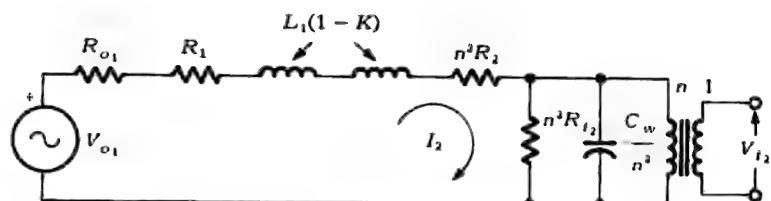
Fig. 6.20 Interstage-coupling equivalent circuit for high-frequency condition. Loading on the transformer output terminals is assumed negligible.

Fig. 6.21 Gain characteristic of a transformer coupling network.

The high-frequency region of the frequency-response characteristic is distinguished by the increasing importance of the series inductors, $L_1(1-K)$. The shunt inductor KL_1 leads to a very high reactance at high frequency, and may be neglected. The equivalent circuit for high-frequency conditions is shown in Fig. 6.20.

For simplicity, capacitance C_w will be neglected for the present. This is usually a practical assumption in transistor circuits, as R_{i_2} generally provides a relatively low-resistance shunt at the upper frequencies of typical matching transformers. From the equivalent circuit, the L/R time constant is determined by inspection:

$$\frac{L}{R} = \frac{2(1-K)L_1}{R_{o_1} + R_1 + n^2(R_{i_2} + R_2)}. \tag{6.11}$$

The corner frequency corresponding to this time constant is

$$\omega = \frac{R_{o_1} + R_1 + n^2(R_{i_2} + R_2)}{2(1-K)L_1}$$

With the upper and lower corner frequencies determined, as well as the level of the intermediate frequency region, the gain characteristic may be plotted on logarithmic coordinates as in Fig. 6.21. Sketches of both asymptotes, as well as the general shape of the gain curve itself, are shown.

Thus far C_w has been ignored. However, it is possible for C_w to series-resonate with the equivalent transformer leakage reactance somewhere in the high-frequency region. Should this be the case, the gain curve is modified to show a characteristic resonant peak (Fig. 6.21), whose amplitude is determined by the "Q" of the circuit. Above this resonant peak, the shunting capacitor acts to attenuate the output even more rapidly than before.

Commercially, K, n, and L_1 are not generally given in transformer catalogs. However, it is often possible to estimate these parameters. For a matching transformer,

$$n = \sqrt{\frac{R_s}{R_L}}, \tag{6.12}$$

where R_s and R_L are the driving and load impedances, respectively, to be matched.

If the lower corner frequency ω_L is given, for $K=1$, $R_1 = R_2 = 0$, and letting $R_{o_1} = R_s$, $R_{i_2} = R_L$ (see Fig. 6.18b),

$$\omega_L = \frac{R_s R_L n^2}{(R_s + n^2 R_L)L_1} = \frac{R_s^2}{2 R_s L_1} = \frac{R_s}{2 L_1},$$

$$L_1 = \frac{R_s}{2\omega_L}. \tag{6.13}$$
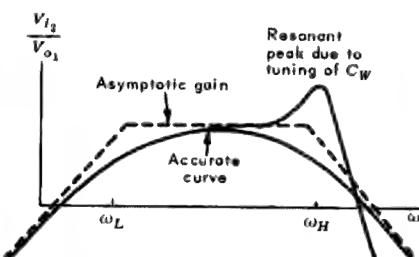
PROBLEM 6.12   A manufacturer's catalog lists the following data on a transformer:

$$R_s = 10,000 \ \Omega,$$

$$R_L = 100 \ \Omega,$$

$$\omega_L = 500 \ \text{rad/sec.}$$

Estimate L_1 and n.

Solution: From (6.12) and (6.13),

$$n = \sqrt{\frac{R_s}{R_L}} = \sqrt{\frac{10,000}{100}} = 10,$$

$$L_1 = \frac{R_s}{2 \ \omega_L} = \frac{10,000}{2 \times 500} = 10 \ \text{h.}$$

Resistors R_1 and R_2 can be measured as the d-c resistances of the transformer windings, or *very roughly* estimated as

$$R_1 \cong \frac{1}{10} R_s,$$

$$R_2 \cong \frac{1}{10} R_L.$$

PROBLEM 6.13   For the circuit of Fig. 6.22, estimate the required transformer primary inductance L_1, such that the low-frequency response is 3 db down at 60 Hz.

Solution: From Table 5.1, the *transistor* output impedance is easily estimated:

$$R_o \cong h_{oe} = 33 \ \text{K} \ \Omega.$$

A simplified but satisfactory equivalent circuit is given in Fig. 6.23a. Figure 6.23b shows the circuit rearranged to simplify determination of the corner frequency. The effective resistance for the computation of corner frequency is 33 K $\Omega \| 3$ K Ω, or 2.75 K Ω.

The lower corner frequency,

$$\omega_L = 2 \pi \ f_L = 2 \pi \times 60 = 377 \ \text{rad/sec.}$$

The time constant of the inductive circuit must equal the reciprocal of ω_L:

$$\frac{L_1}{2750} = \frac{1}{377},$$

$$L_1 = \frac{2750}{377} = 7.3 \ \text{h,}$$

for $I_C = 4$ ma d-c through the transformer primary.

PROBLEM 6.14   Using reasonable approximations for the circuit of Fig. 6.24 at the specified operating conditions, determine

   (a) R_2, for correct bias,
   (b) C_1, for a corner frequency $\omega = 10$ rad/sec,
   (c) output transformer inductance L_1 for a corner frequency, $\omega_L = 200$ rad/sec.
Assume that the d-c resistance of the transformer secondary is 10% of the load resistance.

Solution: For the conditions of Fig. 6.24, $I_E \cong I_C = 10$ ma. The emitter voltage is 1.2 K $\Omega \times 10$ ma $= 12$ v d-c. To compensate for the base-emitter drop, the voltage at the base $V_B \cong 12.6$ v.
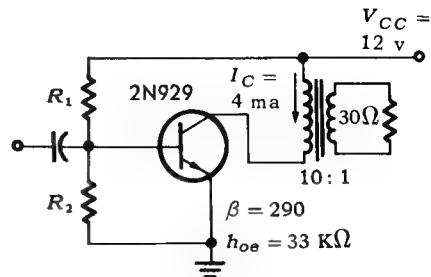

Fig. 6.22 Output transformer to match load in a common-emitter amplifier.
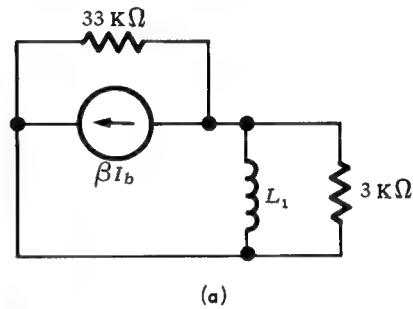

(a)
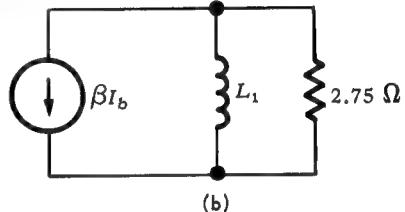
(b)

Fig. 6.23 (a) Simplified equivalent output circuit. (b) Simplified equivalent circuit for estimating corner frequency. (See Prob. 6.13.)
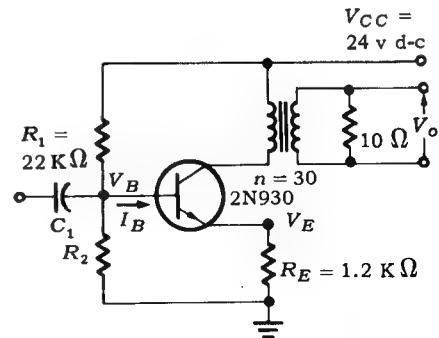

Fig. 6.24 Amplifier circuit with transformer-coupled output. At $I_C = 10$ ma: $\beta = 380$, $r_e = 11 \ \Omega$, $r_b = 700 \ \Omega$, $r_d = 5250 \ \Omega$.

It is convenient to estimate the input impedance R_I of the base circuit. From Table 5.1,

$$R_I \cong (1 + h_{fe}) R_E = 381 \times 1200 = 458 \text{ K } \Omega.$$

Since this high input impedance is in parallel with $R_1 \| R_2$ (where $R_1 = 22$ KΩ) at the base input, it may be neglected without introducing more than a few percent error. Thus, neglecting base current drawn from the voltage divider formed by R_1 and R_2, it is easy to calculate R_2:

$$12.6 = \frac{R_2}{R_1 + R_2} \times 24.$$

Since $R_1 = 22$ K Ω, R_2 is calculated as 24 K Ω.

We can now determine the value of C_1 for a corner frequency of 10 rad/sec. The RC time constant must be 0.1, so that

$$(R_1 \| R_2) \times C_1 = \frac{1}{10},$$

$$R_1 \| R_2 = \frac{22 \times 24}{22 + 24} = 11.5 \text{ K } \Omega,$$

$$C_1 = \frac{1}{10} \times \frac{1}{11,500} = 8.7 \ \mu f.$$

Now examine the transformer in the collector circuit of the transistor. The transistor is effectively a high impedance current source, in comparison with the relatively low load impedance. A simplified but fairly accurate equivalent circuit is shown in Fig. 6.25. The effective time constant is

$$\frac{L_1}{n^2(R_2 + R_L)} \cong \frac{L_1}{9900}.$$

This must equal the inverse of the specified transformer low-frequency corner:

$$\frac{L_1}{9900} = \frac{1}{200},$$

$$L_1 = \frac{9900}{20} \cong 50 \text{ h.}$$

Fig. 6.25 Transformer-coupled equivalent circuit calculation. (See Prob. 6.14.)

PROBLEM 6.15 For the amplifier of Fig. 6.24, estimate voltage gain at $\omega = 200$ rad/sec.

Solution: Neglecting the effect of transformer inductance, from Table 5.1,

$$A_v \cong \frac{R_L}{R_E},$$

where R_L is the effective a-c resistance in the collector circuit. From Fig. 6.25, this is 10,800 Ω. Substituting,

$$A_v = \frac{10,800}{1200} = 9.0.$$

This, however, is the voltage on the primary side of the transformer, reduced on the secondary by a factor of 30 by the transformer step-down ratio. An additional attenuation of 9000/10,800 is introduced by the transformer winding resistance. Further, the gain is reduced by a factor of $\sqrt{2}/2 = 0.707$ at the corner frequency, $\omega_L = 200$ rad/sec. Therefore, the voltage gain at $\omega_L = 200$ rad/sec is

$$\frac{V_o}{V_i}\bigg|_{\omega=200} = 9.0 \times \frac{1}{30} \times \frac{9000}{10,800} \times 0.707 = 0.176.$$

In the design of signal amplifiers (as contrasted with power amplifiers discussed in Chap. 7), it is not only necessary to verify that gain is adequate, but one must also verify that the required "swing" of the output voltage is restricted to the linear region. This problem is important in the output of multi-stage amplifiers.

PROBLEM 6.16 For the circuit of Fig. 6.26, design the bias circuit to permit a distortion-free output voltage of 2 v rms, while keeping the stability factor $S \leq 4$.

Solution: We must determine the range of I_C. For $I_C = 0$, the collector is at a 12 v potential. Recall that 2 v rms corresponds to $2 \times 2\sqrt{2} = 5.66$ v, peak-to-peak. Thus, the collector potential may be as low as $12 - 5.66 = 6.34$ v for peak collector current. This value of peak current $= 5.66/5000 \cong 1.13$ ma.

This reasoning indicates a value of collector bias current of about 0.6 ma, swinging from nearly zero to a value somewhat under 1.2 ma. A load line for this condition is shown in Fig. 6.27.

For the 2N929 transistor, a minimum V_{CE} of 1 v assures satisfactory operation (see Fig. 2.5b). Thus,

$$V_E = V_{CC} - R_L \, I_{C_{max}} - V_{CE_{min}}.$$

Substituting values,

$$V_E = 12 - \left(5000 \times 0.0006 + \frac{5.66}{2}\right) - 1 = 6.17 \text{ v}.$$

Assume, as a convenient approximation that $V_E = 6$ v for the d-c operating level. Since $I_E \cong I_C = 0.6$ ma,

$$R_{E_a} + R_{E_b} = \frac{6}{0.0006} = 10 \text{ K } \Omega.$$

Thus, $R_{E_a} = 500 \ \Omega$ and $R_{E_b} = 9,500 \ \Omega$.

The base voltage is 6 v $+ V_{BE} \cong 6.6$ v. Base current is also easily found:

$$I_B = \frac{I_C}{\beta} = \frac{0.6 \times 10^{-3}}{300} \cong 2 \ \mu\text{a}.$$

From (4.16),

$$S \cong 1 + \frac{R_p}{R_E}.$$

For $S = 4$,

$$\frac{R_p}{R_E} = 3, \qquad R_p = 30 \text{ K } \Omega.$$

If we assume that the 2 μa of base current is negligible compared with the current drawn by the R_1, R_2 divider, then

$$\frac{R_2}{R_1 + R_2} \, V_{CC} = 6.6 \text{ v}.$$

However,

$$R_p = \frac{R_1 \, R_2}{R_1 + R_2}.$$

$$R_{E_a} = 500 \ \Omega$$
$$r_e = 10 \text{ M} \Omega$$
$$\beta = 300$$
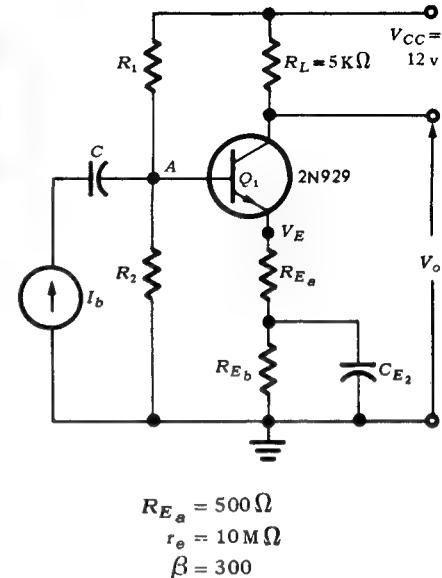
Fig. 6.26 Load line superimposed on idealized collector characteristics. (See Prob. 6.16.)
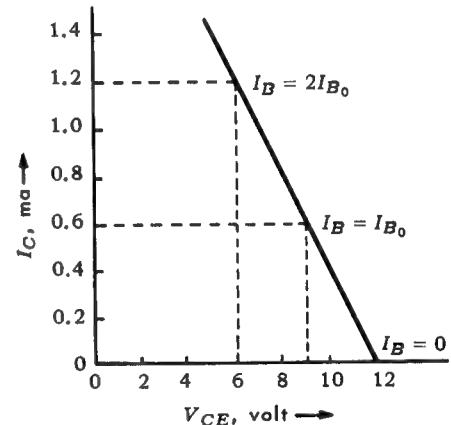

Fig. 6.27 Load line superimposed on idealized collector characteristics. (See Prob. 6.16.)

Substituting,

$$\frac{R_p}{R_1} V_{CC} = 6.6 \text{ v.}$$

Solving, using known values,

$$R_1 = 54.5 \text{ K } \Omega,$$

$$R_2 = 66.5 \text{ K } \Omega.$$

It may be verified, if desired, that divider current is much greater than base input current.

PROBLEM 6.17 If, in Fig. 6.26, a large capacitance is connected from the output terminal to ground, what is the maximum undistorted rms capacitance current?

Solution: Since bias current is 0.6 ma, this is the maximum instantaneous peak collector current that can flow without the collector current actually reaching zero. Therefore,

$$I_{o_{rms}} = \frac{0.6}{\sqrt{2}} = 0.424 \text{ ma rms.}$$

PROBLEM 6.18 In Prob. 6.13 (Fig. 6.22), what is the maximum undistorted voltage across the transformer primary?
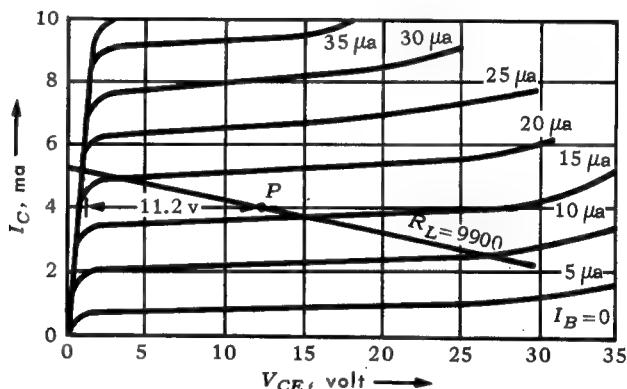
Fig. 6.28 Collector characteristics with superimposed
load line for the circuit of Fig. 6.22.

Solution: The transformer primary voltage measured at the collector can theoretically vary from 0 to 24 v, since the voltage may be either plus or minus (see Fig. 6.28). However, since the transistor drop V_{CE} must not be less than 1 v and the collector current not be allowed to go to zero, the distortion-free primary voltage can typically vary from 1 v to 23 v.

Actually, referring to Fig. 6.28, $V_{min} = 0.8$ v, so that the full sinusoidal voltage swing is $2 \times 11.2 = 22.4$ v peak-to-peak, or 7.85 v rms.

6.4 Direct Coupling

Direct coupling of amplifier stages leads to the following advantages:
1. It avoids large coupling capacitors, and does not limit the low-frequency response or allow low-frequency phase-shift.
2. Quiescent output voltages provide input bias to subsequent stages, avoiding bias networks. This allows higher base-circuit input impedances.

3. Feedback around several stages can lead to bias stability factors, S, less than unity.

In this section, we will examine some two- and three-transistor direct-coupled amplifiers, which may then be cascaded, as desired, using a-c coupling methods.

PROBLEM 6.19 Making reasonable assumptions, analyze the circuit of Fig. 6.29 for the variation of I_{C_2} due to changes in leakage current I_{CBO} with temperature.

Solution: This is a two-stage direct-coupled amplifier with d-c feedback from the emitter circuit of the second stage to the input of the first stage. Now first examine the nature of the feedback itself. If I_{CBO_2} increases, the emitter current of Q_2 increases correspondingly, thus increasing the base voltage of Q_1. The base potential of Q_2 decreases, acting to reduce I_{E_2}. In a similar manner, the circuit automatically tends to compensate for changes in I_{CBO_1}. Note that the by-pass capacitor C_{E_2} prevents a-c feedback which would reduce amplifier gain.
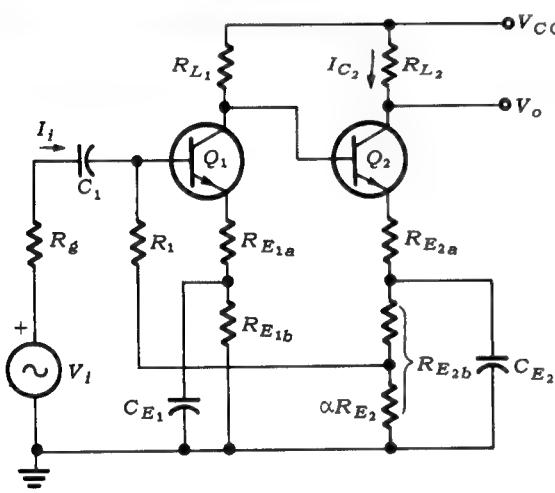

$$R_{E_2} = R_{E_{2a}} + R_{E_{2b}}$$
$$R_{E_1} = R_{E_{1a}} + R_{E_{1b}}$$

Fig. 6.29 Two-stage direct-coupled amplifier.

(a)

(b)

Fig. 6.30 (a) Simplified d-c equivalent circuit of the two-stage amplifier of Fig. 6.29. (b) Simplified Thevenin's equivalent circuit for the input to Q_2.

To analyze the circuit of Fig. 6.29, use the techniques of Chaps. 3-4 to set up the d-c equivalent circuit of Fig. 6.30a. The circuit is simplified, in that the usual resistances (r_d) across the two current generators are omitted without introducing appreciable error. Further simplification is achieved by using Thevenin's theorem (see Fig. 6.30b).

The circuit equations are

$$I_{E_2} R_{E_2} + V_{BE_2} = V_A - \underbrace{(R_{L_1} + r_{b_2})}_{R_L^*} I_{B_2}, \tag{6.14}$$

$$V_A = V_{CC} - R_{L_1} I_{C_1}, \tag{6.15}$$

$$I_{B_2} = \frac{I_{C_2} - I_{CBO_2}(1 + \beta_2)}{\beta_2} \cong \frac{I_{E_2}}{1 + \beta_2} - I_{CBO_2}. \tag{6.16}$$

Similarly,

$$I_{B_1} \cong \frac{I_{E_1}}{1 + \beta_1} - I_{CBO_1}. \tag{6.17}$$

Also,

$$I_{B_1} = \frac{\alpha R_{E_2} I_{E_2} - R_{E_1} I_{E_1} - V_{BE_1}}{\underbrace{r_{b_1} + R_1 + \alpha R_{E_1}}_{R_1^*}}.$$ (6.18)

Equation (6.16) may be substituted in (6.14) to eliminate I_{B_2}, and (6.18) may be substituted in (6.17) to eliminate I_{B_1}. There remain two equations in unknowns I_{E_1} and I_{E_2}, with I_{CBO_1} and I_{CBO_2} as independent variables:

$$I_{E_2}\left(R_{E_2} + \frac{R_L^*}{1+\beta_2}\right) + V_{BE_2} = V_{CC} - R_{L_1} I_{E_1} + R_L^* I_{CBO_2},$$ (6.19)

$$\alpha R_{E_2} I_{E_2} - V_{BE_1} = I_{E_1}\left(\frac{R_1^*}{1+\beta_1} + R_{E_1}\right) - I_{CBO_1} R_1^*.$$ (6.20)

Solve (6.20) for I_{E_1} and substitute in (6.19) to develop a formula for I_{E_2}:

$$I_{E_2}\left[R_{E_2} + \frac{R_L^*}{1+\beta_2} + \frac{R_{E_2} R_{L_1} \alpha}{R_1^*\left(\frac{1}{1+\beta_1} + \frac{R_{E_1}}{R_1^*}\right)}\right] + V_{BE_2}$$

$$= V_{CC} + \frac{V_{BE_1} \dfrac{R_{L_1}}{R_1^*}}{\dfrac{R_{E_1}}{R_1^*} + \dfrac{1}{1+\beta_1}} - \frac{R_{L_1} I_{CBO_1}}{\dfrac{R_{E_1}}{R_1^*} + \dfrac{1}{1+\beta_1}} + R_L^* I_{CBO_2}.$$ (6.21)

Equation (6.21) contains the desired information relating changes in I_{E_2} to changes in leakage currents. Use derivatives to get a convenient expression for dI_{E_2} in terms of dI_{CBO_1} and dI_{CBO_2}. This expression is

$$dI_{E_2} = \frac{\left(\dfrac{-R_{L_1}}{\dfrac{R_{E_1}}{R_1^*} + \dfrac{1}{1+\beta_1}}\right) dI_{CBO_1} + R_L^* \, dI_{CBO_2}}{R_{E_2} + \dfrac{R_L^*}{1+\beta_2} + \dfrac{R_{E_2} R_{L_1} \alpha}{R_1^*\left(\dfrac{1}{1+\beta_1} + \dfrac{R_{E_1}}{R_1^*}\right)}}.$$ (6.22)

PROBLEM 6.20 The component values for the circuit of Fig. 6.29 are

$$R_d = 1000 \ \Omega,$$

$$R_{E_{1a}} = R_{E_{2a}} = 100 \ \Omega,$$

$$R_{E_{1b}} = 1900 \ \Omega,$$

$$V_{CC} = 12 \ v,$$

$$I_{C_1} = 1 \ ma, \qquad I_{C_2} = 5 \ ma.$$

The required distortion-free output voltage is 2 v rms, minimum. Determine the remaining circuit parameters to meet the specified requirements.

Solution: The emitter potential of Q_1 is

$$V_{E_1} \cong 0.001 \times 2000 = 2 \ v,$$

so that

$$V_{B_1} \cong V_{E_1} + 0.6 = 2.6 \ v.$$

For the 2N930 transistor, $h_{FE_1} = 280$ at 1 ma; therefore,

$$I_{B_1} = \frac{0.001}{280} = 3.58 \ \mu a.$$

Proceed now to the second stage. A 2 v rms output corresponds to a 5.67 peak-to-peak voltage swing. Allowing a minimum of about 1 v for V_{CE_2},

$$V_{E_2} = 12 - 5.67 - 1 = 5.3 \ v,$$

$$R_{E_2} = \frac{5.3}{I_{E_2}} \cong \frac{5.3}{I_{C_2}}.$$

Therefore,

$$R_{E_2} = \frac{5.3}{5 \times 10^{-3}} = 1060 \ \Omega.$$

Now determine R_{L_2}:

$$R_{L_2} I_{C_2} = 2.84 \ v \ (\tfrac{1}{2} \text{ of peak-to-peak value}).$$

Solving,

$$R_{L_2} = \frac{2.84}{0.005} = 567 \ \Omega.$$

To determine α, we must at the same time choose R_1 for a required stability; R_1 is the principal component of R_1^*, the d-c resistance in the base circuit. In Chap. 4, it was pointed out that this resistance must be low for reasonable stability in the first stage. On the other hand, R_1^* acts as a load on the input. A compromise is necessary.

Assume, somewhat arbitrarily, that $R_1^* = 30 \ K \ \Omega$. Then,

$$\alpha \ V_{E_2} = 5.3 \ \alpha = I_{B_1} R_1^* + V_{B_1}.$$

For $R_1^* = 30 \ K \ \Omega$, $\alpha = 0.492$. Since $V_A = V_{B_2} \cong I_{E_2} R_{E_2} + 0.6 = 5.9 \ v$,

$$V_{CC} - I_{C_1} R_{L_1} = 12 - 0.001 R_{L_1} = 5.9,$$

so that

$$R_{L_1} = 6100 \ \Omega.$$

PROBLEM 6.21 For the parameters of the preceding problem, determine the stability factors $\partial I_{E_2}/\partial I_{CBO_1}$, $\partial I_{E_2}/\partial I_{CBO_2}$.

Solution: From (6.22), the following expressions are derived by simplification:

$$\frac{\partial I_{E_2}}{\partial I_{CBO_2}} = \frac{1 + \beta_2}{1 + \left[\dfrac{R_{E_2}}{R_{L_1}} + \dfrac{\alpha(1 + \beta_1) R_{E_1}}{R_1^* + R_{E_1}(1 + \beta_1)}\right] \dfrac{R_{L_1}(1 + \beta_2)}{R_{L_1} + r_{b_2}}}, \tag{6.23}$$

$$\frac{\partial I_{E_2}}{\partial I_{CBO_1}} = \frac{-(1 + \beta_1)}{\left[1 + (1 + \beta_1)\dfrac{R_{E_1}}{R_1^*}\right]\left[\dfrac{R_{L_1} + r_{b_2}}{R_{L_1}(1 + \beta_2)} + \dfrac{R_{E_2}}{R_{L_1}}\left(1 + \dfrac{R_{L_1}(1 + \beta_1)\alpha}{R_1^* + R_{E_1}(1 + \beta_1)}\right)\right]}. \tag{6.24}$$

Making the approximation that $r_b \ll R_{L_1}$ and substituting previously derived numerical values,

$$\frac{\partial I_{E_2}}{\partial I_{CBO_2}} = 2.3,$$

$$\frac{\partial I_{E_2}}{\partial I_{CBO_1}} = -32.5.$$

PROBLEM 6.22 Referring to the circuit of Fig. 6.29, develop an expression for the stability of I_{E_2} with respect to changes in V_{BE_1} and V_{BE_2}.

Solution: By simplifying and differentiating (6.21), the required expression is

$$dI_{E_2} = \frac{-dV_{BE_2} + \dfrac{dV_{BE_1}}{\dfrac{R_1^*}{R_{L_1}(1+\beta_1)} + \dfrac{R_{E_1}}{R_{L_1}}}}{R_{E_2}\left[1 + \dfrac{R_{L_1}\,\alpha}{\dfrac{R_1^*}{1+\beta_1} + R_{E_1}} + \dfrac{R_L^*}{(1+\beta_2)\,R_{E_2}}\right]}. \tag{6.25}$$

PROBLEM 6.23 For the circuit of Fig. 6.29, using (6.25), determine ΔI_{E_2} due to changing V_{BE} for a $100\,°C$ change in temperature.

Solution: As pointed out in Chap. 1, $\Delta V_{BE} \cong -2.2$ mv per °C increase in temperature. Substituting numerical values in (6.25),

$$\Delta I_{E_2} \cong (-85 + 246) \times 10^{-6} = 161 \ \mu\text{a}.$$

The calculation of multi-stage amplifier performance is so cumbersome that maximum use must be made of reasonable approximations for achieving practical results. Little is lost by these approximations, however, since the values of the transistor parameters themselves vary widely with temperature and among transistors. In the following problems, idealized transistors are used, where $r_E = 0$, $r_C = \infty$, and $r_B = 0$.

PROBLEM 6.24 In the circuit of Fig. 6.31 and its equivalent circuit (Fig. 6.32), determine the stability of the operating point of Q_3 with variations in I_{CBO}.

Solution: Refer to the equivalent circuit Fig. 6.33 of Fig. 6.31. Let ΔI_C be the change in collector current due to the change in I_{CBO}. It is necessary to determine

$$\Delta I_{C_3} = \Delta I_{C_{3-1}} + \Delta I_{C_{3-2}} + \Delta I_{C_{3-3}} \tag{6.26}$$
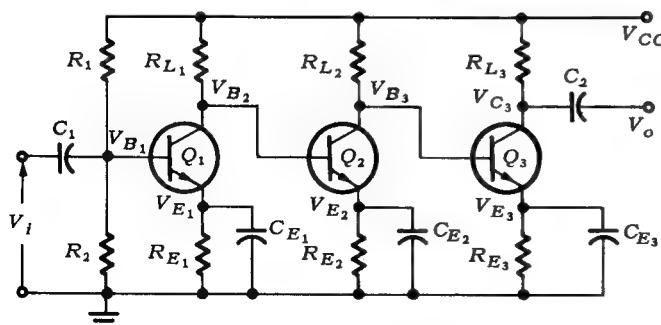

Fig. 6.31 Three-stage, direct-coupled common-emitter transistor amplifier.
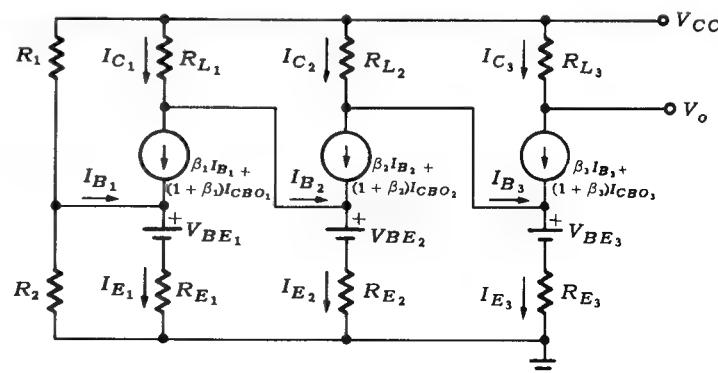
Fig. 6.32 Simplified equivalent circuit of three-stage amplifier for bias calculations. (See Fig. 6.31.)
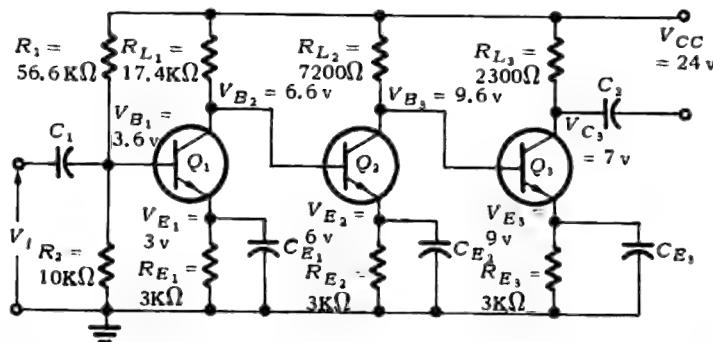
Fig. 6.33 Three-stage, direct-coupled common-emitter transistor amplifier of Fig. 6.31, with calculated resistance values and bias voltages.

where the separate components are due to changes in I_{CBO} in stages 1, 2, and 3, respectively.

Recall that, by definition, $\Delta I_{C_{1-1}} = S_1 \Delta I_{CBO_1}$. The voltage at the collector of Q_1 is reduced by $S_1 R_{L_1} \Delta I_{CBO_1}$, which corresponds to a reduction in the base voltage of Q_2. Since the d-c input impedance of Q_2 is approximately equal to $R_{E_2}(1 + \beta_2)$,

$$\Delta I_{B_2} = -\frac{S_1 R_{L_1} \Delta I_{CBO_1}}{R_{L_1} + R_{E_2}(1 + \beta_2)}. \tag{6.27}$$

Since $\Delta I_{C_{2-1}} = \beta_2 \Delta I_{B_2}$,

$$\Delta I_{B_3} = \frac{-\Delta I_{C_{2-1}} R_{L_2}}{R_{L_2} + R_{E_3}(1 + \beta_3)}. \tag{6.28}$$

Therefore, combining terms,

$$\Delta I_{C_{3-1}} = \beta_3 \Delta I_{B_3} = \frac{S_1 \beta_2 \beta_3 \Delta I_{CBO_1}}{\left[1 + \dfrac{R_{E_2}}{R_{L_1}}(1 + \beta_2)\right]\left[1 + \dfrac{R_{E_3}}{R_{L_2}}(1 + \beta_3)\right]}. \tag{6.29}$$

This is the change in the collector current of Q_3, due to ΔI_{CBO_1}.

Similarly, the contribution from ΔI_{CBO_2} is

$$\Delta I_{C_{3-2}} = \frac{-\beta_3 S_2 \Delta I_{CBO_2}}{1 + \dfrac{R_{E_3}}{R_{L_2}}(1 + \beta_3)}, \tag{6.30}$$

$$\Delta I_{C_{3-3}} = S_3 \Delta I_{CBO_3}. \tag{6.31}$$

The total variation in I_{C_3} is determined by substituting in the expressions for the components of ΔI_{C_3} in (6.26); S may be calculated using expressions developed in Chap. 4. Since $\Delta I_{C_{3-2}}$ is negative, some compensation exists, but this is not significant in practical cases. Note that the principal drift components are introduced by leakage changes in the first stage.

PROBLEM 6.25 For the circuit of Fig. 6.31 and its equivalent circuit (Fig. 6.32), determine the stability of I_{C_3} due to variations in V_{BB}. Assume $I_{CBO} = 0.01 \ \mu a$.

Solution: Proceed from stage to stage, as in Prob. 6.24:

$$\Delta I_{C_{1-1}} = \beta_1 \frac{\Delta V_{EB_1}}{R_{B_1} + R_{E_1}(1 + \beta_1)}$$

is the current change in Q_1 due to ΔV_{EB_1}. As before,

$$\Delta I_{C_{2-1}} = -\Delta I_{C_{1-1}} \frac{R_{L_1} \beta_2}{R_{L_1} + R_{E_2}(1 + \beta_2)}.$$

At the third stage,

$$\Delta I_{C_{3-1}} = \Delta I_{C_{2-1}} \frac{R_{L_2} \beta_3}{R_{L_2} + R_{E_3}(1 + \beta_3)}.$$

Combine terms:

$$\Delta I_{C_{3-1}} = \frac{-\beta_1 \beta_2 \beta_3 R_{L_1} R_{L_2} \Delta V_{EB_1}}{[R_{B_1} + R_{E_1}(1 + \beta_1)][R_{L_1} + R_{E_2}(1 + \beta_2)][R_{L_2} + R_{E_3}(1 + \beta_3)]}.$$

Similarly, we may derive expressions for $\Delta I_{C_{3-2}}$ and $I_{C_{3-3}}$, which may be summed to give the total change, ΔI_{C_3}:

$$\Delta I_{C_3} = \frac{-\beta_1 \beta_2 \beta_3 R_{L_1} R_{L_2} \Delta V_{BE_1}}{[R_{B_1} + R_{E_1}(1 + \beta_1)][R_{L_1} + R_{E_2}(1 + \beta_2)][R_{L_2} + R_{E_3}(1 + \beta_3)]}$$
$$+ \frac{\beta_2 \beta_3 R_{L_2} \Delta V_{BE_2}}{[R_{L_1} + R_{E_2}(1 + \beta_2)][R_{L_2} + R_{E_3}(1 + \beta_3)]} - \frac{\beta_3 \Delta V_{BE_3}}{R_{L_2} + R_{E_3}(1 + \beta_3)}. \quad (6.32)$$

This expression shows some compensation. It is possible to take advantage of this by adjustment of parameters.

PROBLEM 6.26 Design an amplifier for maximum output voltage, using the circuit of Fig. 6.31. Let

$$I_{C_1} = 1 \text{ ma}, \qquad R_{E_1} = R_{E_2} = R_{E_3} = 3 \text{ K }\Omega,$$
$$I_{C_2} = 2 \text{ ma}, \qquad R_2 = 10 \text{ K }\Omega,$$
$$I_{C_3} = 3 \text{ ma}, \qquad C_{E_1} = C_{E_2} = C_{E_3} = 3000 \text{ }\mu\text{f},$$
$$V_{CC} = 24 \text{ v}.$$

Use approximate design procedures. Considering the sensitivity of I_{CBO} and V_{BE} to temperature, calculate ΔI_{C_3} resulting from changes in these two parameters as temperature increases from 25 °C to 100 °C.

Solution: Assume base currents are negligible compared to collector currents. Then,

$$V_{E_1} \cong I_{C_1} R_{E_1} = 0.001 \times 3000 = 3 \text{ v},$$
$$V_{B_1} = V_{E_1} + V_{BE_1} \cong 3.0 + 0.6 = 3.6 \text{ v}.$$

Calculating R_1 from the voltage division ratio of the bias divider, $R_1 \cong 57 \text{ K}\Omega$. Then,

$$V_{E_2} \cong I_{C_2} R_{E_2} = 0.002 \times 3000 = 6 \text{ v},$$
$$V_{B_2} = V_{E_2} + V_{BE_2} \cong 6.0 + 0.6 = 6.6 \text{ v}.$$

We may now determine R_{L_1}:

$$V_{CC} - I_{C_1} R_{L_1} = V_{B_2}.$$

Substituting and solving, $R_{L_1} = 17.4 \text{ K }\Omega$.
Continuing the above with bias calculations,

$$V_{E_3} \cong I_{C_3} R_{E_3} = 0.003 \times 3000 = 9 \text{ v},$$

$$V_{B_3} = V_{E_3} + V_{BE_3} \cong 9.0 + 0.6 = 9.6 \text{ v},$$

$$24 - 0.002 R_{L_2} = 9.6, \qquad R_{L_2} = 7.2 \text{ K } \Omega.$$

The choice of R_{L_3} is based on the requirement for developing maximum output. We require the maximum swing in collector voltage, V_{C_3}:

$$V_{C_{3_{min}}} = V_{E_3} + V_{CE_{min}},$$

where whole $V_{CE\,min}$ is the minimum V_{CE} for Q_3 for correct transistor operation, and is assumed to be 1 v. Therefore,

$$V_{C_{3_{min}}} = 9 + 1 = 10 \text{ v},$$

and when the transistor is nearly at cut-off, $V_{C_{3_{max}}} \cong 24$ v. The collector voltage may swing from 10 v to 24 v, with a quiescent level of 17 v. The peak-to-peak swing is 14 v, and the peak swing = 14/2 = 7 v:

$$R_{L_3} I_{C_3} = 7, \qquad R_{L_3} = \frac{7}{0.003} = 2330 \ \Omega.$$

The final circuit with all parameters included is shown in Fig. 6.33.

Now calculate the temperature sensitivity of I_{C_3}, as I_{CBO} and V_{BE} vary. The assumed $I_{CBO} = 0.01 \ \mu$a. From Fig. 4.2, I_{CBO} increases by a factor of 17 at 100 °C. Thus, $\Delta I_{CBO} \cong I_{CBO} = \Delta I_{CBO_2} = \Delta I_{CBO_3} = 0.16 \ \mu$a. Substitute in (6.29), (6.30), and (6.31), with known ΔI_{CBO}:

$$\Delta I'_{C_3} = \frac{\beta_2 \beta_3 S_1 \Delta I_{CBO}}{\left[1 + \dfrac{R_{E_2}}{R_{L_1}}(1 + \beta_2) \right] \left[1 + \dfrac{R_{E_3}}{R_{L_2}}(1 + \beta_3) \right]}$$

$$- \frac{\beta_3 S_2 \Delta I_{CBO}}{1 + \dfrac{R_{E_3}}{R_{L_2}}(1 + \beta_2)} + S_3 \Delta I_{CBO}. \tag{6.33}$$

Calculating stability factors,

$$S_1 \cong 1 + \frac{R_1 \| R_2}{R_{E_1}} = 3.8,$$

$$S_2 \cong 1 + \frac{R_{L_1}}{R_{E_2}} = 6.8,$$

$$S_3 \cong 1 + \frac{R_{L_2}}{R_{E_3}}.$$

Substituting in (6.33) and solving,

$$\Delta I_{C_3} = 71.1 \ \Delta I_{CBO} = 11.4 \ \mu\text{a at } 100\,°\text{C}.$$

This is negligible since $I_{C_3} = 3$ ma, and $\Delta I'_{C_3}$ corresponds to only a slight bias shift. The result confirms the validity of our approximation methods; high calculation accuracy is not justified.

Now determine the component of change, $\Delta I''_{C_3}$, due to ΔV_{BE} over the specified temperature range:

$$\Delta V_{BE} = (75\,°\text{C})(-2.2 \text{ mv/}°\text{C}) = -165 \text{ mv}.$$

Substituting in (6.32),

$$\Delta I''_{C_3} = 0.69 \text{ ma.}$$

While this is much more significant than the $\Delta I'_{C_3}$ resulting from ΔI_{CBO}, it is still not a serious shift. The stability of the multi-stage direct-coupled amplifier is very satisfactory.

We may make an estimate of the effect on I_C of a change in β:

$$\frac{\Delta I_C}{I_C} \cong S \frac{\Delta \alpha}{\alpha}. \qquad [4.15]$$

Assume, as the basis of estimating, that β_1 varies from 325 at 25°C to 460 at 100°C, with an average value of 390. The value of $\Delta \alpha / \alpha$ corresponding to this β_1 change is 0.9×10^{-3}. Therefore, for the first amplifier stage,

$$\frac{\Delta I_{C_1}}{I_{C_1}} = S_1 \ (0.9 \times 10^{-3}),$$

and since $S_1 = 3.8$,

$$\frac{\Delta I_{C_1}}{I_{C_1}} = 0.34 \times 10^{-4}.$$

Due to the change in β_1, I_{C_1} changes by 0.34%. This is also negligible.

The effects of changes in β_2 and β_3 may similarly be estimated as negligible. Only the temperature effects of changes in V_{BE} are significant. These can be compensated for by the methods of Chap. 4.

PROBLEM 6.27 For the amplifier circuit of Fig. 6.33, estimate the input impedance and voltage gain at 1000 Hz, and the maximum undistorted peak-to-peak output voltage at 25°C and 100°C. Specify C_1 so that voltage gain is 3 db down at 60 Hz. Note that the circuit parameters are those derived in Prob. 6.26.

Solution: This problem provides an example of a step-by-step series of calculations of input and output impedances, starting with the last stage. At 1000 Hz ($\omega = 6280$ rad/sec), all emitter by-pass capacitors are essentially short-circuits. The transistor parameters used here are summarized in Table 6.2. Practical approximations are made throughout.

From Table 5.1:

$$R_i = r_b + (r_e + R_{E\,a}) \frac{1 + \beta}{1 + \dfrac{R_L + R_{E\,a}}{r_c} (1 + \beta)},$$

with $R_L \ll r_c$, and $r_e \ll r_c / (1 + \beta)$. The portion of emitter resistor *not* by-passed by C_E, $R_{E\,a}$, is zero. Now substitute numerical values from Table 6.2 in the above expression to find the input impedance of the third stage:

At 25°C, $R_{i_3} = 5280 \ \Omega$,

At 100°C, $R_{i_3} = 8550 \ \Omega$.

These input impedances, paralleled with R_{L_2}, establish the effective load, $R^*_{L_2}$, on the second stage:

At 25°C, $R^*_{L_2} = 3040 \ \Omega$,

At 100°C, $R^*_{L_2} = 3910 \ \Omega$.

Proceeding in this manner, the required additional items may be calculated, and are summarized in Table 6.3. These include the required amplifier input impedance.

TABLE 6.3

	25°C	100°C	Unit
R_{i_2}	6310	9830	ohm
$R^*_{L_1}$	4640	6290	ohm
R_{i_1}	8800	13,850	ohm
R_{i_3}	5280	8550	ohm
$R^*_{L_2}$	3040	3910	ohm

Now calculate the currents and voltages in successive stages as required to determine over-all gain. If the current gain of the input stage is A_{i_1}, then

$$I_{b_2} = I_{b_1} A_{i_1} \frac{R_{L_1}}{R_{L_1} + R_{i_2}}.$$

Substituting the expression for current gain from Table 5.1, and replacing I_{b_1} by V_i / R_{i_1},

$$I_{b_2} = \frac{V_i \beta_1}{R_{i_1} \left[1 + \frac{R_{L_1}^*}{r_{c_1}} (1 + \beta_1) \right]} \frac{R_{L_1}}{R_{L_1} + R_{i_2}}$$

or

$$\frac{I_{b_2}}{V_i} = \frac{\beta_1 R_{L_1}}{R_{i_1}} \frac{1}{\left[1 + \frac{R_{L_1}^*}{r_{c_1}} (1 + \beta_1) \right] \left[R_{L_1} + R_{i_2} \right]}. \qquad (6.34)$$

Similarly,

$$I_{b_3} = \frac{I_{b_2} \beta_2 R_{L_2}}{\left[1 + \frac{R_{L_2}^*}{r_{c_2}} (1 + \beta_2) \right] \left[R_{L_2} + R_{i_3} \right]}. \qquad (6.35)$$

Note that

$$\frac{V_o}{V_i} = \frac{I_{b_3}}{V_i} \frac{\beta_3 R_{L_3}}{\left[1 + \frac{R_{L_3}}{r_{c_3}} (1 + \beta_3) \right]}. \qquad (6.36)$$

Substituting numerical values for the circuit parameters (see Table 6.1), the required performance data summarized in Table 6.4 are obtained. The voltage gains in Table 6.4 are part of the required solution to the problem.

Note that although β increases by about 40% with increasing temperature, suggesting an over-all increase in gain of about $(1.4)^3 = 2.75$ times, the actual gain increase is only about 15%. The separate effects of changing β, as shown in the gain equations, partially cancel.

Determine C_1 such that gain is 3 db down at 60 Hz. At this frequency, the capacitive reactance must equal the minimum (25 °C) input impedance:

TABLE 6.4		
	25°C	100°C
I_{b_2}/V_i	17.8×10^{-3}	17.5×10^{-3}
I_{b_3}/V_i	2.83	2.54
V_o/V_i	2.1×10^6	2.4×10^6

$$X_{C_1} = R_{i_1} = 8800 \ \Omega,$$

$$C_1 = 0.302 \ \mu f.$$

Determine the maximum undistorted peak-to-peak output voltage from the bias point. At 25 °C, the quiescent conditions are

$$I_{C_3} = 3 \ ma,$$

and since $R_{L_3} = 2330 \ \Omega$ and $R_{E_3} = 3000 \ \Omega$,

$$V_E = 0.003 \times 3000 = 9 \ v,$$

$$V_C = 24 - 7 = 17 \ v,$$

$$V_{CE} = 24 - (9 + 7) = 8 \ v.$$

The resistance R_{E_3} is by-passed, so that the voltage V_{E_3} is a fixed 9 v regardless of the a-c signal component. A load line for this amplifier stage is drawn for an effective d-c voltage of $24 - 9 = 15$ v, and a resistance of 2330 Ω

(see Fig. 6.34). If a minimum V_{CE} for satisfactory transistor operation is set at 1 v, it may be seen that the peak-to-peak a-c voltage swing is 14 v.

Re-examine the peak-to-peak output range for 100 °C operation. As previously calculated in Prob. 6.26, $I_{c_3} = 3.69$ ma at 100 °C. The emitter voltage is 11.1 v, so that the effective voltage for the load line is 12.9 v. The modified load line is indicated in Fig. 6.34, showing a possible peak-to-peak output excursion of 11.9 v. This reduction in output voltage range is the principal reason for maintaining bias point stability. If I_C increases to 6 ma, the amplifier actually becomes inoperative.

PROBLEM 6.28   For the amplifier of Fig. 6.33, connect a 1000 Ω output load to the collector of Q_3 through a blocking capacitor C_2 having negligible a-c reactance. What is the maximum undistorted output swing?

Solution: Since the 1000 Ω load does not effect the d-c operating point (because of the blocking capacitor), this point remains the same in Fig. 6.34. The a-c load line, however, corresponds to an effective resistance, $R_{L_3}^*$, equal to 2330 Ω in parallel with 1000 Ω, or 700 Ω. The maximum undistorted output swing is limited by the $I_C = 0$ axis, and is 8.56 v peak-to-peak.
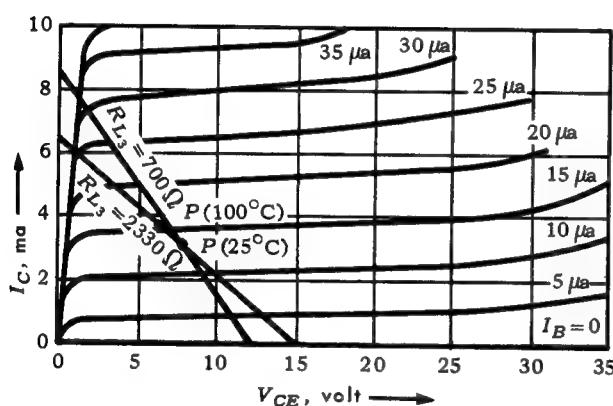

Fig. 6.34 Load lines superimposed on 2N929 common-emitter characteristics; $V_E = 9$ v.
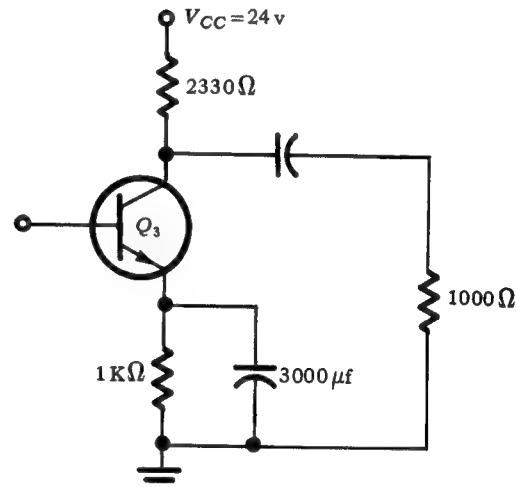
Fig. 6.35 Output transistor circuit driving a 1000 Ω a-c load.

PROBLEM 6.29   With the amplifier of Fig. 6.33 and the load of Fig. 6.35, find the voltage gain at 25 °C.

Solution: From (6.36),

$$\frac{V_o}{V_i} = \frac{I_{b_3}}{V_i} \beta_3 \frac{R_{L_3}}{1 + \frac{R_{L_3}}{r_{c_3}}(1 + \beta_3)}. \qquad [6.36]$$

We replace R_{L_3} by $R_{L_3}^* = 700$ Ω. Substituting numerical values from Prob. 6.27,

$$\frac{V_o}{V_i} = 2.83 \times 360 \frac{700}{1 + \frac{700 \times 361}{6.7 \times 10^6}} = 690,000,$$

as compared with over a million before the 1 K Ω load was added.

PROBLEM 6.30   Repeat Prob. 6.27, but with 100 Ω (see Fig. 6.36) of each emitter resistor unby-passed. Calculate only V_o/V_i.

Solution: Proceed as in Prob. 6.27, using the formulae summarized below:

$$R_i \cong r_b + (r_e + R_{Ea})(1 + \beta)\frac{1}{1 + \dfrac{R_L}{r_c}(1 + \beta)},$$

for $R_{Ea} \ll r_c/(1 + \beta)$. Then,

$$\frac{I_{b_2}}{V_i} = \frac{\beta_1}{R_{i_1}}\frac{R_{L_1}}{\left[1 + \dfrac{R_{L_1}^*}{r_{c_1}}(1 + \beta_1)\right][R_{L_1} + R_{i_2}]}, \qquad [6.34]$$

$$\frac{I_{b_3}}{V_i} = \frac{I_{b_2}}{V_i}\beta_2\frac{R_{L_2}}{\left[1 + \dfrac{R_{L_2}^*}{r_{c_2}}(1 + \beta_2)\right][R_{L_2} + R_{i_3}]}, \qquad [6.35]$$

$$\frac{V_o}{V_i} = \frac{I_{b_3}}{V_i}\beta_3\frac{R_{L_3}}{1 + \dfrac{R_{L_3}}{r_{c_3}}(1 + \beta_3)}. \qquad [6.36]$$

Fig. 6.36 Modified portion of the circuit of Fig. 6.33, with portion of emitter resistor unby-passed.

     By substituting numerical values, the partial results and the computed voltage gain are determined and listed in Table 6.5. Observe the much reduced gain by comparing the data with that of Table 6.4. Although the variation in gain with temperature is somewhat improved by the unby-passed emitter resistances, the principal benefit is the reduced sensitivity of circuit gain to variations in the β's of individual transistors.

<div align="center">TABLE 6.5</div>

	25°C	100°C	Unit
R_{i_3}	37,200	50,000	ohm
$R_{L_2}^*$	6040	6300	ohm
R_{i_2}	33,710	43,500	ohm
$R_{L_1}^*$	11,500	12,400	ohm
R_{i_1}	33,000	43,000	ohm
I_{b_2}/V_i	2.62×10^{-3}	2.06×10^{-3}	amp/volt
I_{b_3}/V_i	111×10^{-3}	88×10^{-3}	amp/volt
V_o/V_i	8.3×10^4	8.4×10^4	

6.5 Complementary Transistors

     The availability of *complementary pairs* of transistors (n-p-n and p-n-p types with otherwise similar characteristics) has made it easier to design direct-coupled amplifier stages. They overcome the difficult biasing problems of direct-coupled stages using only one transistor type. The following example shows how easy it is to devise direct-coupled stages using complementary pairs.

PROBLEM 6.31 Referring to Fig. 6.37, determine the load resistors, R_{L_1} and R_{L_2}, for the specified operating conditions; select R_{L_3} for maximum undistorted output.

Solution: For the specified conditions,

$$V_{E_1} = I_{E_1} R_{E_1} \cong I_{C_1} R_{E_1} = 10^{-3} \times 3000 = 3 \text{ v.}$$

Allowing 0.6 v for the base-emitter drop of Q_1, $V_A = 3.0 + 0.6 = 3.6$ v.

Since high β transistors are employed, we may neglect the base current of Q_1 in determining R_1 for the required V_A:

$$V_A = V_{CC} \frac{R_2}{R_1 + R_2}.$$

The validity of this approximation may be verified later, if desired. Substituting numerical values for V_A, R_2, and V_{CC}, R_1 is determined to be 15 KΩ. Continuing to the second stage,

$$V_{E_2} = 9 - (0.001)(3000) = 6 \text{ v.}$$

The base potential, allowing the usual 0.6 v drop from the emitter, is 5.4 v. This, of course, must be the collector potential of Q_1. Thus,

$$V_{C_1} = 5.4 = 9 - (0.001) R_{L_1}.$$

Solving, $R_{L_1} = 3.6$ KΩ.

Continue in a similar fashion to the third stage:

$$V_{E_3} = (0.001) \, 3000 = 3 \text{ v,}$$

$$V_{C_2} = 3 + 0.6 = 3.6 \text{ v,}$$

$$3.6 = (0.001) R_{L_2}, \qquad R_{L_2} = 3,600 \text{ Ω.}$$

This completes the determination of all parameters except R_{L_3}, which is found from the requirement for maximum undistorted output. Allowing a minimum V_{CE} of 1 v for Q_3, V_{C_3} varies from 4 v to a cut-off 9 v, for a peak-to-peak swing of 5 v. Set V_{C_3} to the average of 6.5 v. Thus, a 1 ma swing of collector current corresponds to 2.5 v, so that $R_{L_3} = 2.5$ KΩ. For greater gain, R_{L_3} can be increased until the limiting condition is reached where $V_{C_3} = 4$ v maximum for $R_{L_3} = 5$ KΩ. For this condition, the gain is doubled and the peak-to-peak undistorted output is zero.

Previous multi-stage amplifier calculations relating to performance and temperature sensitivity apply to amplifiers using complementary transistors, except that there are no d-c polarity inversions between stages. Therefore effects of changes in V_{BE}, I_{CBO}, and β, always *add*. A-c calculations are *identical* to those illustrated earlier in this chapter.

PROBLEM 6.32 For the circuit of Fig. 6.38, determine the unspecified parameters for the given operating conditions, as well as a-c gain and maximum power absorbed by R_{L_2}.

Solution: Assume, as a crude estimate (which may be re-examined after an approximate analysis is completed) that about 5% of the collector current of Q_2 is diverted by feedback to the first stage. Thus, if current through R_{L_2} is specified at 95 ma, and current through R_3 at about 5 ma, then $I_{C_2} = 100$ ma. Therefore,

$$V_{C_2} = 31 \times (-0.095) \cong -3 \text{ v.}$$
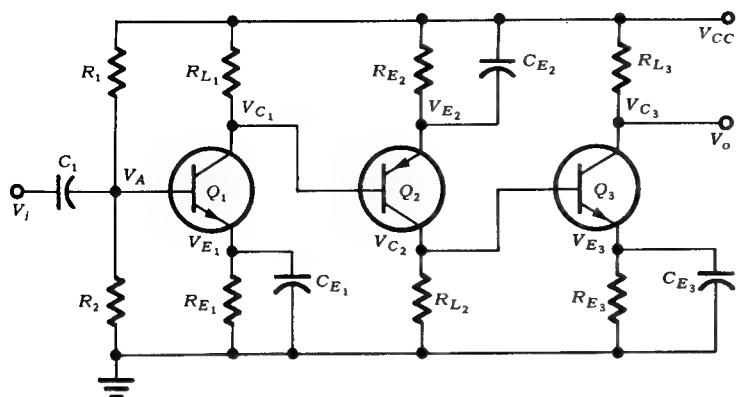
Q_1, Q_3: n-p-n silicon transistor $\bigg\}$ high β, $\beta > 100$
Q_2: p-n-p silicon transistor

$R_{E_1} = R_{E_2} = R_{E_3} = 3\,K\Omega$, $R_2 = 10\,K\Omega$
$V_{CC} = 9\,v$
C_{E_1}, C_{E_2}, C_{E_3}, C_1: essentially infinite
$I_{C_1} = I_{C_2} = I_{C_3} = 1\,ma$

Fig. 6.37 Direct-coupled amplifier using complementary transistors.
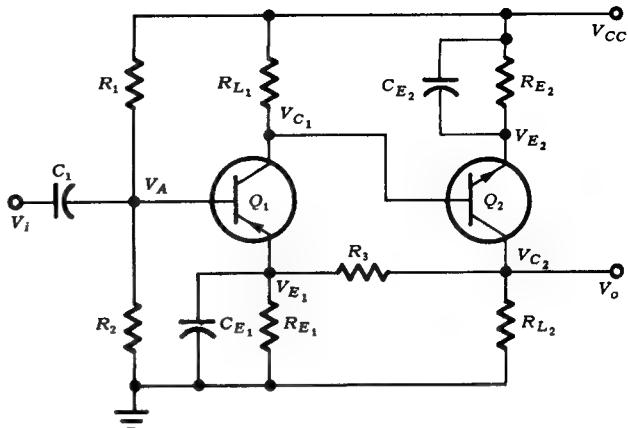
Q_2: 2N2907

$I_{C_2} = 100\,ma$, $r_{e_2} = 0.26\,\Omega$, $r_{b_2} = 74\,\Omega$
$\beta_2 = h_{fe_2} = 100$, $h_{FE_2} \cong 110$ at $I_{C_2} = 100\,ma$
C_{E_1}, C_{E_2}: essentially infinite
$V_{CC} = 10\,v$, $R_{L_2} = 31\,\Omega$

Q_1: 2N930

$r_{e_1} = 11\,\Omega$, $r_{c_1} = 2 \times 10^6$
$\beta_1 = h_{fe_1} = 380$; $h_{FE_1} = 380$ at $I_{C_1} = 10\,ma$

Fig. 6.38 Two-stage direct-coupled amplifier using complementary transistors, and d-c feedback for bias stabilization.

Dynamically, V_{C_2} may vary from zero, near transistor cut-off, to approximately $-6\,v$ maximum. Allowing for the usual 1 v minimum V_{CE}, the drop across R_{E_2} is

$$10 - (6 + 1) = 3\ v.$$

For $I_{E_2} \cong 100\,ma$, $R_{E_2} = 30\,\Omega$. Continuing, since $V_{E_2} = -7\,v$, allowing 0.6 v for V_{BE_2}, $V_{C_1} = -6.4\,v$.

At $I_{C_2} = 100\,ma$, the 2N2907 transistor has a d-c current gain of $h_{FE} \cong 110$, so that a bias current of less than 1 ma is required. Thus, $I_{C_1} = 10\,ma$ should be ample drive. This gives

$$R_{L_1} = \frac{10 - 6.4}{0.01} = 360\ \Omega.$$

Now evaluate the parameters of the feedback circuit containing R_3. Feedback resistor R_3 tends to stabilize collector current by resetting the bias of Q_1 so as to automatically oppose changes. For correct feedback, V_{C_2} must be greater than V_{E_1}. Assume, consistent with earlier calculations, that $V_{E_1} = 2\,v$, and current through R_3 is 5 ma. Then,

$$R_3 = \frac{3 - 2}{0.005} = 200\ \Omega.$$

With current through R_{E_1} equal to $I_{C_1} + 5\,ma$,

$$R_{E_1} = \frac{2\ v}{0.015} = 133\ \Omega.$$

Now calculate the base bias resistors of Q_1. Since $V_{E_1} = 2\,v$, $V_A = 2 + 0.6 = 2.6\,v$. Assume (as a starting point) 1 ma through R_2. Thus,

$$R_2 = \frac{2.6}{0.001} = 2600\ \Omega.$$

The d-c input impedance to the first transistor may be estimated:

$$R_{i_1}\big|_{\text{d-c}} = (1 + h_{FE}) R_{E_1} = 381 \times 133 = 51 \text{ K } \Omega.$$

We may safely ignore the base drain of Q_1 in calculating R_1:

$$\frac{R_2}{R_1 + R_2} V_{CC} = V_A.$$

Substituting and solving, $R_1 = 7400 \ \Omega$. If the shunting effect of the input impedance of Q_1 is considered, R_1 becomes 7050 Ω. (Actually, final bias adjustments are best done experimentally.)

For Q_1, a 2N930 transistor, $r_e = 11 \ \Omega$, $h_{fe} = 380$, and $r_c = 2 \times 10^6$. Thus, continuing,

$$R_{i_1} \cong (1 + h_{fe}) \, r_e = 381 \times 11 = 4200 \ \Omega,$$

$$I_{b_1} = \frac{V_i}{R_{i_1}} = \frac{V_i}{4200},$$

$$A_i \cong \frac{\beta}{1 + \dfrac{R_L}{r_c}(1 + \beta)} = \frac{380}{1 + \dfrac{360 \times 381}{2 \times 10^6}} = 358, \qquad \text{[Table 5.1]}$$

$$I_{c_1} = \frac{358 \, V_i}{4200},$$

$$I_{b_2} = I_{c_1} \frac{R_{L_1}}{R_{L_1} + R_{i_2}},$$

$$R_{i_2} \cong r_{b_2} + r_{e_2}(1 + h_{fe_2}). \qquad \text{[Table 5.1]}$$

Substituting numerical values for the 2N2907 transistor,

$$R_{i_2} = (0.26)(101) + 74 \cong 100 \ \Omega.$$

Continuing to substitute numerical values,

$$A_{i_2} \cong 100, \qquad I_{c_2} = A_{i_2} I_{b_2} = 6.7 \ V_i.$$

For a-c signals, R_3 is in parallel with R_{L_2}, so that effective load resistance is $31||200$, or 26.8 Ω.

Therefore $V_o = 6.7 \ V_i \times 26.8 = 179 \ V_i$; hence, the required voltage gain is

$$\frac{V_o}{V_i} = 179.$$

The instantaneous voltage across R_{L_2} can go from 9 to 6 v (leaving a 1 v minimum for V_{CE}). Thus, maximum undistorted output is 6 v peak-to-peak, or 2.12 v rms. Maximum undistorted *power output P* is

$$P = \frac{V_o^2}{R_{L_2}} = \frac{(2.12)^2}{31} \cong 135 \text{ mw}.$$

Under quiescent (zero a-c) conditions, the power in the collector junction of Q_2 is $0.1 \text{ a} \times (7 - 3) \text{ v} = 400 \text{ mw}$. From the data sheet of the 2N2907, the transistor power rating at $T \ ^\circ\text{C}$ is

$$\text{Power rating} = 1.8 - 10.3 \times 10^{-3} \, (T - 25^\circ\text{C}).$$

At $T = 100\,^\circ\text{C}$, the rating is approximately a watt, so we are well within the rating for the calculated 135 mw dissipation. As shown in the next chapter, the dissipation in this type amplifier *decreases* with increased a-c input signals.

Note in Fig. 6.38 that if only *part* of R_{E_1} is by-passed by a capacitor, a-c

feedback is introduced which simultaneously lowers and stabilizes the gain, and increases input impedance. (Feedback is considered in greater detail in Chap. 8.)

6.6 Supplementary Problems

PROBLEM 6.33 In the circuit of Fig. 6.3, let $R_{11} = R_{12} = 1 \text{ M}\Omega$, $R_g = 100 \Omega$, $R_{L_1} = R_{L_2} = 6.8 \text{ K}\Omega$, $h_{ie} = 2200 \Omega$, $h_{ie} = 100 \Omega$, $h_{re} \sim 0$, and $h_{oe} \sim 0$. Calculate C_2 for a break frequency of 25 Hz. Assume that the influence of all other capacitors is negligible.

PROBLEM 6.34 For the circuit of Prob. 6.33, calculate the frequency response if $C_{E_2} = 5 \mu F$ and C_2 is equal to the value obtained in Prob. 6.33. Assume $C_{E_1} = C_1 = \infty$.

PROBLEM 6.35 In the circuit of Fig. 6.24, let $R_1 = R_2 = 10 \text{ K}\Omega$, $R_E = 1.5 \text{ K}\Omega$, $C_1 = 10 \mu F$, and $n = 30$. The load resistance $R_L = 10 \Omega$ with all other transistor characteristics the same as in Fig. 6.24. Calculate (a) the frequency response of the amplifier if it is driven by a zero-resistance generator, (b) the power gain at 1000 Hz, and (c) the maximum power output using the characteristics of the 2N930 transistor in Fig. 6.28.

PROBLEM 6.36 In the circuit of Fig. 6.38, let $R_{L_2} = 18 \Omega$, $R_{E_2} = 33 \Omega$, $C_{E_2} = 100 \mu F$, $R_{E_1} = 120 \Omega$, $C_{E_1} = 100 \mu F$, $R_{L_1} = 270 \Omega$, $R_3 = 180 \Omega$, $R_2 = 270 \Omega$, and $R_1 = 7500 \Omega$. Then the transistor characteristics of the Q_2: 2N2907 and the Q_1: 2N930 transistors are as follows:

Q_2: 2N2907	Q_1: 2N930
$h_{fe} = h_{FE} = 100$	$h_{fe} = h_{FE} = 400$
$r_e = 0.25 \Omega$	$r_e = 10 \Omega$
$r_b = 100 \Omega$	$r_b = 0 \Omega$
$r_c = \infty$	$r_c = \infty$

Determine (a) the frequency response when feeding R_{L_2} if $C_1 = \infty$ and $R_g = 0$, (b) the maximum undistorted power absorbed by R_{L_2}, (c) the d-c gain in R_{L_2} with zero input, and (d) the power dissipated in Q_2 with zero input.

7 | POWER AMPLIFIERS

7.1 Introduction

Up until this chapter we have focused our attention on the transistor small-signal amplifier, with emphasis on voltage and current gains. But in an amplifier system that delivers appreciable output power, voltage and current gains are only important considerations in the design of the *preamplifier stages*, not in the *power stage*. The prime objective in the design of the power stage is the achievement of a required power output with a specified efficiency and permissible distortion.

The power transistor must usually be operated over its full range of output characteristics, which includes regions of nonlinearity. Because of this latter factor, power stage design by means of equivalent circuits is less useful. Graphical methods are much more suitable, as will be illustrated.

A more detailed knowledge of transistor characteristics is needed for the analysis and design of power stages than for small-signal stages. Refer to Fig. 7.1 which shows the transistor output characteristics for the common-emitter connection over their full range of interest. In particular, let us examine the characteristic curves in the high-voltage region.
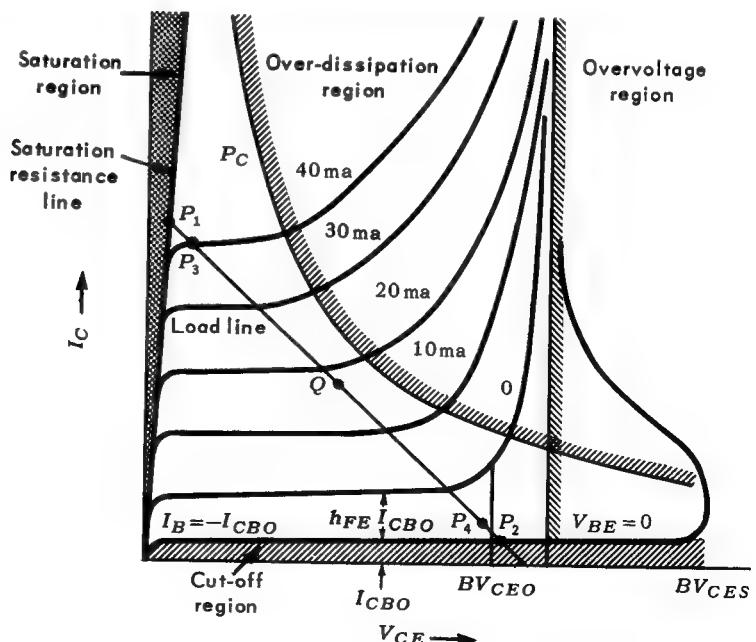

Fig. 7.1 Permissible operating limits of power transistors, showing non-linear regions.

Consider the case where the emitter is open, and a normal reverse bias is applied to the collector-base junction. As described in Chap. 1, minority carriers are accelerated across the depletion layer and impinge on other atoms in the crystal. If the applied voltage is sufficiently high, these impacts lead to the generation of additional electron-hole pairs, thus increasing the current flow. The newly created carriers, themselves accelerated, in turn may generate even more electron-hole pairs. A *multiplication* or *avalanche effect* thus occurs, which may be described analytically by the following expression:

$$\alpha^* = M\alpha. \tag{7.1}$$

where α is the current gain of the transistor in the common-base circuit, M is a dimensionless multiplying factor, and α^* is the current gain at higher voltages in the vicinity of breakdown.

The multiplying factor is described by the expression

$$M = \frac{1}{1 - \left(\dfrac{V}{V_B}\right)^n}, \tag{7.2}$$

where V_B is the breakdown voltage of the collector-base junction with the emitter open-circuited (BV_{CBO}), and V is the applied junction voltage. In the breakdown region, the collector-base current is multiplied by M.

An expression for the *effective* forward current gain for the common-emitter connection is easily derived:

$$\alpha^* = \alpha M = \frac{h_{FE}^*}{1 + h_{FE}^*}.$$

Solving for h_{FE}^*,

$$h_{FE}^* = \frac{\alpha M}{1 - \alpha M}. \tag{7.3}$$

For zero base current,

$$\begin{aligned}
I_C &= I_{CBO}(1 + h_{FE}^*)M \\
&= I_{CBO}\frac{M}{1 - \alpha M} \\
&= I_{CBO}\frac{1}{(1 - \alpha) - \left(\dfrac{V}{V_B}\right)^n}. \tag{7.4}
\end{aligned}$$

Note that n and V_B are constants for a particular transistor. Typically, $n \cong 3$ for a germanium p-n-p transistor, and $n \cong 5$ for a germanium n-p-n transistor.

From (7.4) when $I_C \doteq \infty$,

$$\left(\frac{V}{V_B}\right)^n + \alpha = 1.$$

Substituting typical numerical values, e.g., $\alpha = 0.97$, $n = 3$, and solving, $V/V_B = 0.31$. The voltage V, for which the collector current approaches infinity, is referred to as BV_{CEO} (collector-emitter breakdown voltage with base open). Thus, for this particular case,

$$BV_{CEO} = 0.31\ BV_{CBO}.$$

In the interest of low distortion and as a safeguard against damaging transients, the collector voltage is best limited to a maximum of BV_{CEO}.

Collector current, on the other hand, has no such well-defined limit. Practically, the maximum current is limited by the fall-off in h_{FE}, as shown in Fig. 7.2.
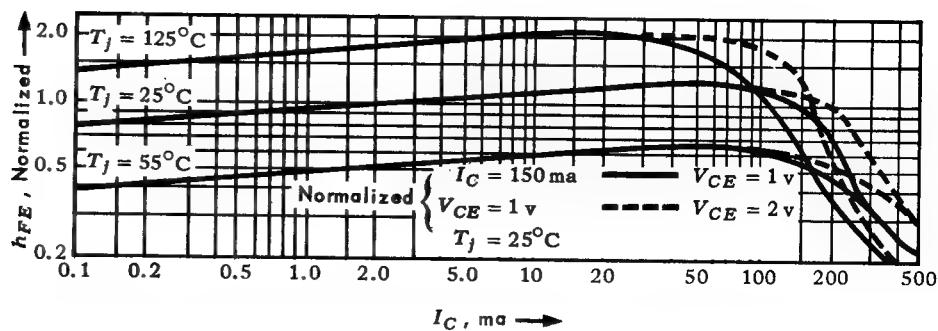
Fig. 7.2 Typical current gain characteristics of a medium power germanium transistor. Results are normalized for convenient representation.

High current occurring simultaneously with high voltage is limited by *junction temperature*.

Junction temperature depends directly on the product of power dissipation and the *thermal resistance* between the collector-base junction and its environment. The thermal resistance from the junction to the transistor case is normally specified by the transistor manufacturer. The unit for thermal resistance is °C/watt. Additional components of thermal resistance are the resistance from transistor case to mounting surface, and the resistance from mounting surface to the en-
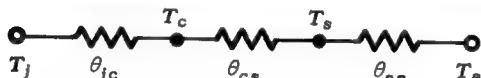
T_j = junction temperature
T_c = case temperature
T_s = heat sink temperature
T_a = ambient temperature
θ_{jc} = thermal resistance, junction to case
θ_{cs} = thermal resistance, case to heat sink
θ_{sa} = thermal resistance, heat sink to ambient temperature

All temperatures, °C

All thermal resistances, °C/watt

Total thermal resistance

$$\theta_{ja} = \theta_{jc} + \theta_{cs} + \theta_{sa}$$

(a)

Units mounted in the center of square sheets of 1/8-inch thick bright aluminum. Heat sinks were held vertically in still air. (Heat sink area is twice the area of one side.)

Experimental average
$$\theta_{sa} = 32.6A^{-0.472}$$
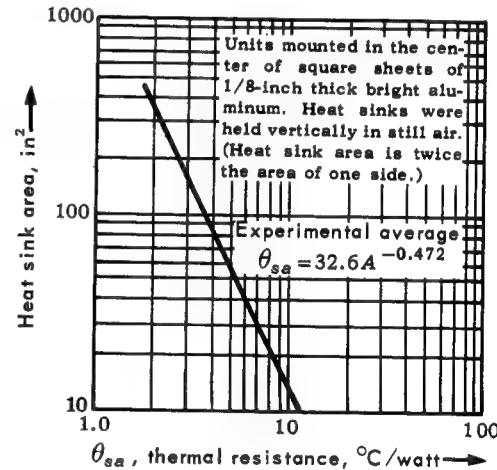
(b)

Kit No.	Insulating Washer	Typical Mounting Thermal Resistance (θ_{cs}) °C/w (includes contact resistance)	
		Dry	With DC4*
–	No insulator	0.20	0.10
MK-10	Teflon	1.45	0.80
MK-15	Mica	0.80	0.40
MK-20	Anodized Aluminum	0.40	0.35

*DC4 is Dow Corning No. 4 Silicone Lubricant. The use of the DC4 or equivalent is highly recommended especially for high power applications. The grease should be applied in a thin layer on both sides of the washer. When transistors are replaced in the sockets a new layer of the grease should be added.

(c)

Fig. 7.3 Basic components of thermal resistance. (a) The resultant thermal resistance is the sum of the separate series components. (b) Thermal resistance to the environment of an aluminum plate. (c) Junction to case resistances of typical Motorola components.

vironment. Figure 7.3 shows the series addition of thermal resistances, as well as typical numerical values. Based on these considerations,

$$T_{j\,max} - T_a = P_C\,\theta_{ja},$$

where P_C = maximum permissible collector junction dissipation (watt), $T_{j\,max}$ = maximum permissible junction temperature (°C), T_a = ambient temperature (°C), and θ_{ja} = total thermal resistance from junction to environment (°C/watt).

Saturation is another limiting transistor characteristic (Fig. 7.1). In the saturation region, V_{CE} falls below the value required for proper transistor action. Since this region is bounded by an approximately straight line whose inverse slope has the dimensions of ohms, we may define a *saturation resistance*, R_S.

Figure 7.1 also shows a *cut-off* region. When $I_C < I_{CBO}$, I_E reverses sign, the emitter-base diode blocks, and transistor action ceases. At $I_C = I_{CBO}$, $I_B = -I_{CBO}$ and $I_E = 0$. The transistor is said to be *cut-off*. The transistor can be driven to this condition if the driving source supplies a negative base current.

Thermal runaway, covered in Chap. 5, sets a further limit on transistor operation. For safest results, the thermal runaway condition should not exist anywhere on the load line. Thermal runaway cannot exist if $V_{CE} \leq \frac{1}{2} V_{CC}$.

Also relative to some of the above items is *distortion*, which is often a limiting factor in transistor power amplifier design. While theoretically it is possible to operate between points P_1 and P_2 on the load line of Fig. 7.1, distortion is considerably less for operation between points P_3 and P_4.

PROBLEM 7.1 Collector power dissipation in a transistor is given as the product of collector current and collector-base voltage, or $P_C = V_{CB}I_C$.[*] The locus of constant power dissipation may be plotted on the common-emitter collector characteristics as a hyperbola:

$$I_C = \frac{P_C}{V_{CB}} \approx \frac{P_C}{V_{CE}}. \tag{7.5}$$

Show that maximum power output is equal to $1/2\,P_C$, and that the load line is tangent to the hyperbola corresponding to the maximum permissible transistor dissipation. Neglect leakage current and saturation voltage.

Solution: Refer to Fig. 7.4. The equation for the load line is

$$I_C = I_{C_{max}} - \frac{V_{CE}}{R_L}.$$

where $R_L = V_{max}/I_{C_{max}}$. Since the constant power hyperbola is defined by (7.5), we may solve for V_{CE}:

$$\frac{P_C}{V_{CE}} = I_{C_{max}} - \frac{V_{CE}}{R_L}. \tag{7.6}$$

Equation (7.6) is a quadratic. Solving for V_{CE},

$$\frac{V_{CE}^2}{R_L} = V_{CE}\,I_{C_{max}} - P_C = 0,$$

or

$$V_{CE} = \frac{+I_{C_{max}} \pm \sqrt{I_{C_{max}}^2 - \dfrac{4\,P_C}{R_L}}}{\dfrac{2}{R_L}}.$$

---

[*]Dissipation at the emitter-base junction is usually negligible compared with dissipation at the collector-base junction.
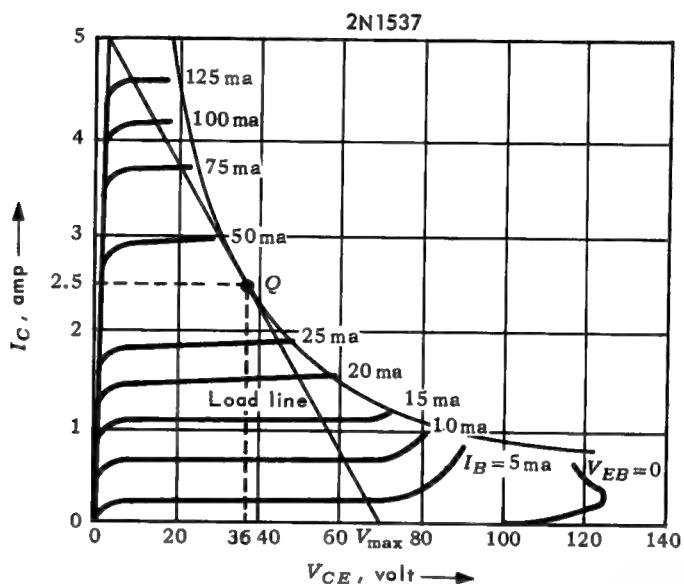
Fig. 7.4 Collector characteristics of the common-emitter circuit with superimposed load line and constant power hyperbola.

Since the load line and hyperbola intersect only at the point of tangency, the radical term goes to zero, and

$$I^2_{C_{max}} = 4 \frac{P_C}{R_L},$$

or

$$P_C = \frac{1}{4} I^2_{C_{max}} R_L .$$

The load power for sinusoidal signals is given as

$$P_L = \left(\frac{I_{C_{max}}}{2\sqrt{2}} \right) \left(\frac{V_{max}}{2\sqrt{2}} \right) = \frac{1}{8} V_{max} I_{C_{max}} . \qquad (7.7)$$

Changing parameters,

$$P_L = \frac{1}{8} I^2_{C_{max}} R_L . \qquad (7.8)$$

Comparing transistor dissipation and load power,

$$P_L = \frac{1}{2} P_C, \qquad (7.9)$$

This relationship is true regardless of R_L, so long as the load line is tangent to the P_C curve.

An elementary design procedure to follow is to draw a load line on the family of collector characteristics, tangent to the hyperbola of permissible power dissipation. This will insure that the maximum rated collector dissipation for the transistor is never exceeded.

PROBLEM 7.2   Design the power amplifier circuit of Fig. 7.5 for maximum power

output using the transistor characteristics of Fig. 7.6. The additional parameters are

$$T_{j\,max} = 80\,°C,$$
$$T_a = 25\,°C,$$
$$\left. \begin{array}{l} \theta_{jc} = 0.6\,°C/w, \\ \theta_{cs} = 0.2\,°C/w, \\ \theta_{sa} = 0.5\,°C/w. \end{array} \right\} \text{ See Fig. 7.3}$$

Use approximate methods of analysis. Neglect distortion and leakage currents.
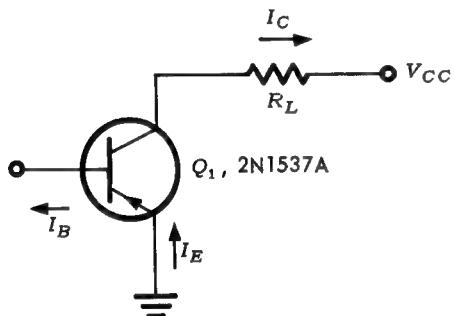
Fig. 7.5 Simplified power amplifier circuit.
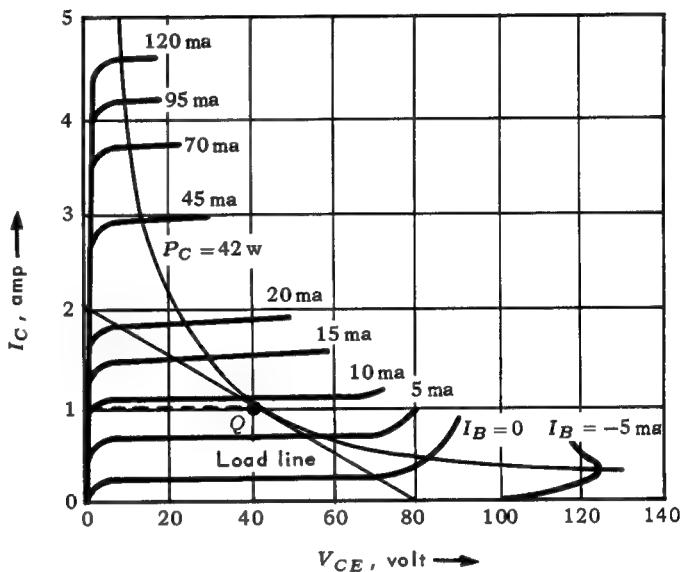
Fig. 7.6 Superimposed load line and $P_C = 42$ w hyperbola. The current at $Q = 1.05$ a.

Solution: First determine the permissible power dissipation. Total thermal resistance θ_{ja} is $\theta_{ja} = 0.6 + 0.2 + 0.5 = 1.3\,°C/w$. Hence,

$$P_C = \frac{T_{j\,max} - T_a}{\theta_{ja}} = \frac{80 - 25}{1.3} \cong 42 \text{ w.}$$

The hyperbola corresponding to this power is plotted on Fig. 7.6. A load line ($R_L = 38\,\Omega$) is sketched from $V_{max} = 80$ v tangent to the hyperbola, and the operating point Q is noted. This load line avoids both the high-voltage and high-current regions of the characteristics, where excessive curvature occurs.

Maximum load power, from (7.9), is $1/2\,P_C = 42/2 = 21$ w. Total quiescent power, from the load line, is

$$P_{TOT} = V_{CC} \times I_{CQ} = 80 \times 1.05 = 84 \text{ w.}$$

This high input power is required since 42 w are dissipated in R_L. To avoid this dissipation component, power amplifier stages almost always use transformer coupled outputs.

PROBLEM 7.3 In the circuit of Fig. 7.7, the transistor is operated at the same quiescent point as in Prob. 7.2. What is the total quiescent power?

Solution: Assuming an ideal transformer, the d-c load line sees only the transistor drop, and extends from $V_{CC} = 40$ vertically to Q. The a-c load line passes through Q as before. Power input is half of the previous value, or 42 w, corresponding to the maximum transistor dissipation.
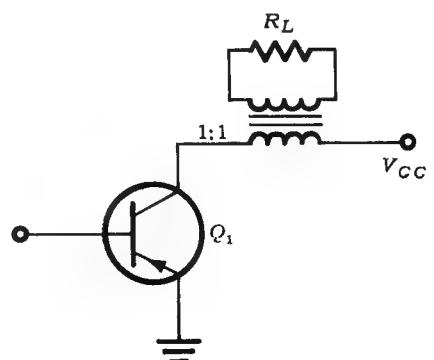

Fig. 7.7 Power amplifier circuit using transformer-coupled output.

7.2 Distortion

Fig. 7.8 The fall-off in h_{FE} at high I_C is a distortion-producing factor in power amplifiers.

Although one avoids the region of collector current multiplication, where I_C increases rapidly with increasing collector voltage, there are nevertheless two additional factors introducing distortion:

1. The rapid fall-off of h_{FE} at high I_C (see Fig. 7.8).
2. The highly nonlinear I_B vs. V_{EB} characteristic (see Fig. 7.9a).

From inspection of the above two figures, it becomes apparent that the two components of distortion-generating nonlinearity tend to cancel one another. The resultant I_C vs. V_{EB} characteristic is more linear than either component. Figure 7.10 shows this characteristic for the 2N1537A germanium power transistor. The ratio $g_{FE} = I_C/V_{BE}$, the *transconductance*, is the parameter used to describe this type of curve. Operation at a bias voltage of $V_{BB} \cong 1.1$ v leads to excellent linearity for the approximate range, $0.3 < V_{EB} < 2.0$ v, thus permitting a 1.7 v peak-to-peak input voltage swing.

In the above instance, the transistor base is driven from a low-impedance voltage source. For other transistors, optimum linearity may be obtained at some particular value of driving resistance. As an extreme condition, observe the "reverse" nature of the resulting distortion in Fig. 7.9b when driving from a sinusoidal *current source*, where V_{BE} (and I_C) take on a decidedly nonsinusoidal character.

(b)

Fig. 7.9 (a) Base current distortion with low impedance source (voltage drive) for the 2N1537A transistor. (b) Distortion in output current of the 2N1537A transistor with sinusoidal base current drive and high impedance source.
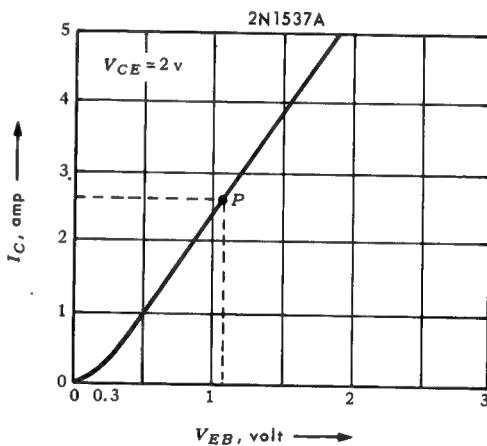
Fig. 7.10 A plot of collector current I_C vs. emitter-base voltage V_{EB}.

PROBLEM 7.4 Given a set of transistor common-emitter collector and input characteristics, devise a simple graphical construction for determining output voltage distortion in the circuit of Fig. 7.11.

Solution: The required construction is shown in Fig. 7.12. Note how selection of the driving or source resistance R_s and load resistance R_L can lead to minimization of distortion through reduction and cancellation of distortion components.

As previously noted, the load resistance R_L is wasteful in dissipating d-c quiescent power, so that transformer coupling to the load is normally used. The transformer primary d-c resistance leads to a much smaller quiescent power loss. Figure 7.13 shows a transformer-coupled amplifier. Note that R_E is added for bias
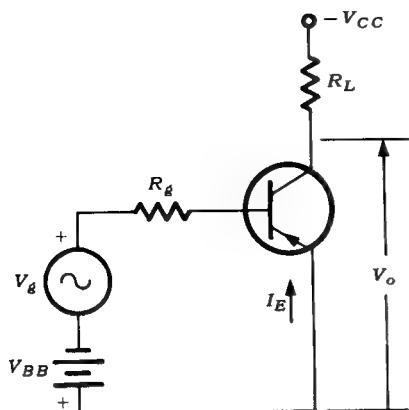
Fig. 7.11 Biased power stage with quiescent current going through the load. (See Prob. 7.4.)
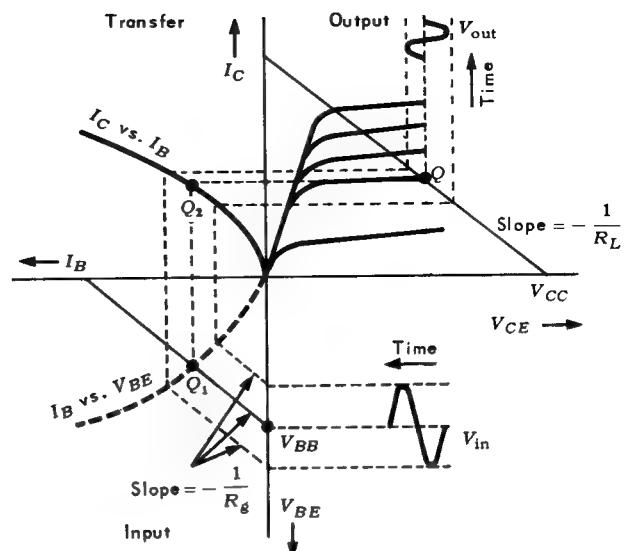

Fig. 7.12 Graphical analysis of typical operating conditions using current gain curves.

stability. This is usually not by-passed in power amplifiers due to the awkwardly large size of the required capacitor. In addition, an unby-passed R_E will provide improved a-c performance. Though gain is reduced, distortion and gain stability are improved.

The circuit of Fig. 7.13 may be investigated in nearly the same manner as that of Fig. 7.11. The significant difference is that the input to the base now includes the R_E drop as well as V_{BE}.

PROBLEM 7.5 Devise a simple graphical construction relating output voltage to applied base voltage for the circuit of Fig. 7.13. Use the same transistor characteristics and general approach as in Prob. 7.4.

Solution: Refer to Fig. 7.14. Note the d-c and a-c load lines superimposed on the collector characteristics. The I_C vs. I_B curve is easily plotted as before. For each I_C, there is a drop $I_E R_E \cong I_C R_E$ in the emitter resistor. This drop must be
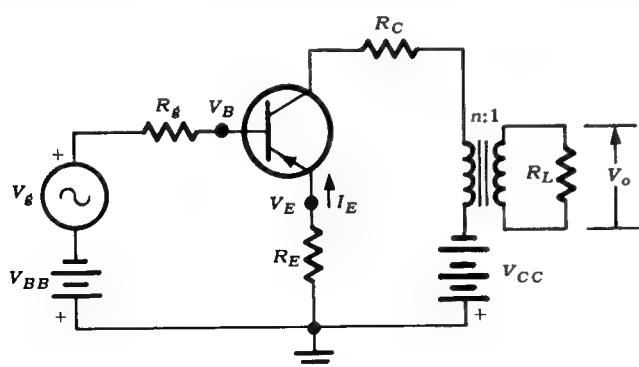

Fig. 7.13 Typical bias amplifier with transformer-coupled output.
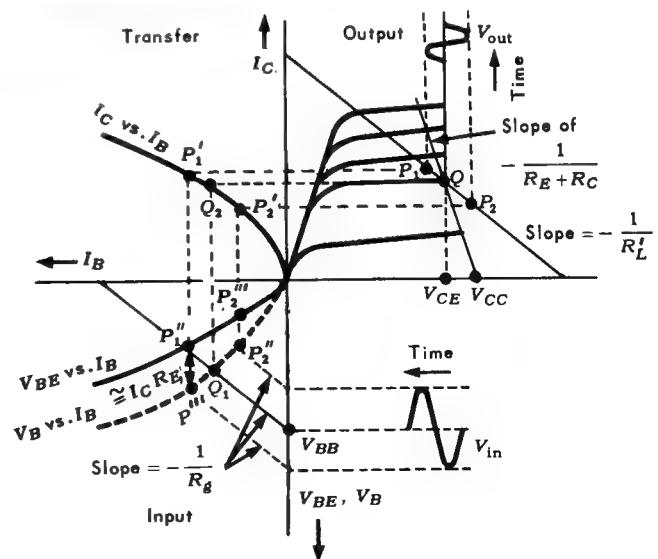
Fig. 7.14. Solution to Prob. 7.5.

added to V_{BE} at corresponding points to come up with the resultant V_{BE} vs. I_B characteristic. Figure 7.14 also shows how input and output voltages for the amplifier of Fig. 7.13 are compared in order to determine gain, power output, and distortion.

In the accurate analysis of power transistor circuits, it is best to use transistor characteristics corresponding to the actual operating temperatures. These are often unavailable, however, in the manufacturers' literature. Figure 7.15 shows how the significant transistor characteristics vary typically with temperature, for estimating the order of magnitude of inaccuracies which might be expected from using room temperature characteristics.

2N1167
Collector current
vs. base current
(a)

2N1167
Current gain
vs. collector current
(b)

2N1167
Collector current
vs. base-emitter voltage
(c)

2N1167
Base-emitter voltage
vs. base current
(d)

h_{FE} vs. temperature
(e)

β_{FE} vs. temperature
(f)
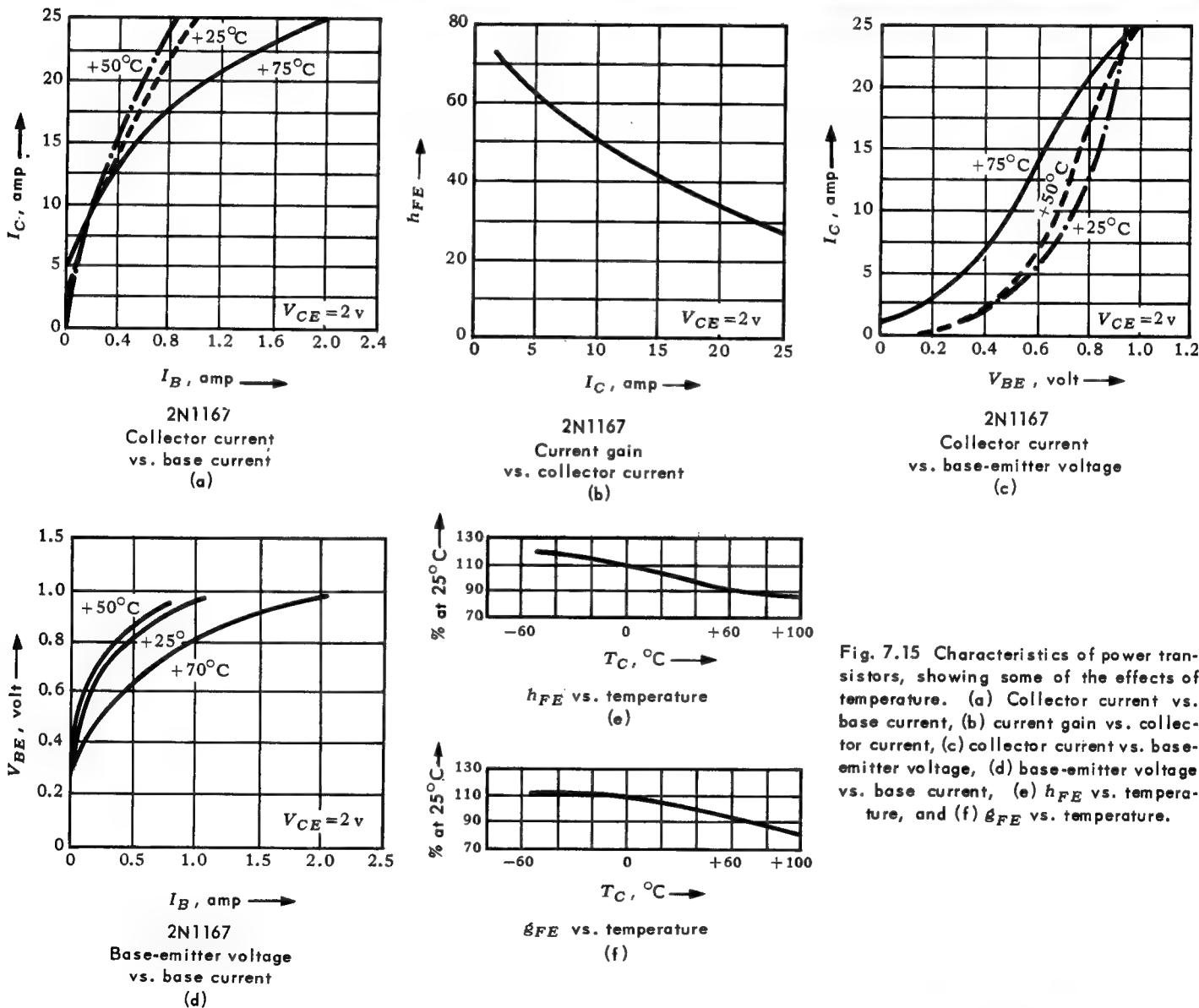
Fig. 7.15 Characteristics of power transistors, showing some of the effects of temperature. (a) Collector current vs. base current, (b) current gain vs. collector current, (c) collector current vs. base-emitter voltage, (d) base-emitter voltage vs. base current, (e) h_{FE} vs. temperature, and (f) β_{FE} vs. temperature.

PROBLEM 7.6 Design a common-emitter power output stage to deliver 17 w of maximum power to a 10 Ω loudspeaker coil. Ambient temperature is 25 °C; maximum junction temperature is limited to 80 °C. Use a 2N1537A germanium transistor mounted on a cooling plate which results in $\theta_{ja} = 1.3$ °C/w of dissipated power. Check bias stability and the possibility of thermal runaway. Assume $I_{CBO} = 5$ ma

at 80°C. Aim for a stability factor S of about 5. Assume that the output coupling transformer d-c resistance is 10% of the load resistance referred to the primary.
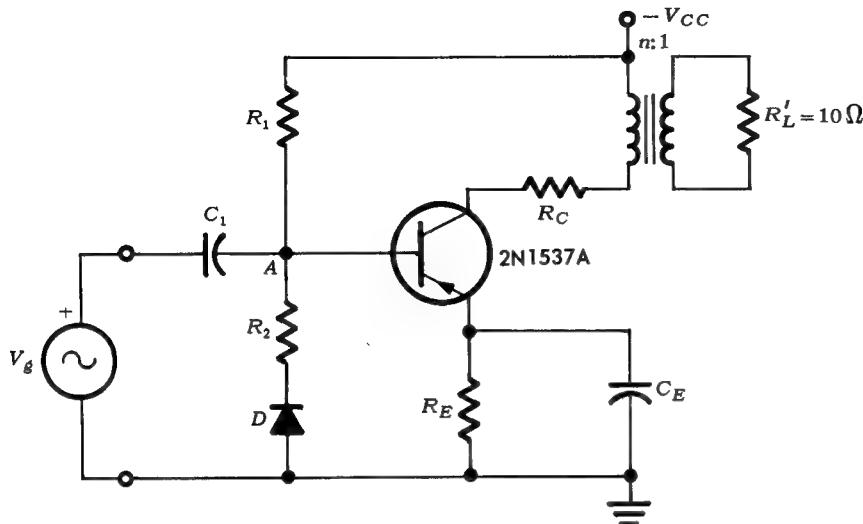

Fig. 7.16 Transformer-coupled power amplifier. (See Prob. 7.6.)

Solution: Use the configuration of Fig. 7.16. Note the unby-passed emitter resistor R_E used for bias stabilization. Now following the procedures of Prob. 7.2, we establish a Q-point at $V_{CE} = 40$ v and $I_C = 1.05$ a. To minimize shifts in the operating point with temperature, restrict ΔI_C due to increased I_{CBO} to less than 25 ma, corresponding to a maximum S of 5. Letting the reflected load = 38 Ω, the transformer resistance is $R_C = 0.1 \times 38 = 3.8$ Ω. Resistance R_E may be chosen on the basis of its quiescent power loss. To minimize power dissipation in R_E, let $R_E = 4$ Ω. Then,

$$S = \frac{4 + R_B}{\dfrac{4 + R_B}{1 + h_{FE}}} = 5, \qquad [4.38]$$

where

$$R_B = \frac{R_1 R_2}{R_1 + R_2}.$$

Since $h_{FE} \cong 100$ at the Q-point (see Fig. 7.8), we may substitute and solve for $R_B = 16.8$ Ω maximum for $S = 5$. From the I_C vs. V_{BE} curve (Fig. 7.10), at $I_C = 1.05$ a at 25°C, $V_{BE} = 0.5$ v. The voltage at point A is therefore

$$V_A = 1.05 R_E + V_{BE} = 4.2 + 0.5 = 4.7 \text{ v}.$$

However, the diode drop cancels V_{BE}, so that a drop of only 4.2 v across R_2 is required. Since

$$V_{CC} = V_{CE} + R_C I_C + R_E I_C = 40 + (3.8 \times 1.05) + 4.2 = 48.2 \text{ v},$$

we may solve for the resistances R_1 and R_2:

$$R_1 = 193 \ \Omega,$$

$$R_2 = 18.4 \ \Omega.$$

The current in the bias network is approximately

$$\frac{48.2 - 4.2}{193} = 0.23 \text{ a.}$$

Since this is quite large, we might wish to redesign the bias network, contenting ourselves with an increased value of S, or else use a separate bias supply as shown in Fig. 4.22.

From Prob. 7.2, $R_L = 38\ \Omega$ has been determined as optimum, and since $R_C = 3.8\ \Omega$, the load impedance observed at the transformer primary is $38 - 3.8 = 34.2\ \Omega$. The transformation ratio, primary to secondary, is therefore $\sqrt{34.2/10} \doteq 1.85$.

The rms collector current is

$$\frac{\Delta I_{C_{\text{p-p}}}}{2\sqrt{2}},$$

where $\Delta I_{C_{\text{p-p}}}$ is the peak-to-peak collector current. Thus, maximum load power is

$$\left(\frac{2.05}{2\sqrt{2}}\right)^2 \times 34.2 = 18 \text{ w}.$$

To check for the possibility of thermal runaway, use (4.49):

$$\frac{1}{S\,\theta_{ja}} \geq 0.07\, I_{CBO}\left[V_{CC} - 2\,I_C\,(R_E + R_C)\right].$$

Substituting numerical values,

$$\frac{1}{5 \times 1.3} = 0.15 > 0.07 \times 5 \times 10^{-3}\,[48.2 - 2\,(1.05)\,(4 + 3.8)] = 0.014.$$

The safety factor is greater than 10. This should provide sufficient margin, even allowing for the approximate nature of the calculation.

PROBLEM 7.7   In the amplifier of Prob. 7.6, determine the maximum current output without clipping due to saturation. Also determine the distortion for this output.

Solution: Figure 7.17 gives the transistor collector characteristics with d-c and a-c load lines and the quiescent operating point Q (which was determined in Prob. 7.2). Figure 7.17 also shows I_C vs. V_{EB} ($V_{EB} = -V_{BE} =$ a positive number).
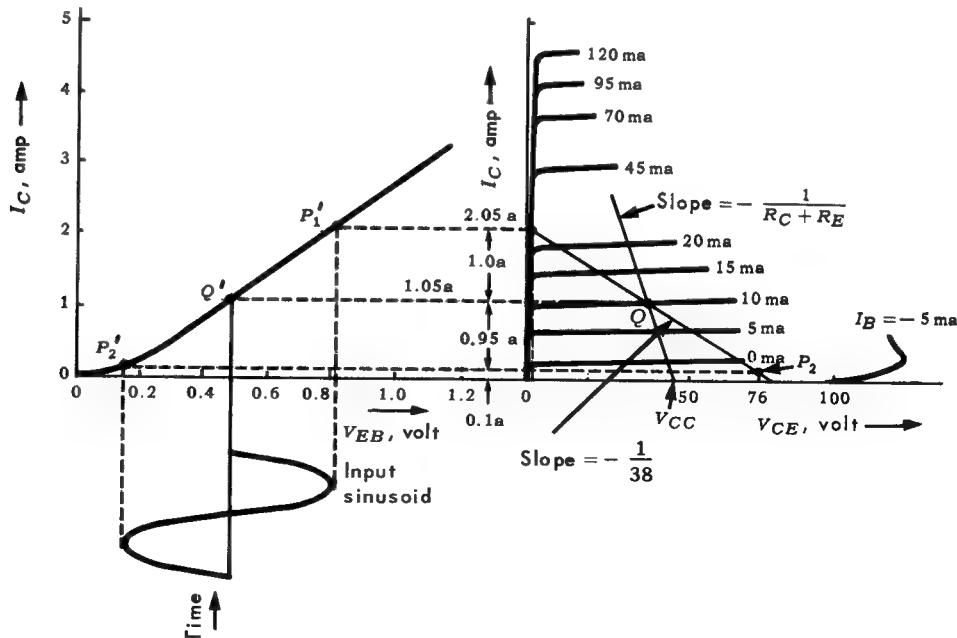

Fig. 7.17 Excursion of collector current with sinusoidal base-emitter voltage drive.

From the saturation point P_1, we determine V_{EB} at saturation. If we apply a symmetrical sinusoidal base-emitter voltage about Q from a zero impedance source, point P_2 is established. The output I_C varies from 0.1 a to 2.05 a about $I_C = 1.05$ a at point Q. This is the range of the a-c output current swing.

Now determine distortion. This is accomplished by the methods of Appendix D. Use the following simplified formula, applicable to waves exhibiting primarily a moderate degree of second harmonic distortion:

$$D_2 = \frac{B_2}{B_1} \times 100 = \frac{I_1 + I_2 - 2 I_Q}{2(I_2 - I_1)} \times 100 .$$

In the present instance, $I_1 = 0.1$ a, $I_2 = 2.05$ a, and $I_Q = 1.05$ a. Substituting, $D_2 = 1.3\%$, second harmonic distortion.

PROBLEM 7.8 For the amplifier of Prob. 7.6, determine the driving current and voltage.

Solution: Refer to Fig. 7.17, and interpolate to establish base currents:

$$I_C = 0.1 \text{ a}, \qquad I_B = -3 \text{ ma},$$

$$I_C = 1.05 \text{ a}, \qquad I_B = 10 \text{ ma},$$

$$I_C = 2.05 \text{ a}, \qquad I_B = 29 \text{ ma}.$$

Peak-to-peak base current is $29 - (-3) = 32$ ma. (From the above tabulation, note that base current is not sinusoidal, although input and output voltages are nearly so.) Peak-to-peak base-emitter voltage, from Fig. 7.17, is 0.7 v. Thus, input power may be approximately calculated:

$$\text{Input power} = \frac{0.7}{2\sqrt{2}} \times \frac{0.032}{2\sqrt{2}} = 2.8 \text{ mw},$$

$$\text{Power gain} = \frac{18}{0.0028} = 6400.$$

This power calculation neglects distortion. However, it is certainly sufficiently accurate for the purposes of designing a *driver stage* to precede the power stage.

7.3 Power Amplifier Design Equations

Manufacturers' data on power transistors are rarely sufficient for meticulous design calculations. The principal deficiencies relate to differences among transistors of the same type, and the effects of temperature. As a result, practical design procedures are based on idealized transistor characteristics. The design may then be refined by more detailed graphical methods and/or laboratory adjustments.

In this section, we examine the idealized transistor characteristics. Derived design formulae are tabulated, and a complete list is developed. The formulae are summarized in Table 7.1.

Refer to the idealized characteristics of Fig. 7.18 and note the following:

1. Total equivalent saturation resistance $R_T = R_S + R_E + R_C$.

2. Maximum usable voltage $BV_{max} = 2 V_{CC} - V_{CS}$.

3. A-c power output $P_o = \left(\dfrac{V_{CC} - V_{CS}}{2} \right) I_Q$, or $P_o = \dfrac{(V_{CC} - V_{CS})^2}{2 R_L'}$.

4. $V_{CC} = \dfrac{BV_{max} + 2 R_T I_Q}{2}$.

TABLE 7.1   Class A amplifier design formulae.*

Item	Formula $(R_T \neq 0)$	Formula $(R_T = 0)$	
$P_{o_{max}}$	$\dfrac{BV_{max}I_Q}{4} - \dfrac{R_T I_Q^2}{2}$	$\dfrac{P_C}{2}$	(7.10a)
$P_{CE_{max}}$	$V_{CC}I_Q = P_C$	P_C	(7.10b)
V_{CC}	$\dfrac{BV_{max} + 2R_T I_Q}{2}$	$\dfrac{BV_{max}}{2}$	(7.10c)
η_{max}	$0.5\,\dfrac{R_L'}{R_L' + 2R_T}$	0.5	(7.10d)
R_L'	$\dfrac{BV_{max}}{2I_Q} - R_T$	$\dfrac{BV_{max}^2}{4P_C}$	(7.10e)
$\dfrac{P_{o_{max}}}{P_{CE_{max}}}$		0.5	(7.10f)
$I_{Q(opt)}$	$\dfrac{BV_{max}}{4R_T}\left[\sqrt{1 + \dfrac{16 P_C R_T}{BV_{max}^2}} - 1\right]$	$I_Q = \dfrac{2P_C}{BV_{max}}$	(7.10g)
$P_{CC_{max}}$	$V_{CC}I_Q = P_C$	$V_{CC}I_Q = P_C$	(7.10h)
I_{max}	$2I_Q$	$2I_Q$	(7.10i)

*Transformer coupling to load assumed.

$R_T = R_S + R_E + R_C$

Slope $= -\dfrac{1}{R_L'}$

$i_c = I_C \sin \omega t$

R_S = Transistor saturation resistance
R_E = Equivalent d-c emitter circuit resistance
R_C = d-c resistance of transformer primary winding

Fig. 7.18 Load line construction for Class A amplifier operation.

By integrating the expression for instantaneous transistor power over a complete sinusoidal cycle of collector current, the following formula is obtained:

$$P_{CE} \text{ (transistor dissipation)} = V_{CC} I_Q - \frac{I_C^2}{2}\left(\frac{V_{CC} - V_{CS}}{I_Q}\right). \tag{7.11}$$

This expresses the almost obvious relationship that transistor dissipation is the difference between the (approximately) constant input power and the output power. Dissipation is minimized when power output is at a maximum.

Within limits imposed by BV_{max} and $I_{C_{max}}$, the transistor dissipation is determined by the hyperbola of constant power dissipation. The approximate design formulae for setting the operating point and estimating efficiency are listed in Table 7.1.


Fig. 7.19 Single transistor power amplifier stage with transformer-coupled load. (See Prob. 7.9.)

PROBLEM 7.9   Using a 2N930 transistor in the circuit of Fig. 7.19 having a thermal resistance of 500°C/w and a permissible junction temperature of 175°C, calculate $I_{Q\,opt}$, V_{CC}, P_o, η (the collector circuit efficiency), and R_L'. Use $BV_{max} = 40$ v, $R_S = 50\ \Omega$, and assume an ambient temperature of 70°C.

Solution: Start by determining the permissible transistor dissipation:

$$175°C - 70°C = 500°C/w \times P_C.$$

Solving, the maximum permissible dissipation P_C is 0.21 w. Also,

$$R_T = R_C + R_E + R_S = 150 + 50 + 50 = 250\ \Omega.$$

To determine the required performance characteristics, merely substitute in the formula of Table 7.1:

$$I_{Q\,opt} = \frac{BV_{max}}{4R_T}\left(\sqrt{1 + \frac{16 P_C R_T}{BV_{max}^2}} - 1\right). \tag{7.10g}$$

Substituting numerical values, $I_{Q\,opt} = 9.4$ ma. Continuing, we obtain by direct substitution the following quantities:

$$V_{CC} = \frac{BV_{max} + 2\,R_T\,I_Q}{2} = 22.3 \text{ v}, \qquad [7.10c]$$

$$P_o = \frac{BV_{max}\,I_Q}{4} - \frac{R_T\,I_Q^2}{2} = 0.084 \text{ w}, \qquad [7.10a]$$

$$R_L' = R_L = \frac{BV_{max}}{2\,I_Q} - R_T = 2130 \;\Omega, \qquad [7.10e]$$

$$\eta = \frac{R_L'}{2\,(R_L' + 2\,R_T)} = 0.405, \text{ or } 40.5\%. \qquad [7.10d]$$

7.4 Common-Base Connection

The common-base collector characteristics of transistors with high h_{FE} are quite linear as shown in Fig. 7.20. In contrast with h_{FE}, h_{FB} is almost exactly unity over the full operating range of the transistor. For the common-base connection, leakage current is negligible. The maximum voltage (BV_{CBO}) is greater than for the common-emitter or common-collector configurations. Because I_C is very nearly equal to I_E, the only distortion introduced is by the nonlinearity of the emitter input circuit. If the input is a high impedance current source, such as is usually the case when the input is not transformer-coupled, distortion is very low. If a transformer-coupled input is used to increase power gain, distortion is sharply increased. To determine this distortion, the V_{BE} vs. I_E characteristic, not usually available, is required. However, the V_{BE} vs. I_C characteristic may be used without significant error.
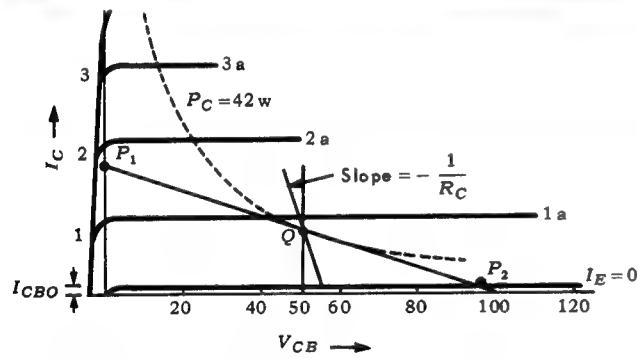

Fig. 7.20 Common-base characteristics of the 2N1537A transistor at $T_j = 80°C$ and $BV_{CBO} = 100$ v.
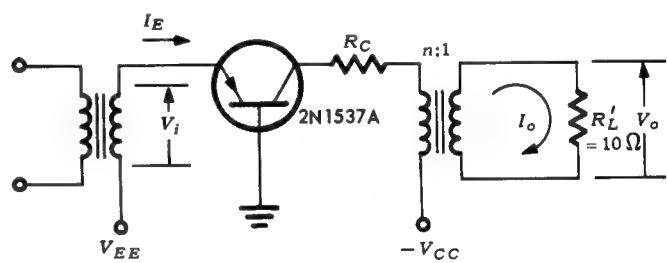
Fig. 7.21 Common-base transformer-coupled output stage, $BV_{CBO} = 100$ v.

PROBLEM 7.10 Design a transformer-coupled common-base power output stage under approximately the conditions of Prob. 7.6. Assume the transformer d-c resistance is 10% of the reflected load resistance and determine the optimum output transformer ratio. Calculate maximum load power, distortion, input current, voltage, and power, and approximate input impedance, with current drive and voltage drive. Determine V_{CE} and compare with the common-emitter amplifier of Prob. 7.6.

Solution: The circuit configuration is shown in Fig. 7.21. From Prob. 7.6 and the manufacturer's data in Appendix A, extract the following parameters:

$T_j = 80°C$, allowable junction temperature,

$T_a = 25°C$, ambient temperature,

$\theta_{ja} = 1.3°C/w$, thermal resistance,

$$I_{CBO} = 5 \text{ ma at } 80°C,$$

$$BV_{CBO} = 100 \text{ v.}$$

Using these parameters, calculate permissible junction dissipation:

$$P_C = \frac{T_J - T_a}{\theta_{ja}} = \frac{80 - 25}{1.3} = 42 \text{ w.}$$

Now refer to Fig. 7.20 where the 5 ma I_{CBO} is shown on an exaggerated scale, since otherwise it would not be discernible. For the common-base connection, voltage breakdown occurs at BV_{CBO}. A load line may therefore originate at 100 v on the horizontal axis. For a permissible transistor dissipation of 42 w, the load line must be tangent to the $P_C = 42$ w hyperbola at Q (50 v, 0.84 a). This is the operating point. The load line, therefore, corresponds to

$$R_L = \frac{50}{0.84} = 59.5 \text{ }\Omega.$$

We have assumed that 10% of the apparent load resistance occurs in the output transformer winding, a reasonable assumption related to transformer efficiency. Thus, R_C, the transformer resistance, is 5.95 Ω, and the effective load resistance must be $59.5 - 5.95 \cong 53.5$ Ω. Since the load is actually a 10 Ω resistor, the turns ratio may be determined:

$$n = \sqrt{\frac{53.5}{10}} = 2.3.$$

Calculate power output P_o to the load. The rms current is $I_o = \dfrac{0.84}{\sqrt{2}} = 0.6$ a (neglecting distortion). Therefore,

$$P_o = \left(\frac{0.84}{\sqrt{2}}\right)^2 \times 53.5 = 19.2 \text{ w.}$$

Saturation actually reduces the power output slightly.

Now establish V_{CC}:

$$V_{CC} = V_Q + R_C I_Q = 50 + 5.95 \, (0.84) = 55 \text{ v.}$$

For sinusoidal input current, output distortion is negligible. This is a direct consequence of the current gain characteristic of the common-base circuit, where

$$I_C = \frac{h_{FE}}{1 + h_{FE}} I_E, \qquad h_{FE} \gg 1.$$

However, there is no current amplification.

The driving voltage, on the other hand, is decidedly nonsinusoidal. The V_{EB} vs. I_C curve, Fig. 7.22, is used instead of the usually unavailable V_{EB} vs. I_E curve, with little loss of accuracy. Note that the curves used should correspond to the actual junction temperature.

From the operating points superimposed on Fig. 7.22, the evidence of voltage distortion is apparent. The lower voltage extreme is 0.45 v below the quiescent value, while the upper extreme is 0.3 v above the quiescent value. Using our approximate formula for second-harmonic distortion from Appendix D,

$$D_2 \, (\%) = \frac{E_1 + E_2 - 2E_Q}{2(E_2 - E_1)}.$$

Substituting numerical values,

$$|D_2| \, (\%) = \frac{0 + 0.75 - 2\,(0.45)}{2\,(0.75 - 0)} \times 100 = |-10|\% = 10\%.$$

The negative sign has no meaning; the second harmonic distortion is 10%.

The fundamental component is similarly evaluated:

$$\text{Fundamental} = \frac{E_1 + E_2}{2};$$

then substituting, the fundamental voltage is $0 + 0.75/2 = 0.375$ v peak, or 0.265 v rms. Since $I_i \cong I_o = 0.6$ a rms, input power is

$$P_i = 0.265 \times 0.6 = 0.158 \text{ w.}$$

Power gain is $19.2/0.158 = 120$. This is much less than the power gain of the comparable common-emitter circuit, explaining why the common-base circuit is not often used.

Input impedance is readily estimated:

$$R_i = \frac{0.265 \text{ v}}{0.6 \text{ a}} = 0.44 \ \Omega.$$

This is much lower than for the common-emitter connection.

The only significant advantage over the common-emitter connection, apart from the somewhat increased output power rating, is the reduced distortion. This, however, can also be achieved by negative feedback from the power stage output to earlier amplifier stages (see Chap. 8). The high input current requirement of the common-base amplifier is a serious disadvantage.

Now consider the same common-base amplifier circuit, Fig. 7.21, driven from a sinusoidal voltage source. This could be, for instance, a transformer input with a sufficient voltage step-down to reduce generator resistance R_g to a negligible value.
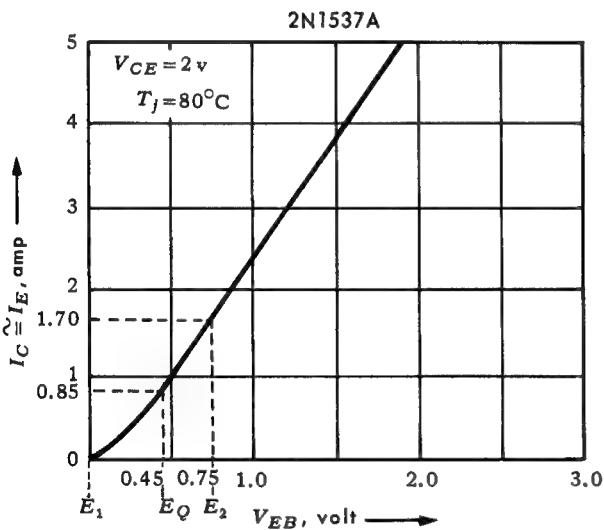

Fig. 7.22 Emitter-base voltage vs. collector current for $T = 80°C$.
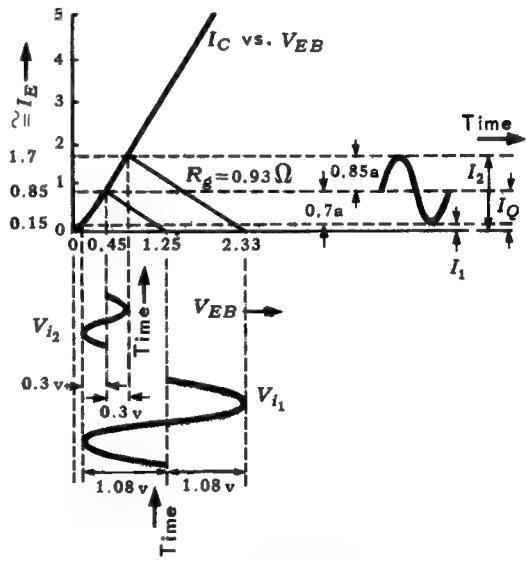
Fig. 7.23 Influence of generator source resistance on a 2N1537A transistor stage characteristic.

Figure 7.23 shows how the now distorted input current is obtained by graphical construction. From the figure, we see that a maximum $V_i = 0.3$ v peak (corresponding to 0.212 v rms), which avoids saturation clipping. Second harmonic current distortion is (from Appendix D)

$$D_2 \ (\%) = \frac{I_1 + I_2 - 2I_Q}{2(I_2 - I_1)} \times 100.$$

Substituting numerical values from Fig. 7.23, $D_2 = 10\%$.

Neglecting harmonic distortion, input power is approximately $0.212 \times 0.545 = 0.115$ w. The fundamental power output is

$$P_o = (0.545)^2 \, 53.5 = 15.8 \text{ w.}$$

Thus, power gain is $15.8/0.115 = 138$.

We may see the effect of introducing some moderate value of source resistance R_g. Figure 7.23 shows an input load line corresponding to an R_g of 0.93 Ω. Input voltage must be increased to 1.08 v peak, or 0.765 v rms, leading to an increased power input, $P_i = 0.545 \times 0.765 = 0.418$ w. Distortion is essentially unaffected by introducing R_g. Much greater values, approaching a current drive input, would be required.

The input resistance for voltage drive is

$$R_i = \frac{0.212}{0.545} = 0.4 \text{ Ω,}$$

nearly the same as for current drive.

7.5 Common-Collector Power Amplifier Stage

The common-collector or emitter-follower circuit has a characteristic *voltage gain* of somewhat less than unity. The techniques for the design of common-emitter amplifiers may be directly transferred to the design of the common-collector amplifiers. The load, in effect, becomes R_g, with $R_L = 0$, and the transformer d-c resistance now serves as a d-c stabilizing emitter resistance. Input impedance approximately equal to $(1 + h_{FE})R_g$ is high. The common-collector connection is seldom used for power amplifiers.

PROBLEM 7.11 Using the 2N1537A transistor with the same characteristics as in Probs. 7.6 and 7.10, design a common-collector power stage to drive an 8 Ω loud-speaker coil without an output transformer. Calculate maximum power output, distortion, input power, and power gain. Determine V_{CC} and V_{EE}. If the transformer has a secondary resistance of 1 Ω, i.e., $R_B = 1$ Ω, calculate the stability factor S. Source impedance $R_g = 0$.

Solution: Refer to Fig. 7.24 which shows the configuration of the power-stage circuit. Using the thermal characteristics of Prob. 7.6, permissible transistor dissipation is 42 w. Now draw a load line on the collector characteristics of Fig. 7.25. Since collector and emitter currents are nearly equal, the load line is drawn to correspond to an 8 Ω load. Therefore the figure will show the load line and the operating point Q corresponding to a 42-watt dissipation. Limiting the total output signal swing to avoid clipping due to saturation, voltage ranges from 3.5 v to 36.3 v, and the current swing is 4.2 a, p-p. Collector supply voltage V_{CC} is thus 36.6 v. Neglecting distortion,

Fig. 7.24 Common-collector power stage driving an 8 Ω load.

$$P_o = \frac{33}{2\sqrt{2}} \times \frac{4.2}{2\sqrt{2}} = 17.3 \text{ w.}$$

Figure 7.26 shows the $I_E \, (\cong I_C)$ vs. V_{EB} characteristic. From this curve and the relationship

$$V_i = I_C R_E + V_{EB}$$

(V_i = base voltage), the required swing of V_i is determined as ± 17.6 v around a bias point of $V_{EE} = 17.6$ v. Because of this symmetry, there is no distortion to affect the accuracy of our calculations.
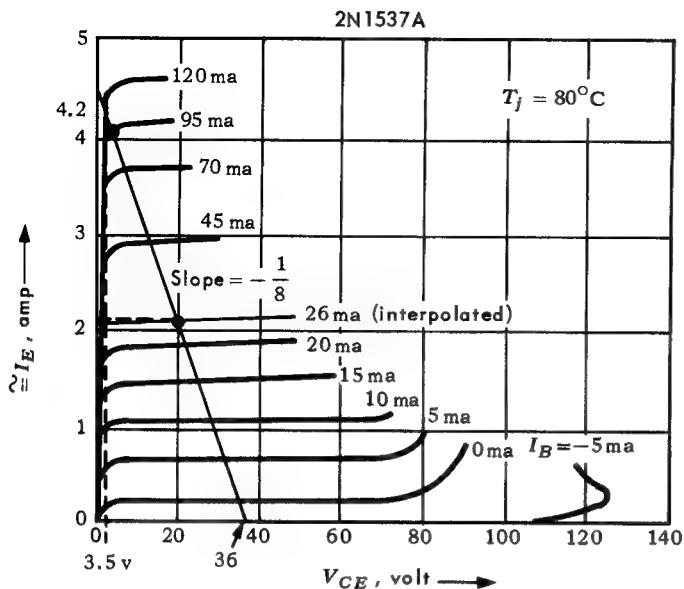
Fig. 7.25 Collector characteristics with superimposed load line for Prob. 7.11.

Fig. 7.26 Emitter-base voltage vs. collector current. (See Prob. 7.11.)

Input (base) current is readily determined from Fig. 7.25:

$$I_{B_{max}} = 0.095 \text{ a},$$

$$I_{BQ} = 0.026 \text{ a},$$

$$I_{B_{min}} = -0.005 \text{ a}.$$

It can be seen that I_B is quite nonlinear, so that a low source impedance is necessary to insure low output distortion. Using the methods already applied several times in the preceding problems, it may be determined that a 40 Ω source impedance leads to about 5% distortion. The 1 Ω transformer resistance leads to negligible distortion.

Input current is very roughly

$$\frac{0.095}{2} = 0.0475 \text{ ma peak, or } 33.5 \text{ ma rms}.$$

This neglects distortion. Thus,

$$R_i \cong \frac{\dfrac{17.6}{\sqrt{2}}}{33.5 \times 10^{-3}} = 373 \text{ Ω}.$$

Continuing,

$$P_i = \frac{17.6}{\sqrt{2}} \times 33.5 \times 10^{-3} = 0.418 \text{ w}.$$

Power gain is 41.5, by far the lowest figure of each of the transistor configurations.

To calculate S, use (4.38):

$$S \cong 1 + \frac{R_B}{R_E} = 1 + \frac{1}{8} = 1.125.$$

This low stability factor is characteristic of transformer-coupled input circuits.

To calculate collector efficiency η, note that quiescent battery power is 36.6 × 2.1 = 77 w. Efficiency, the ratio of power output to input d-c power, is 17.3/77 = 22.5%. This poor efficiency is primarily due to the d-c dissipation in the 8 Ω emitter load resistance.

7.6 Push-Pull Amplifiers

Fig. 7.27 Push-Pull transistor amplifier with transformer-coupled input and output.

For relatively high distortion-free output power, the *push-pull amplifier* is used (Fig. 7.27). As a consequence of its circuit symmetry, there exists a characteristic symmetry of the output waveform, such that even harmonic distortion components are cancelled. Additional advantages, not immediately obvious, are the d-c cancellation in the output transformer, and greatly increased efficiency as compared with single-ended devices.

Depending on the bias voltage of the circuit of Fig. 7.27, we get different *classes* of operation. These classes may be defined most easily by reference to Fig. 7.28. Classification is based primarily on the degree of clipping of collector current during operation.

The principal advantage of clipping is improved efficiency. Class AB operation is more efficient than Class A, and Classes B and C are even more efficient. However, the latter two modes lead to relatively high distortion, and are not employed except for tuned loads.

Because of the numerous advantages of the common-emitter circuit as a power stage, we will confine our discussion to this configuration. However, the methodology developed below is equally adaptable to the other basic configurations.
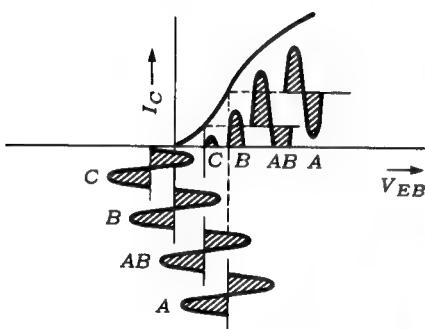
Fig. 7.28 Classes of amplifier operation determined by portion of cycle in which the transistor is cut off.

7.6a Class A Push-Pull Amplifier

Because of simplicity of design, we will initially consider Class A operation, although more efficient Class AB operation is usually preferred in practice. Actually, Class A push-pull operation is about the same as Class A operation of two separate but symmetrical transistor circuits, whose outputs are combined by the action of the output transformer.

PROBLEM 7.12 Design a push-pull Class A amplifier by combining two amplifiers of the type designed in Prob. 7.6. Draw load lines, determine its power output to a 10 Ω load, and determine its second harmonic distortion when operated to the point where clipping barely occurs (maximum output). Also determine its efficiency, and calculate the output transformer turns ratio.

Solution: The push-pull circuit is shown in Fig. 7.29. Figure 7.30 shows the *composite* transistor collector characteristics, obtained by superimposing the two sets of characteristics to show push-pull behavior. Resistances R_A and R_B are used to adjust bias, as well as to optimize diode temperature compensation. The diode provides a compensating voltage drop for the variation in V_{BE} with temperature.

From Probs. 7.6–7, the following quiescent operating conditions for the separate transistor circuits are established:

$$I_{C_1} = I_{C_2} = 1.045 \text{ a},$$

$$V_{CE} = 40 \text{ v}.$$

The voltage drive is 0.7 v p-p, and bias is adjusted for the required Q-point.

The design is similar to the design of single-ended Class A amplifiers, except for the effect of the output transformer, which couples the separate circuits. The basic transformer equation is

$$I_o = n(I_{c_1} - I_{c_2}).$$

Since the separate outputs are 180° out of phase, I_{C_1} is maximum when I_{C_2} is minimum, and vice-versa.
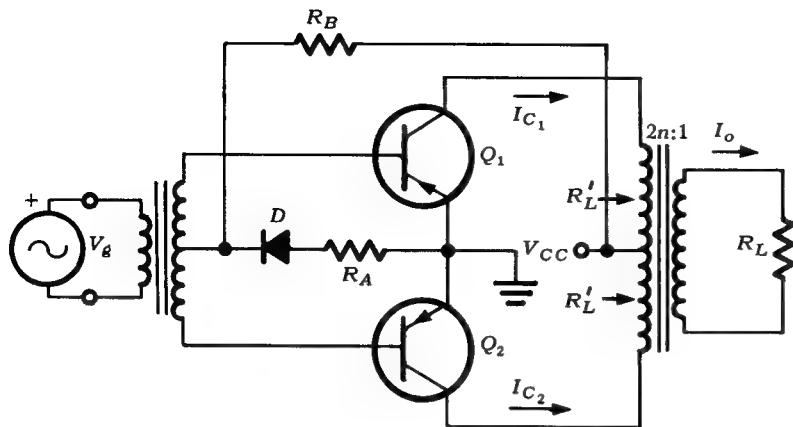
Fig. 7.29 Push-pull power amplifier showing tempera-ture-compensated bias circuit.

Fig. 7.30 Superimposed collector characteristics for evaluation of push-pull operation. Load lines are shown for a Class A circuit.

Substituting extreme values,

$$I_o = n(2.05 - 0.1) = 1.95\, n = I_2, \text{ positive maximum output},$$

$$I_o = n(0) = 0 = I_Q, \text{ quiescent output},$$

$$I_o = n(0.1 - 2.05) = -1.95\, n = I_1, \text{ negative maximum output}.$$

It may be immediately noted that current swing is double the value for the single-ended circuit. Because of the symmetry of the peak output currents, the second harmonic distortion is zero (assuming identical transistors and ideal transformers). This freedom from even harmonic distortion is characteristic of symmetrical push-pull stages.

The voltage swing across the load resistance R_L is $(38 + 38)/n$ v p-p. Calculate power output:

$$P_o = \frac{1.95\, n}{\sqrt{2}} \times \frac{38}{n \sqrt{2}} = 37 \text{ w},$$

assuming an ideal output transformer.

From Fig. 7.30, since $R_L' = 2n^2 R_L$ and $R_L = 10$, $R_L' = 38$. We may solve for the turns ratio (1/2 of primary to secondary), $n = \sqrt{1.9} = 1.38$.

With regard to efficiency, note that the output voltage swing is unchanged, and the output current swing is doubled, in comparison with a single-ended stage. Also, the supply voltage V_{CC} is unchanged, and I_Q is doubled. Thus, efficiency is the same as for a single-ended stage.

We have assumed in Prob. 7.12 that the transistor load lines are perfectly straight. This is not exactly true for push-pull amplifiers, although the deviation is usually small. The curvature is most pronounced where current gain varies substantially with I_C. Figure 7.31 shows a characteristic exhibiting relatively high curvature.

Fig. 7.31 Curved load line in push-pull transistor circuit.

PROBLEM 7.13 Draw the equivalent circuit for a push-pull Class A amplifier. Reduce it to a simple format for easy analysis.

Solution: The equivalent circuit is shown in Fig. 7.32. Because of symmetry, the circuit may be reduced to the single-transistor circuit of Fig. 7.33, where the circuit parameters are modified appropriately by factors of two. The equations for the single-transistor circuit of Fig. 7.33 are identical to the equations of the com-

Fig. 7.32 Equivalent circuit of a push-pull
Class A amplifier.
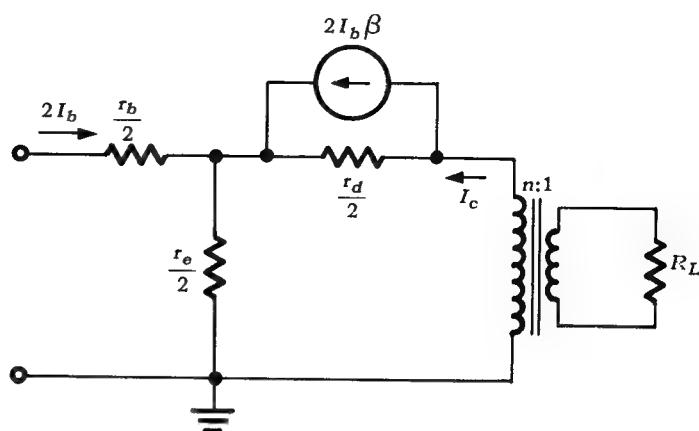
Fig. 7.33 Simplified single-transistor equivalent circuit of
push-pull Class A amplifier.

plete circuit of Fig. 7.32. The reflected load impedance is $n^2 R_L$, half of the load
for each transistor.

7.6b Class B Push-Pull Amplifier

Where high power efficiency is required, Class B opera-
tion is recommended. For Class B operation, bias is adjusted for approximately
zero quiescent current. Transistor conduction is essentially zero for half of each
cycle. However, in the push-pull connection (Fig. 7.34) with each transistor con-
ducting half the time but coupled through a common transformer to the load, the
complete output wave is generated.
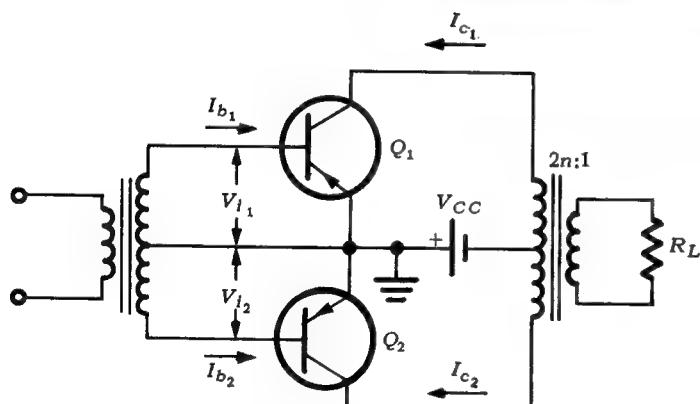
Fig. 7.34 Push-pull Class B amplifier.
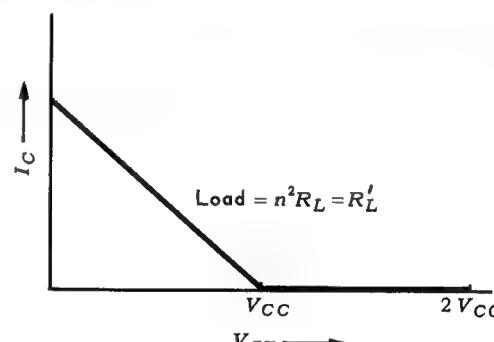
Fig. 7.35 Load line for a Class B amplifier,
cut-off for half a cycle.

Figure 7.35 shows the typical load-line for the individual transistors. The
load lines are combined in the composite characteristic of Fig. 7.36. Note from
Fig. 7.35 that current is zero when voltage is at its maximum, thus minimizing
dissipation. Each transistor effectively amplifies half the input wave. Figure
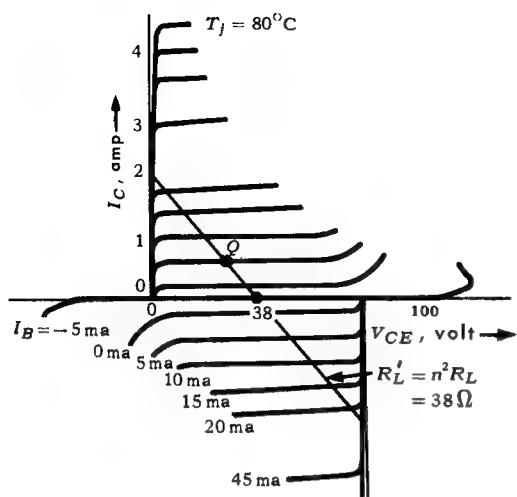
Fig. 7.36 Superimposed collector character-
istics for evaluation of push-pull operation.
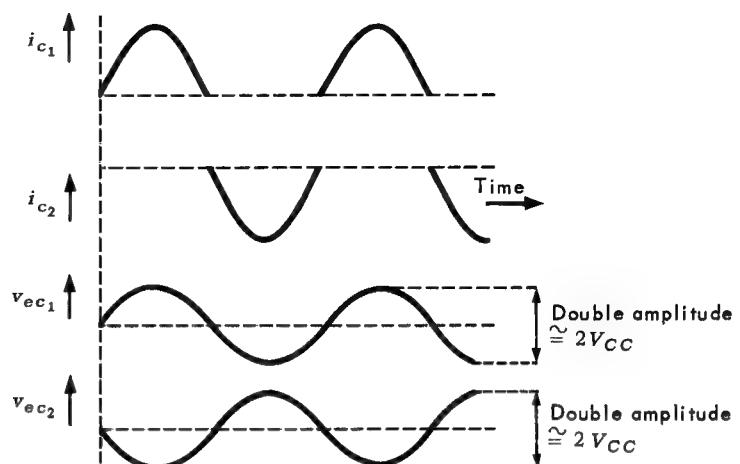
Fig. 7.37 Waveforms in a push-pull Class B amplifier.
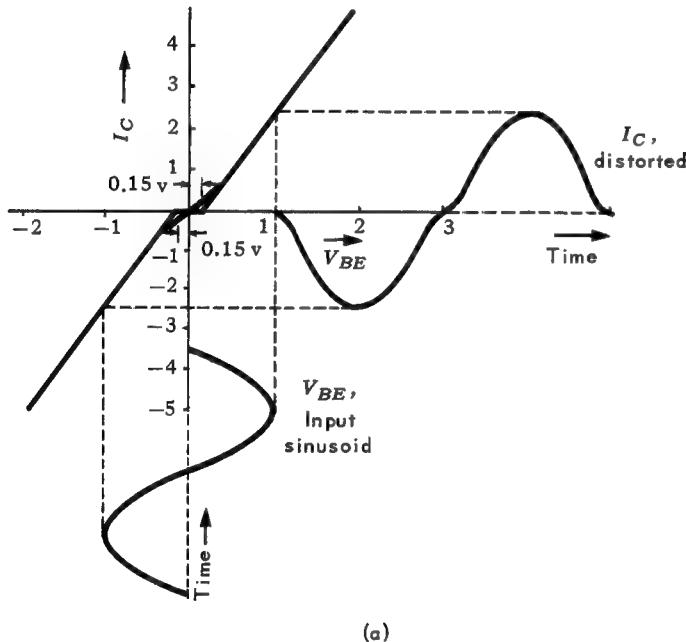

(a)
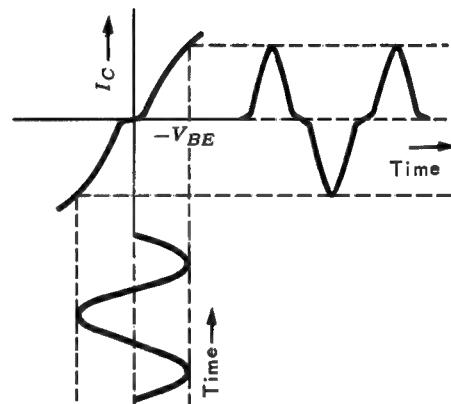
(b)

Fig. 7.38 (a) Superimposed 2N1537A transistor characteristics showing distortion in
push-pull output. This distortion is due to an equivalent offset in V_{BE}. (b) Typical
crossover distortion in a Class B push-pull amplifier.

7.37 shows current and voltage waveforms for the Class B connection. Since only
one transistor is conducting at a time, the load line corresponds to the resistance
$n^2 R_L$.

Figure 7.38 shows the composite I_C vs. V_{BE} characteristic. A sinusoidal in-
put wave leads to a distorted output current. This is called *cross-over distortion*.
To avoid cross-over distortion, it is advisable to operate slightly in Class AB
with an added bias, above the cut-off value. This provides for conduction during
slightly more than half of each cycle. The bias differential is about 0.15 v for
germanium and 0.6 v for silicon. Preferably, the bias is provided by a diode to
compensate for temperature. The improved composite characteristic is shown in
Fig. 7.39. The improvement in linearity is obvious.

(a)

(b)
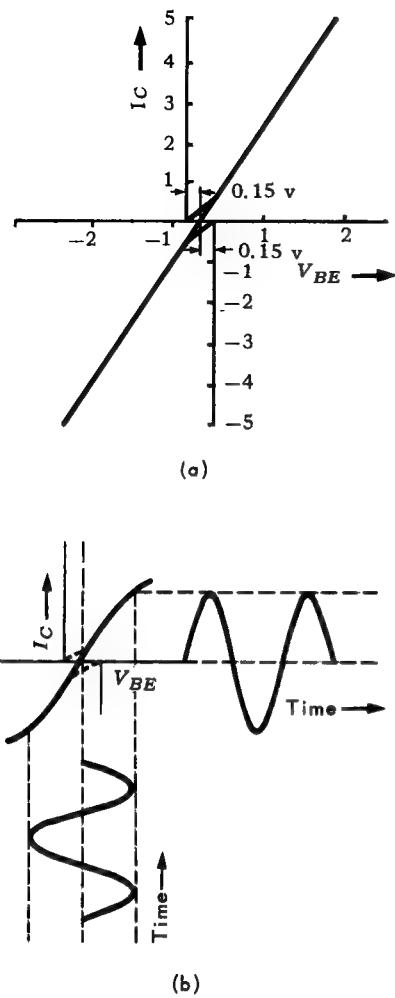
Fig. 7.39 (a) Superimposed 2N1537A transistor characteristics showing how crossover distortion is eliminated by modifying the bias of push-pull transistors. Compare with Fig. 7.38(a). (b) Class A-B push-pull amplifier biased to eliminate crossover distortion.

TABLE 7.2 Class B push-pull amplifier, design formulae.

Item	Formula $(R_T \neq 0)$	Formula $(R_T = 0)$	Equation
$P_{o_{max}}$	$\dfrac{V_{CC}^2 R_L'}{4(R_T + R_L')^2}$	$\dfrac{V_{CC}^2}{4 R_L'}$	(7.12a)
$P_{CE_{max}}$	$\dfrac{V_{CC}^2}{\pi^2 R_L'}$	$\dfrac{V_{CC}^2}{\pi^2 R_L'}$	(7.12b)
η_{max}	$\dfrac{\pi}{4}\dfrac{R_L'}{R_T + R_L'}$	0.785	(7.12c)
R_L'	$\dfrac{V_{CC}^2}{\pi^2 P_C}$	$\dfrac{V_{CC}^2}{\pi^2 P_C}$	(7.12d)
$\dfrac{P_{o_{max}}}{P_{CE_{max}}}$	$\dfrac{\pi^2}{4}\left(\dfrac{R_L'}{R_T + R_L'}\right)^2$	$\dfrac{\pi^2}{4} = 2.466$	(7.12e)
V_{CC}	$2V_{CC}^3 - BV_{max}V_{CC}^2 + \pi^2 P_C R_T V_{CC}$ $= BV_{max} P_C R_T \pi^2$	$V_{CC} = \dfrac{BV_{max}}{2}$	(7.12f)
$P_{CC_{max}}$	$\dfrac{V_{CC}^2}{\pi(R_T + R_L')}$	$\dfrac{V_{CC}^2}{\pi R_L'}$	(7.12g)
For $I_C = k I_{C_{max}}$, $k < 1$			
P_{CC}		$\dfrac{k V_{CC}^2}{\pi R_L'}$ (per transistor)	(7.12h)
η		$\dfrac{k \pi}{4}$	(7.12i)
P_o		$\dfrac{k^2 V_{CC}^2}{4 R_L'}$ (per transistor)	(7.12j)
I_{max}	$\dfrac{V_{CC}}{R_T + R_L'}$	$\dfrac{V_{CC}}{R_L'}$	(7.12k)

Design formulae for Class B operation are readily derived by reference to the circuit diagram of Fig. 7.40 and the idealized collector characteristics of Fig. 7.41. All significant symbols are shown on the figures. Although the derivations are not presented here, the design formulae are given in Table 7.2.

Comparing Class A and B operations for the same permissible transistor dissipation, power output is about five times greater for Class B operation than for Class A. The theoretical efficiency at maximum output is 78.5% for Class B as compared with 50% for Class A. Furthermore, d-c power for Class B approaches zero as the input signal is reduced, so that in normal use, the average d-c power
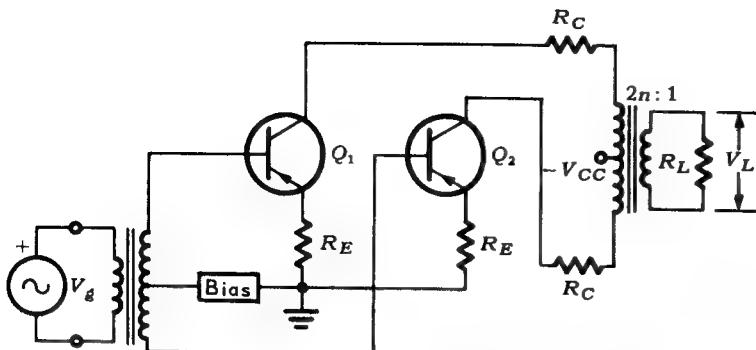
Fig. 7.40 Class B push-pull circuit rearranged for convenient calculations.

$$2V_{CC} - V_{CS} = BV_{max}$$

Fig. 7.41 Load line characteristics applicable to the push-pull Class B circuit.

is far less than the maximum. This is often a most important consideration. These reasons favor the use of Class B operation for most high power applications.

PROBLEM 7.14 For the Class B circuit of Fig. 7.42, determine V_{CC}, P_o, n, η, R'_L, R_1, and R_2. Use a maximum collector-emitter voltage, $BV_{max} = 45$ v. Thermal resistance $\theta_{ja} = 500°C/w$, and $T_j = 175°C$, max. Assume that the maximum ambient temperature is 70°C.

Fig. 7.42 Push-pull Class B transistor amplifier. (See Prob. 7.14.)

Solution: Estimate allowable collector dissipation P_C:

$$P_C = \theta_{ja}(175 - 70) = \frac{1}{500}(105) = 0.210 \text{ w.}$$

Saturation resistance $R_S = 50\ \Omega$ (see Prob. 7.9). No emitter resistor is used, since for Class B biasing, minimum power loss is more important than stability. Therefore,

$$R_T = R_C + R_S = 50 + 30 = 80\ \Omega.$$

To find V_{CC}, refer to Table 7.2:

$$2V_{CC}^3 - BV_{max}\ V_{CC}^2 + \pi^2\ P_C\ R_T\ V_{CC} = BV_{max}\ P_C\ R_T\ \pi^2. \qquad [7.12f]$$

Substituting numerical values and solving,

$$V_{CC} = 25.14 \text{ v.}$$

For our purposes, it is sufficiently accurate to let

$$V_{CC} = 25 \text{ v.}$$

Again, referring to Table 7.2,

$$R_L' = \frac{V_{CC}^2}{\pi^2 P_C} = 302 \ \Omega, \qquad\qquad [7.12d]$$

$$P_{o\,max} = \frac{V_{CC}^2 R_L'}{4(R_T + R_L')^2} = 0.323 \text{ w per transistor.} \qquad [7.12a]$$

For both transistors, $P_{o\,max} = 0.646$ w.

Continuing,

$$\eta_{max} = \frac{\pi}{4} \frac{R_L'}{R_T + R_L'} = 0.62 \text{ or } 62\%. \qquad\qquad [7.12c]$$

The transformer turns ratio is obtained from the relationship $R_L' = n^2 R_L$, so that $n = 0.376$.

To minimize cross-over distortion, particularly important at small-signal amplitudes, a bias of $V_{BE} = 0.25$ v at $T_j = 175\,°C$ is required (see Fig. 7.43). This curve is actually derived from the 125 °C curve, since the curve for 175 °C was not available. The required characteristic is derived from the 125 °C h_{FE} vs. I_C characteristic. (Approximations in our method are acceptable, since h_{FE} normally varies more among individual transistors than with temperature. Furthermore, refinements in adjustment are best made experimentally.) The sloping straight line approximation moves 2 mv/°C to the left for increasing T_j.

We may use a silicon diode for R_2 in Fig. 7.42. The diode should carry about ten times the sum of the base bias currents for the two transistors, or about 5 ma. Since $V_{CC} = 25$ v,

$$R_1 \cong \frac{V_{CC}}{5 \times 10^{-3}} = \frac{25}{5 \times 10^{-3}} = 5000 \ \Omega.$$

If we do not use the temperature compensating diode,

$$R_2 \cong \frac{0.25}{0.005} = 50 \ \Omega.$$

PROBLEM 7.15 In the circuit of the preceding problem, what is the input power for maximum output? What is the power gain?

Fig. 7.43 Approximate method to determine bias offset to eliminate crossover distortion.

TABLE 7.3 Measured parameters on a 2N930 transistor.

$I_{C\,(ma)}$	$T_j = 175°C$		$T_j = 25°C$	$T_j = 175°C$
	h_{FE}	$I_{B\,(\mu a)}$	V_{BE} (v)	V_{BE} (v)
1	460	2.2	0.515	0.215
2	490	4.1	0.54	0.24
5	500	10	0.56	0.26
10	490	20	0.58	0.28
20	425	47	0.61	0.31
30	380	79	0.635	0.335
40	335	120	0.655	0.355
50	310	161	0.67	0.370
60	290	206	0.68	0.38
70	250	240	0.695	0.395

Solution: Refer again to Table 7.2:

$$I_{C\,max} = \frac{V_{CC}}{R_T + R_L'} = \frac{25}{382} = 0.0655 \text{ a.} \qquad [7.12k]$$

From Fig. 7.43, this yields $V_{BE} = 0.395$ v, and from Table 7.3, $I_B = 240\ \mu$a. Neglecting distortion, we need $V_{BE} = 0.15$ v peak at $I_B = 240\ \mu$a peak, for a collector current of 65.5 ma. Thus,

$$P_1 = \frac{0.15 \times 240 \times 10^{-6}}{\sqrt{2} \times \sqrt{2}} \approx 18\ \mu\text{w,}$$

$$\text{Power gain} = \frac{0.646}{18 \times 10^{-6}} = 36{,}000.$$

7.7 Supplementary Problems

PROBLEM 7.16 Define the terms I_{CBO}, BV_{CEO}, and BV_{CES}.

PROBLEM 7.17 Explain the avalanche effect.

PROBLEM 7.18 What is the effect of temperature on h_{fe} and I_{co}?

PROBLEM 7.19 (a) Define thermal resistance. (b) Describe mathematically the effect of change in temperature on the power that is transferred to a body.

PROBLEM 7.20 Derive the optimum bias point of a common-emitter amplifier for maximum power output.

PROBLEM 7.21 What is the maximum efficiency of a class A amplifier?

PROBLEM 7.22 Design a power stage for maximum power output using the circuit of Fig. 7.5 and the transistor characteristics of Fig. 7.6. Ignore distortion and assume negligible leakage at the temperatures of interest. Maximum junction temperature is 150°C; maximum ambient temperature is 50°C. The total thermal resistance from junction to ambient is 2°C/w.

PROBLEM 7.23 Repeat Prob. 7.22 for the circuit of Fig. 7.7.

PROBLEM 7.24 Consider a 2N1532 transistor in the circuit of Fig. 7.19. Let $R_C = 0\ \Omega$, $R_E = 100\ \Omega$, $R_S = 2\ \Omega$, and $BV_{CEO} = 50$ v. The junction temperature is 90°C, the ambient temperature is 50°C, and the thermal resistance θ_{JC} is 0.6°C/w. Evaluate $I_{Q\,opt}$, V_{CC}, P_O, η, and R_L. Compare the results with those of Prob. 7.9. (Cf., App. A for the characteristics of a 2N1532 transistor.)

PROBLEM 7.25 Repeat Prob. 7.24 using the push-pull circuit of Fig. 2.42.

8
CHAPTER

FEEDBACK

8.1 Basic Concepts of Feedback

As was shown in Chap. 5, a transistor amplifier can be described by its equivalent circuit parameters. The parameters can then be used to calculate various properties of the amplifier, such as gain, and input and output impedances. For a given amplifier, the properties are fixed. In certain applications, however, we may have to alter such properties as gain, or input and output impedances, or frequency response. Obviously we can achieve this by redesigning the amplifier itself. However, there is a much more efficient method that can be used.

When a signal proportional to either the output voltage or current (or some combination thereof) of an amplifier is *fed back* to its input, we find that the amplifier thus formed has properties quite different from those of the original amplifier. This process of adding a portion of the output of an amplifier to its input in order to alter its performance is called *feedback*.

In its simplest form, the effects of feedback can be seen with the help of the block diagram of Fig. 8.1, in which block A denotes the amplifier, and block β, the feedback network. The relations for the system are

$$\left. \begin{array}{c} e = e_i + e_{fb}, \\ e_o = Ae, \\ e_{fb} = \beta e_o. \end{array} \right\} \tag{8.1}$$

The voltage e_{fb} is the signal which is fed back to the input.

The gain of the new amplifier, i.e., the feedback amplifier, is defined by

$$A_{fb} = \frac{e_o}{e_i}. \tag{8.2}$$

Solving (8.1) for e_o in terms of e_i,

$$e_o = \frac{A}{1 - \beta A} e_i. \tag{8.3}$$

The gain therefore becomes

$$A_{fb} = \frac{A}{1 - \beta A}. \tag{8.4}$$

The term βA is called the *feedback factor*. The amount of feedback, expressed in decibels, is usually given as

$$\text{db of feedback} = 20 \log \frac{1}{|1 - \beta A|} = -20 \log |1 - \beta A|, \tag{8.5}$$

where the logarithms are to the base 10.
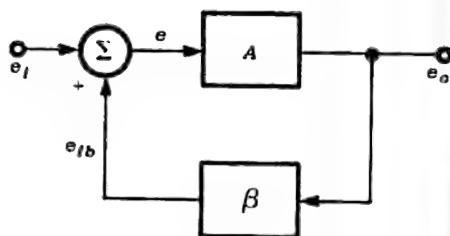
Fig. 8.1 Block diagram of a feed-back amplifier.

The feedback is termed *negative* or *degenerative* when it reduces the magnitude of the gain, i.e., when $|1 - \beta A| > 1$. When βA is real, it becomes $\beta A < 0$.

The feedback is called *positive* or *regenerative* when it increases the magnitude of the gain, i.e., when $|1 - \beta A| < 1$.

However, it is also seen that, when $\beta A = +1$, the *closed-loop gain* becomes infinite. (Closed-loop refers to the amplifier with the feedback in the circuit, and open-loop refers to the amplifier with the feedback removed.) This means, in a practical sense, that the feedback amplifier breaks into spontaneous oscillation. Thus an amplifier employing feedback must be closely examined for the presence of any instability.

It will be seen that negative feedback has the following properties:

1. It stabilizes the gain of the amplifier against component and bias supply variations.
2. It extends the frequency response.
3. It reduces the level of noise generated within the amplifier A.
4. It reduces the harmonic distortion in the output signal.

Suppose that some arbitrary parameter in the amplifier A changes, thereby causing a change in the gain. The fractional change in the gain can be expressed as dA/A. In turn, this will cause a change in the gain of the feedback amplifier which can be written as dA_{fb}/A_{fb}. Differentiating (8.4) with respect to A,

$$\frac{dA_{fb}}{dA} = \frac{1}{(1 - \beta A)^2} = \frac{A}{1 - \beta A}\left(\frac{1}{1 - \beta A}\right)\frac{1}{A}.$$

Thus the fractional changes are related by

$$\frac{dA_{fb}}{A_{fb}} = \frac{1}{1 - \beta A}\frac{dA}{A}. \tag{8.6}$$

It is therefore seen that negative feedback reduces the effects of the parameter variation; i.e., negative feedback stabilizes the gain, while positive feedback has the opposite effect. In addition, it will be seen that feedback can also be used to alter impedance levels and shape frequency response.

PROBLEM 8.1 Show that negative feedback extends the frequency response of the amplifier A when the gain is

$$A(j\omega) = \frac{A_0}{1 + \dfrac{j\omega}{\omega_0}}, \tag{8.7}$$

where A_0 is the middle frequency gain, and ω_0 is the high-frequency cut-off point.

Solution: This can be shown by substituting (8.7) into (8.4) and observing the frequency response of the feedback amplifier:

$$A_{fb}(j\omega) = \frac{\dfrac{A_0}{1 + \dfrac{j\omega}{\omega_0}}}{1 - \beta\dfrac{A_0}{1 + \dfrac{j\omega}{\omega_0}}}$$

$$= \frac{A_0}{1 - \beta A_0 + \dfrac{j\omega}{\omega_0}}$$

$$= \frac{A_0}{1 - \beta A_0}\frac{1}{1 + j\dfrac{\omega}{(1 - \beta A_0)\omega_0}}. \tag{8.8}$$

Define

$$A_{fb_0} = \frac{A_0}{1 - \beta A_0},$$

$$\omega_{fb_0} = (1 - \beta A_0)\omega_0 .$$

$$\tag{8.9}$$

Then,

$$A_{fb}(j\omega) = \frac{A_{fb_0}}{1 + \dfrac{j\omega}{\omega_{fb_0}}} . \tag{8.10}$$

For negative feedback, i.e., $\beta A_0 < 0$, we see that $\omega_{fb_0} > \omega_0$; thus the high-frequency cut-off is higher for the feedback amplifier than for the open-loop amplifier. Figure 8.2 shows the comparison of the frequency responses with and without negative feedback on logarithmic coordinates.

The fact that the two curves merge for very high frequencies can be seen by assuming that ω is very large in (8.7) and (8.10). Then,

$$A_{fb}(j\omega) \cong \frac{A_{fb_0}}{\dfrac{j\omega}{\omega_{fb_0}}} = \frac{A_0}{\dfrac{j\omega}{\omega_0}},$$

$$A(j\omega) \cong \frac{A_0}{\dfrac{j\omega}{\omega_0}} .$$

Fig. 8.2 Frequency response of an amplifier with and without feedback.

Thus the two expressions become identical at very high frequencies.

A similar analysis can be performed to show that negative feedback decreases the low-frequency cut-off point.

Now consider the effect of feedback on a disturbance (e.g., noise) generated within the amplifier A. Examine the block diagram of Fig. 8.3. This amplifier is similar to Fig. 8.1 except that the amplifier A is broken into two parts with gains A_1 and A_2, such that $A = A_1 A_2$. The voltage e_d represents a disturbance that can be thought of as occurring within the amplifier A in Fig. 8.1.
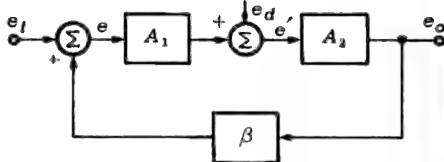
Fig. 8.3 The effect of a disturbance, such as noise, on a feedback amplifier.

PROBLEM 8.2   Find e_o in terms of e_i and e_d for both the open-loop and closed-loop cases.

Solution: First consider the open-loop case which is equivalent to setting $\beta = 0$. We see immediately that

$$e_o = A_1 A_2 e_i + A_2 e_d . \tag{8.11}$$

For the closed-loop case,

$$e_i = e + \beta e_o,$$

$$e_d = -A_1 e + e',$$

$$e_o = A_2 e' .$$

$$\tag{8.12}$$

Solving these equations for e_o in terms of e_i and e_d,

$$e_o = \frac{A_1 A_2}{1 - \beta A_1 A_2} e_i + \frac{A_2}{1 - \beta A_1 A_2} e_d . \tag{8.13}$$

Now define e_{oe} as that part of the output caused by e_i, and e_{od} as that part of e_o due to the disturbance e_d. Then for the open-loop case,

$$e_{os} = A_1 A_2 e_i,$$
$$e_{od} = A_2 e_d. \tag{8.14}$$

And for the closed-loop case,

$$e'_{os} = \frac{A_1 A_2}{1 - \beta A_1 A_2} e_i,$$
$$e'_{od} = \frac{A_2}{1 - \beta A_1 A_2} e_d, \tag{8.15}$$

where the primes have been used to distinguish between the two cases.

A signal to noise ratio can be defined as the magnitude of the ratio of the output signal to the output disturbance. (Noise is defined as any unwanted or undesirable signal.) Thus for the open-loop case,

$$\rho = \left| \frac{e_{os}}{e_{od}} \right| = \frac{|A_1 A_2 e_i|}{|A_2 e_d|} = \frac{|A_1 e_i|}{|e_d|}. \tag{8.16}$$

And for the closed-loop case,

$$\rho' = \left| \frac{e'_{os}}{e'_{od}} \right| = \frac{|A_1 e_i|}{|e_d|}. \tag{8.17}$$

Note that the two ratios are the same, and outwardly at least no advantage is gained by employing feedback.

However, looking at (8.14) and (8.15),

$$\left| \frac{e'_{os}}{e_{os}} \right| = \frac{1}{|1 - \beta A_1 A_2|},$$

and for negative feedback, this ratio is less than unity.

Now suppose that the input to the feedback amplifier is altered by a factor $1 - \beta A_1 A_2$; i.e., the new input is

$$e'_i = (1 - \beta A_1 A_2) e_i.$$

Then the signal output of the feedback amplifier becomes

$$e'_{os} = \frac{A_1 A_2}{1 - \beta A_1 A_2} e'_i = A_1 A_2 e_i. \tag{8.18}$$

In other words, the output signal level is raised until it is the same as for the open-loop case. Then the signal to noise ratio for the closed-loop amplifier becomes

$$\rho' = \left| \frac{e'_{os}}{e'_{od}} \right| = |1 - \beta A_1 A_2| \frac{|A_1 e_i|}{|e_d|} = |1 - \beta A_1 A_2| \rho. \tag{8.19}$$

Thus, when negative feedback is employed, the signal to noise ratio is increased by a factor $|1 - \beta A_1 A_2| > 1$ when the input signal levels are arranged so that the output signal levels are the same for the open- and closed-loop cases. Moreover, the disturbance e_d can be thought of as representing the nonlinearity in the amplifier A; i.e., e_d may represent the origin of the second and higher harmonics that appear in the output signal. Then it can be seen that, when negative feedback is employed, harmonic distortion can be effectively reduced by a factor $|1 - \beta A_1 A_2|$.

8.2 Types of Feedback

The principal types of negative feedback are *voltage* and *current feedback.* Voltage feedback means that part of the amplifier *output signal voltage* is fed back to the input. Similarly, current feedback means that voltage proportional to *output signal current* is fed back to the input.

Negative voltage feedback tends to make output voltage independent of load; i.e., it reduces output impedance. Current feedback tends to make output current independent of load by increasing output impedance. The higher the gain through the amplifier and around the feedback loop, the closer the output characteristics approach the idealized zero and infinite impedance conditions for voltage and current feedback, respectively.

In many instances, voltage and current feedback occur simultaneously, and a clear-cut distinction may not be possible. However, this consideration does not influence the accuracy of our calculations.

PROBLEM 8.3   Referring to Fig. 8.4a, state what type of feedback is used. Calculate input and output impedances, and voltage gain.
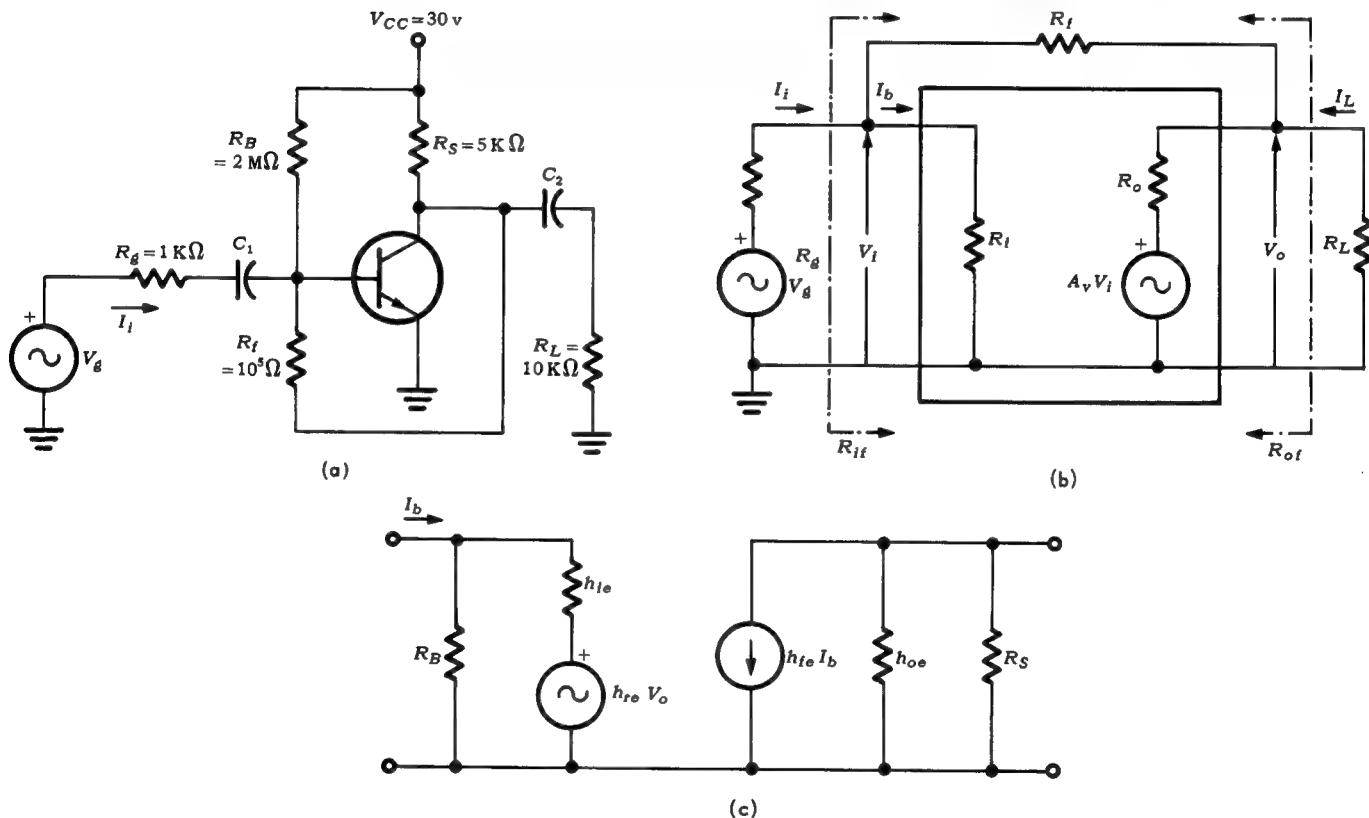
Fig. 8.4 (a) Feedback amplifier. (b) Equivalent circuit of (a). (c) Transistor equivalent circuit.

Solution: The derived feedback is proportional to the output voltage. This is *voltage feedback.* The feedback voltage acts to inject current into the transistor base circuit, in *parallel with* and subtracting from the applied current, I_i. Figure 8.4b shows a simple equivalent circuit, in terms of input and output impedances, of the common-emitter transistor stage. The hybrid circuit for the transistor itself, including the bias resistors, R_B and R_S, is illustrated in Fig. 8.4c.

To calculate voltage gain from Fig. 8.4b, it is necessary to determine A_v, the voltage gain in the absence of feedback. An effective load resistance R_L'

must include the separate parallel paths of R_L and R_f. Resistance R_L' must be known in order to calculate the open-loop gain A_v. Fortunately, R_f is so high that we usually ignore the contributions of R_i in determining R_L'.

Now calculate A_{vL}, the voltage gain with R_L connected:

$$A_{vL} = \frac{V_o}{V_i} = \frac{-R_L' h_{fe}}{h_{ie}\left[1 + R_L'\left(h_{oe} - \dfrac{h_{fe} h_{re}}{h_{ie}}\right)\right]} . \qquad [5.8]$$

Calculating R_L' as described above,

$$R_L' = \frac{R_L R_S}{R_L + R_S} \parallel R_f ,$$

or, substituting numerical values, $R_L' = 3220\,\Omega$. Substituting in (5.8), the expression for voltage gain in the absence of feedback is $A_{vL} = -420$.

Define a voltage feedback factor, β_1, such that

$$\beta_1 = \frac{R_i'}{R_i' + R_f}, \qquad (8.20)$$

where R_i' is the parallel impedance of R_i and R_B, the bias resistor.

From (5.6),

$$R_i = h_{ie} - \frac{h_{fe} h_{re}}{h_{oe} + \dfrac{1}{R_L'}} .$$

Substituting numerical values in (5.6), $R_i = 2030\,\Omega$. This is essentially equal to R_i', since the contribution of R_B is negligible. Therefore,

$$\beta_1 = \frac{2030}{100,000 + 2030}$$

$$= 0.0199.$$

We may use this feedback factor to develop a convenient formula for input impedance including the effects of feedback, R_{if}:

$$R_{if} = \frac{V_i}{I_i},$$

$$I_i = I_b - I_f,$$

$$I_b = \frac{V_o}{A_{vL} R_i'},$$

$$I_f = \frac{V_o}{R_i' + R_f} .$$

These equations may be combined to yield an expression for R_{if}:

$$R_{if} = \frac{V_i}{I_i} = \frac{I_b R_i'}{I_b - \dfrac{V_o}{R_i' + R_f}}, \qquad (8.21a)$$

or

$$R_{if} = \frac{I_b R_i'}{I_b - \dfrac{I_b A_{vL} R_i'}{R_i' + R_f}} . \qquad (8.21b)$$

Cancelling I_b and substituting the expression for β_1 in (8.21b),

$$R_{if} = \frac{R_i'}{1 - A_{vL}\beta_1} \, . \tag{8.22}$$

Recalling that A_{vL} is negative, note that parallel feedback *decreases* the input impedance of an amplifier by a factor of $1 - A_{vL}\beta_1$, or, more generally, $1 - A_v\beta$, where A_v is voltage gain, and β is the fraction of fed-back voltage. Substituting numerical values, $1 - A_{vL}\beta_1 = 9.35$, and $R_{if} = 2030/9.35 = 217\,\Omega$, a very large reduction due to feedback.

Consider the effect of feedback on *voltage gain*:

$$\frac{V_o}{V_g} = A_{vL}\frac{R_{if}}{R_{if} + R_g} \, . \tag{8.23}$$

Substituting numerical values,

$$\frac{V_o}{V_g} = -420\,\frac{217}{1217} = -75.$$

Without feedback, $R_i' = 2030\,\Omega$ is used instead of R_{if} in the equation for gain. Numerically,

$$\frac{V_o}{V_g} = A_{vL}\frac{R_i'}{R_i' + R_g} = -420\,\frac{2030}{3030} = -282.$$

Feedback has led to a substantial loss in gain. However, gain variation and noise have been reduced by the same factor, achieving important advantages, as previously explained.

The output impedance remains to be calculated. To do this, "cut" the output circuit as shown in Fig. 8.4b, and determine the impedance seen looking back into the amplifier from R_L.

Define a voltage gain, A_{vo}, analogous to A_{vL}, but with R_L removed. A new parameter, R_i'', is the apparent input impedance seen looking back toward the input through R_f:

$$R_i'' = \frac{R_i' R_g}{R_i' + R_g} \, .$$

Therefore,

$$V_i = \frac{V_o R_i''}{R_i'' + R_f} = V_o\beta_2 .$$

The basic transistor output impedance in the absence of feedback, R_o (Fig. 8.4c), is determined as

$$R_o = \frac{1}{h_{oe} - \dfrac{h_{fe}h_{re}}{h_{ie} + R_g}} \, . \tag{5.9}$$

Referring again to Fig. 8.4b, R_o is paralleled by R_S and $R_f + R_i'' \cong R_f$ to give an effective output impedance, R_o', still omitting the effect of feedback. Similarly, we may determine the open-circuit voltage gain, A_{vo}, with R_L removed. Gain A_{vo} is computed using the previously developed gain formula with a load resistance

$$R_L'' = \frac{R_f R_S}{R_f + R_S} \, ,$$

the resistance paralleled with R_o in calculating R_o'. The following formulae are applicable:

$$A_{vo} = \frac{V_o}{V_i} = \frac{-h_{fe}R_L''}{h_{ie}\left[1 + R_L\left(h_{oe} - \dfrac{h_{fe}h_{re}}{h_{ie}}\right)\right]} \quad, \qquad [5.8]$$

$$R_o = \frac{1}{h_{oe} - \dfrac{h_{fe}h_{re}}{h_{ie} + R_g}} \quad . \qquad [5.9]$$

Now include the effect of feedback to calculate R_{of}, the output impedance in the presence of feedback. The feedback voltage, with V_o applied to the output and V_g shorted, is

$$V_i = V_o \frac{R_i''}{R_i'' + R_f} \quad, \qquad (8.24)$$

where R_i'' is the parallel impedance of R_i'' and R_g. The ratio, $R_i''/(R_i'' + R_f)$, is another feedback factor, β_2, specifying the proportion of output signal fed back to the input. This fed-back voltage is, of course, amplified and applied to the output as $V_o\beta_2 A_{vo}$. Output impedance, R_{of}, is easily calculated from output current, I_L:

$$I_L = \frac{V_o - V_o\beta_2 A_{vo}}{R_o'} \quad .$$

Solving for $R_{of} = V_o/I_L$,

$$R_{of} = \frac{R_o'}{1 - A_{vo}\beta_2} \quad . \qquad (8.25)$$

This formula shows how output impedance is reduced by the factor, $1 - A_{vo}\beta_2$, due to voltage feedback.

Substituting numerical values in the above formulae,

$$R_L'' = 4750 \ \Omega,$$

$$R_i'' = 705 \ \Omega,$$

$$A_{vo} = -618,$$

$$R_o = 84 \ \text{K}\Omega \ \text{(transistor alone)},$$

$$R_o' = 4500 \ \Omega,$$

$$1 - A_{vo}\beta_2 = 1.425,$$

$$R_{of} = 3160 \ \Omega.$$

Note that the decrease in input impedance is *not the same* as the decrease in output impedance.

PROBLEM 8.4 Repeat Prob. 8.3, using the circuit of Fig. 8.5a.

Solution: Figure 8.5a shows a common-emitter feedback amplifier. Feedback is taken across a resistor in series with the load. The fed-back voltage is proportional to load *current*; this is *current feedback*. Figure 8.5b shows the equivalent circuit of this feedback amplifier. The fed-back voltage is summed at the input *in series* with the applied input signal. The amplifier equivalent circuit without a load termination, but including bias resistors, is the same as given in Fig. 8.4c.

Now start by calculating voltage gain, and then the input impedance. Use roughly the same procedures as in Prob. 8.3. However, we can use simplifying approximations more freely. Highly accurate calculations are rarely justified.
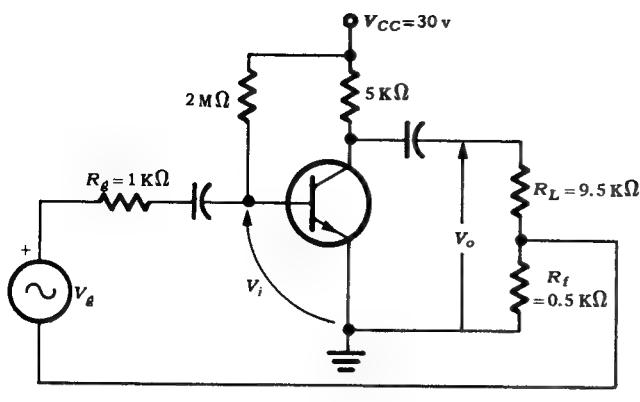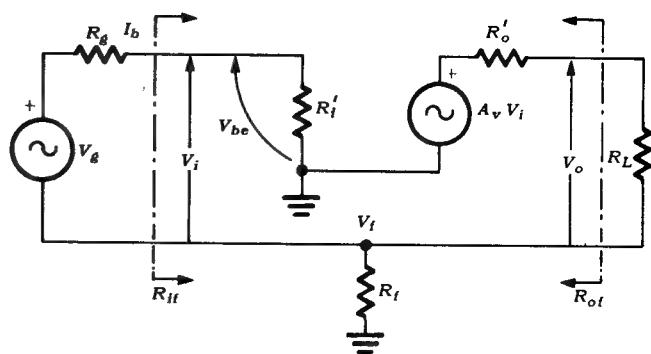
Fig. 8.5 (a) Amplifier with feedback voltage proportional to load current. (b) Equivalent circuit of (a).

If we neglect a small amount of *forward feed* from input to output through R_f, and ignore the loading effect of the 100 KΩ feedback resistor R_f, then the gain, $A_{vL} = -420$, is the same as in Prob. 8.3. The feedback factor is easy to calculate:

$$\beta_1 = \frac{R_f}{R_L + R_f} = \frac{1}{20}.$$

Again, by referring to Prob. 8.3,

$$R_i' = 2030 \ \Omega.$$

We must now calculate $R_{if} = V_i/I_i$. From Fig. 8.5b,

$$V_i = V_{be} - V_f,$$

$$V_f = A_{vL} V_{be} \beta_1,$$

$$I_i = \frac{V_{be}}{R_i'}.$$

Combining and solving,

$$V_f = V_{be} - A_{vL} V_{be} \beta_1 = V_{be} (1 - A_{vL} \beta_1),$$

$$R_{if} = \frac{V_i}{I_i} = \frac{V_{be}(1 - A_{vL} \beta_1)}{\dfrac{V_{be}}{R_i'}} = (1 - A_{vL} \beta_1) R_i'. \tag{8.26}$$

The series feedback at the input increases the input impedance by a factor of $(1 - A_{vL} \beta_1)$.

Substituting numerical values,

$$A_{vL} \beta_1 = (-420)(1/20) = -21,$$

$$R_{if} = 2030 (1 + 21) = 44.7 \ \text{K} \Omega.$$

Now determine the closed-loop voltage gain:

$$\frac{V_o}{V_g} = \frac{V_{be} A_{vL}}{V_g} = \frac{V_i A_{vL}}{(1 - A_{vL} \beta_1) V_g}.$$

But

$$V_i = V_g \frac{R_{if}}{R_{if} + R_g},$$

so that

$$\frac{V_o}{V_g} = \frac{A_{vL}}{(1 - A_{vL}\,\beta_1)} \times \frac{R_{if}}{R_{if} + R_g} \ . \tag{8.27a}$$

For substantial feedback, where $A_{vL}\,\beta_1 \gg 1$, and $R_{if} \gg R_g$,

$$\frac{V_o}{V_g} \cong -\frac{1}{\beta_1} \times \frac{R_{if}}{R_{if} + R_g} \cong -\frac{1}{\beta_1} \ . \tag{8.27b}$$

Thus the closed-loop voltage gain becomes, to a large extent, only a function of the feedback factor β_1. Substituting numerical values, solve for A_{vf}, the voltage gain in the presence of feedback:

$$A_{vf} = \frac{V_o}{V_g} = \frac{\dfrac{44{,}700}{45{,}700}\,(-420)}{.1 - (-21)}$$

$$= -19.1 .$$

The approximate value, $A_{vf} = -1/\beta_1 = -20$, checks very well. Without feedback, the gain is

$$\frac{R_i'}{R_i' + R_g} \ A_{vL} = \frac{2030}{3030}\,(-420) = -282 .$$

The reduction in gain is accompanied by greatly improved stability. Very large percentage changes in the transistor characteristics are accompanied by very much smaller percentage changes in amplifier gain with feedback. Where very high gain is required, it is much better to *cascade* stages, while employing generous amounts of feedback.

Now we calculate the output impedance. Proceeding as before, we open the output circuit by disconnecting R_L, and substituting an *externally applied* voltage, V_o. Source voltage V_g is short-circuited. For this condition, the voltage gain, as before, is $A_{vo} = -618$ (neglecting the small influence of R_f). Hence,

$$V_f = R_f I_L = \frac{R_f}{R_f + R_L} \ V_o = \beta_2\,V_o \ ,$$

$$R_{of} = \frac{V_o}{I_L} = \frac{-R_f A_{vo} I_L + R_o' I_L + R_f I_L}{I_L} ,$$

$$R_{of} = R_o' + R_f(1 - A_{vo}). \tag{8.28}$$

Current feedback has increased the output impedance by $R_f(1 - A_{vo})$. Substituting numerical values,

$$R_{of} = 4500 + (500)(421) = 25{,}500 \ \Omega .$$

The preceding material points out the important benefits that are derived by the use of feedback. Amplifiers with gain stabilities to one part in 10,000 are not uncommon. Feedback allows the use of wide-tolerance transistors in precision devices.

However, feedback cannot be applied indiscriminately. Note that from (8.4),

$$A_{fb} = \frac{A}{1 - A\beta} \ .$$

This shows the characteristic way in which gain is affected by feedback. When $A\beta = 1$, A_{fb} becomes infinite. This means that the amplifier develops an output with no applied input. If $A\beta$ is a function of frequency (as it almost always is),

then even a theoretically correct low-frequency feedback factor can become unity at some high frequency, in which case, self-sustained oscillations occur at that frequency. This, of course, is the basis of operation of oscillators. But in high-gain amplifiers where it is desired to incorporate feedback, the possibility of oscillations is very real, and it is important to carry out a design with this realization in mind.

8.3 Stability

Let us consider the subject of stability in greater detail. Refer to the *open-loop* circuit of Fig. 8.6. It is apparent that if the voltage gain around the loop is such that e_{fb} is equal to e, with a 180° phase shift, then self-sustained oscillations will occur on closing the loop. This may be deduced from the basic gain equation

$$\text{Gain} = \frac{A}{1 - A\beta}, \qquad [8.4]$$

where gain becomes infinite when $A\beta = 1$, so that an output (the sustained oscillation) occurs in the absence of any input. The frequency of oscillation is that frequency where open-loop phase shift is 180°. An oscillator differs from a feedback amplifier only in that the feedback characteristics are chosen to assure a stable oscillation at a desired frequency, rather than a stable gain.

It is important to note that oscillations also occur when e_{fb} *exceeds* e, with the required 180° phase shift. In this instance, oscillations build up in amplitude, until they are limited by amplifier saturation. For the steady saturated condition, loop gain is reduced to unity, since obviously the open-loop output is identical with the amplifier input.

Nyquist devised a fundamental method for analyzing the conditions for instability. The method consists of plotting *complex* open-loop gain on polar coordinates as a function of frequency varying from zero to infinity. The point whose polar coordinates are (1, 180°) is called the *Nyquist point*. If the gain vs. frequency curve passes through this point, then the conditions for oscillation described above, unity gain, and 180° phase shift exist, and self-sustained oscillations occur. Somewhat more generally, if the open-loop gain characteristic *encircles** the Nyquist point, the closed-loop will oscillate. As the loop saturates, the Nyquist characteristic contracts until it lies on the minus one point, as in Fig. 8.7. The frequency of oscillation corresponds to the frequency ω_1 on the gain characteristic at the Nyquist point.

$e = e_I - e_{fb}$, in the closed-loop circuit

Fig. 8.6 Open-loop configuration of feedback amplifier circuit.
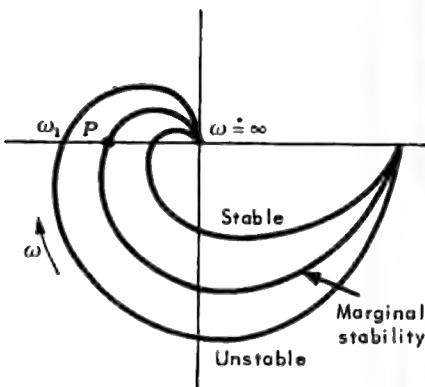
P = Nyquist point at unit distance from origin and 180°.

Fig. 8.7 Polar coordinate Nyquist plot of open-loop gain. Increased gain leads to oscillation at frequency ω_1. If gain is set to the unstable value, resulting oscillation leads to a gain loss so that the curve passes through P.

PROBLEM 8.5 Refer to Fig. 8.8 which shows several Nyquist complex gain plots, and indicate what plots correspond to stable closed-loop conditions.

Solution: The required solution is noted directly on the figure.

Normally, in the mid-frequency range of amplifier operation, gain is relatively uniform with frequency, with phase shift approximately zero. It is only in the low- and high-frequency regions of operation that large phase-shifts occur. Thus, in the design of feedback amplifiers, much attention must be given the low- and high-frequency gain and phase-shift characteristics to avoid instability, even though normal operation may be required only in the mid-frequency region.

There is a practical point to be observed in relating open-loop and closed-loop characteristics. When breaking the loop, care is necessary to ensure that terminating impedances are unchanged. The load on the open feedback circuit

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* The intuitive concept of *encirclement* becomes somewhat ambiguous for complex circuits, and thus Nyquist's *stability criterion* must be extended. However the topic, amply covered elsewhere, is outside the scope of this book.

must correspond to the effective impedance seen by the feedback circuit when the loop is closed. Similarly, the effective impedance in the amplifier input circuit must be unchanged for the open-loop analysis.

PROBLEM 8.6 Consider the simple multi-stage amplifier of Fig. 8.9 which shows the individual amplifier stage and the three cascaded stages, with identical interstage coupling networks. The fraction of output voltage fed back to the input is designated as β. For simplicity, it is assumed that β does not affect either the load seen by the amplifier output, or the driving impedance seen by the input. For $\beta = 1/100$, determine whether the amplifier is stable. Use Nyquist's criterion, with suitable approximations to simplify calculations.

Solution: The key to a reasonable and simple solution is to analyze circuit behavior separately at low and high frequencies. The wide separation between low- and high-frequency regions makes this procedure possible.

Gain falls off at the extreme frequencies. At very low frequency, gain is attenuated by the series capacitor, C_1; at very high frequency, R_o in combination with the shunting capacitor, C_2, serves to attenuate the gain.

Consider the interstage network at low frequency, where $C_2 \ll C_1$ may be neglected in comparison with R_i, and the reactance of C_1. The interstage network, at low frequency, therefore introduces an attenuation (for three stages) of

$$K_l = \left(\frac{R_i}{R_i + \dfrac{1}{j\omega C_1}} \right)^3 = \left(\frac{j\omega R_i C_1}{1 + j\omega R_i C_1} \right)^3. \qquad (8.29)$$

Substituting numerical values,

$$K_l = \left(\frac{j\omega}{1 + j\omega} \right)^3.$$

Similarly, the attenuation at high frequency may be approximated. The network components of importance in this region are R_o and C_2. In the high-frequency region, C_1 is essentially a short-circuit, while R_i is much higher than the reactance of C_2. Therefore,

$$K_h = \left(\frac{\dfrac{1}{j\omega C_2}}{R_o + \dfrac{1}{j\omega C_2}} \right)^3 = \left(\frac{1}{1 + j\omega C_2 R_o} \right)^3. \qquad (8.30)$$

Fig. 8.8 Typical Nyquist frequency plots on polar coordinates.

$R_i = 100 \, \text{K}\Omega, \qquad R_o = 100 \, \Omega$

(a)

$C_1 = 10 \, \mu\text{f}, \qquad C_2 = 0.1 \, \mu\text{f}$

(b)
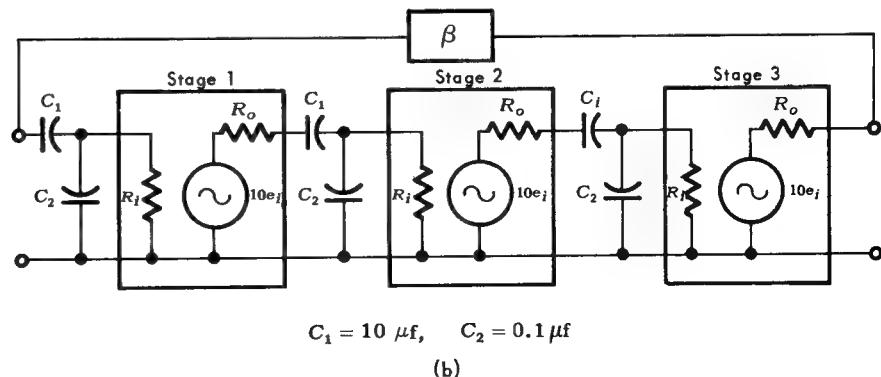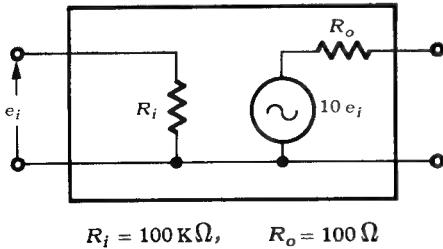
Fig. 8.9 (a) Simple multi-stage amplifier, and (b) its three cascade stages with identical interstage coupling networks.

Substituting numerical values for $R_o C_2$,

$$K_h = \left(\frac{1}{1 + j\omega\, 10^{-5}}\right)^3 .$$

Compare (8.29) with (8.30). For (8.29), as frequency increases to the relatively flat mid-frequency region, $K_l \doteq 1$. Similarly, for (8.30), as frequency *decreases* to the mid-frequency region, $K_h \doteq 1$. These limiting high- and low-frequency conditions must, of course, lead to the same mid-frequency gain if our approximations are valid.

Open-loop gain, used in plotting the Nyquist characteristic, corresponds to the attenuations calculated by (8.29) and (8.30), multiplied by the feedback factor β, and the gains of the amplifier stages, $(10)^3$. Figure 8.10 shows the Nyquist characteristic plotted over the entire frequency range. Note that the Nyquist point is encircled not once, but twice, in both the low- and high-frequency regions. The loop is clearly unstable.

Note particularly that (for this special case), the high- and low-frequency regions of the curve exhibit the same gain at 180° phase shift. Reducing the gain by 80% (by reducing β from 1/100 to 1/125) leads to a marginally stable system. Of course, this marginal stability is not practical; at least 6 db of *gain margin* are normally recommended for the 180° phase-shift point.
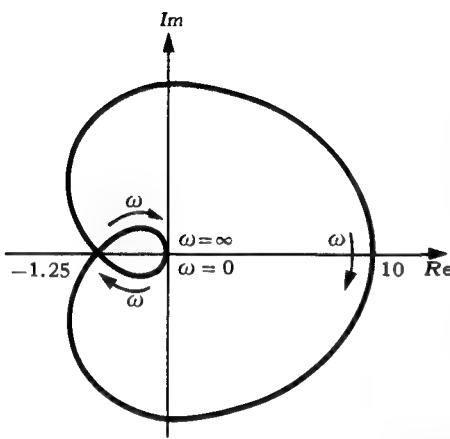
Fig. 8.10 Nyquist plot of transfer function of Prob. 8.2. Note that gain is 1.25 at 180° phase for high- and low-frequency regions.

The simple example illustrated above shows how neatly the Nyquist characteristic describes the amplifier frequency characteristic in the presence of substantial amounts of feedback. The amplifier designer must *shape* the Nyquist curve to avoid the −1 point by an adequate margin, while maintaining the desired degree of feedback required for gain stabilization in the mid-frequency range. Without the visualization provided by the Nyquist plot, stability analysis is relatively tedious.

PROBLEM 8.7   For the feedback amplifier of the preceding problem, determine the frequency and gain at which phase-shift equals 180° at both ends of the frequency band.

Solution: The loop gains for $\beta = 1/100$ are given by the following equations:

$$K_l \text{ (loop gain)} = 10\left(\frac{j\omega}{1 + j\omega}\right)^3, \tag{8.29}$$

$$K_h \text{ (loop gain)} = 10\left(\frac{1}{1 + j\omega\, 10^{-5}}\right)^3 \tag{8.30}$$

The frequency of K_l has a 180° phase shift when

$$270° - 3 \arctan \omega_l = 180°, \quad \text{or} \quad \arctan \omega_l = 30°;$$

that is, when $\omega_l = 0.577$.

Gain at this point may be calculated by substituting $\omega_l = 0.577$ in (8.29):

$$|K_l| = 10\,\frac{0.577^3}{[1 + 0.577^2]^{3/2}} = 1.25 .$$

Similarly, K_h has a 180° phase shift when

$$3 \arctan 10^{-5}\,\omega_h = 180°, \quad \text{or} \quad \tan 60° = 10^{-5}\,\omega_h = \sqrt{3}.$$

Solving,

$$\omega_h = \sqrt{3} \times 10^5 .$$

To calculate gain, substitute $\omega_h = \sqrt{3} \times 10^5$ in (8.30):

$$|K_h| = 10 \frac{1}{[1 + 3]^{3/2}} = \frac{10}{8} = 1.25 .$$

The results calculated above check with those shown on the Nyquist curve of Fig. 8.10. In all but the simplest cases, calculations of the type performed in this problem prove tedious and impractical. Nor do they provide the visual picture of circuit behavior afforded by curves such as the plot of Fig. 8.10. Nevertheless, even the Nyquist characteristic is difficult to use. The polar coordinate plots are tedious to make. The effects of circuit changes to improve specific aspects of performance require equally tedious evaluation. The Nyquist approach is not a convenient tool for *synthesis*.

8.4 The Bode Diagram

The Bode method of plotting frequency response is based on the use of logarithmic coordinates for gain (or attenuation) and frequency. This type of coordinate system leads to easily derived asymptotes which provide a surprisingly accurate representation of the gain function. Appendix C describes how to plot Bode diagrams.

PROBLEM 8.8   Solve Prob. 8.6 using the Bode plotting methods of Appendix C.

Solution: The asymptotic solution is shown in Fig. 8.11. The phase shift needs but to be sketched in, taking accurate points only in the vicinity of 180° phase shift. A convenient stability check, well-suited to the asymptotic method of plotting gain, is to calculate phase shift at those frequencies where asymptotic gain falls to zero db, as shown in Fig. 8.11. If phase shift exceeds 180°, instability occurs. As shown on Fig. 8.11, phase shift does indeed exceed 180° when gain has fallen to unity.
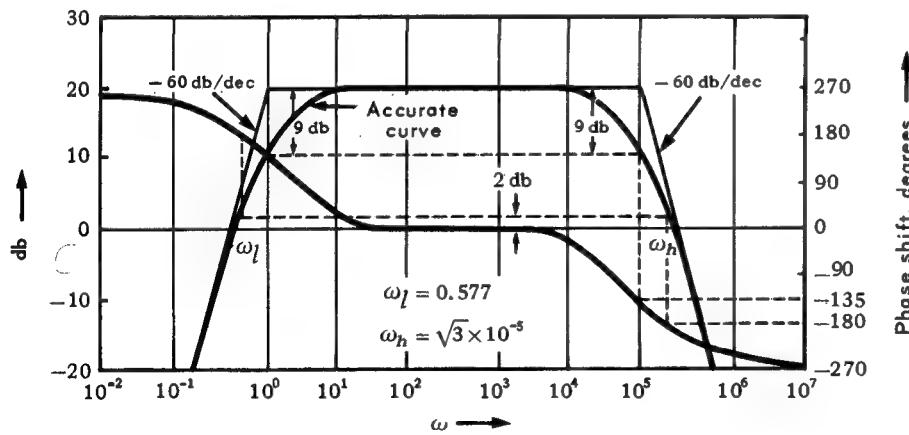
Fig. 8.11   Bode plot of open-loop gain of amplifier circuit of Fig. 8.9.

PROBLEM 8.9   For the feedback amplifier of Prob. 8.8, determine the feedback factor β for the condition of marginal stability. Also find β for a 135° phase shift at the asymptotic zero db point (45° *phase margin*).

Solution: From Fig. 8.11, $\beta = 1/125$ and $1/355$ for 0° phase margin and 45° phase margin, respectively. These results are necessarily compatible with those obtained from the Nyquist plot.

8.5 Operational Amplifiers

Operational amplifiers are feedback amplifiers with very high loop gain. The gain of an operational amplifier depends almost entirely on the feedback factor β:

$$\text{Gain} = \frac{A}{1 - A\beta},$$

where A is the amplifier gain in the absence of feedback. When $A\beta \gg 1$,

$$\text{Gain} \simeq -\frac{1}{\beta}.$$

As a result of this feature, operational amplifiers are used to achieve precise gain characteristics by means of suitable feedback networks. The correct operation of the operational amplifier presumes that factors relating to stability have been taken care of in the design of the open-loop circuitry.

Figure 8.12 shows a typical operational amplifier designed to accept three separate input voltages, taken with respect to ground. The impedances of the amplifier can be pure resistances or complex impedances.
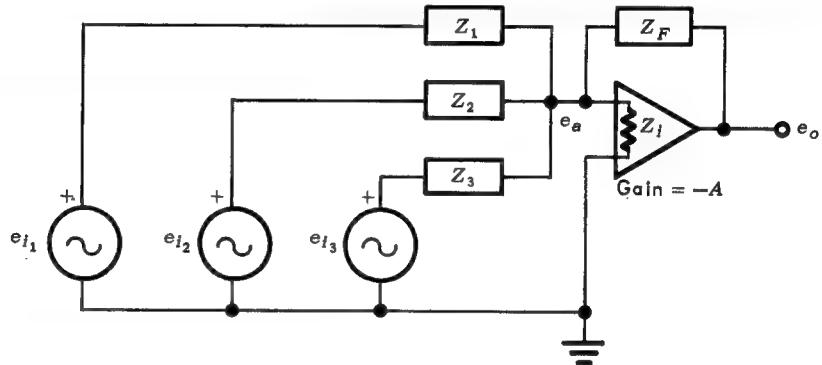
Fig. 8.12 Operational amplifier, including input summing circuit.

PROBLEM 8.10 For the circuit of Fig. 8.12, find the expressions for gain e_o/e_{i_1}, e_o/e_{i_2}, and e_o/e_{i_3}.

Solution: Let the voltage at the amplifier input be e_a. Then, by summing currents,

$$\frac{e_{i_1} - e_a}{Z_1} + \frac{e_{i_2} - e_a}{Z_2} + \frac{e_{i_3} - e_a}{Z_3} = \frac{e_a - e_o}{Z_F} + \frac{e_a}{Z_i}.$$

Rearranging,

$$\frac{e_{i_1}}{Z_1} + \frac{e_{i_2}}{Z_2} + \frac{e_{i_3}}{Z_3} = e_a \left(\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + \frac{1}{Z_i} + \frac{1}{Z_F} \right) - \frac{e_o}{Z_F}.$$

However, $e_o = -A e_a$ (the negative sign means negative feedback). Therefore,

$$\frac{e_{i_1}}{Z_1} + \frac{e_{i_2}}{Z_2} + \frac{e_{i_3}}{Z_3} = -\frac{e_o}{Z_F} \left[1 + \frac{Z_F}{A} \left(\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + \frac{1}{Z_i} + \frac{1}{Z_F} \right) \right]. \quad (8.31)$$

This is the fundamental equation for the required gains of the separate inputs. For the operational amplifier, gain A is very large (assume ∞), so that

$$\frac{e_{i_1}}{Z_1} + \frac{e_{i_2}}{Z_2} + \frac{e_{i_3}}{Z_3} \simeq -\frac{e_o}{Z_F}. \quad (8.32)$$

Equation (8.32) is a very accurate expression for the gain of operational amplifier circuits. The error in gain due to assuming $A = \infty$ is

$$-\frac{100}{A}\left(1 + \frac{Z_F}{Z_i} + \frac{Z_F}{Z_1} + \frac{Z_F}{Z_2} + \frac{Z_F}{Z_3}\right)\%.$$

PROBLEM 8.11 For the feedback amplifier of Fig. 8.12, $A = 100$, $Z_i = 100$ K Ω, $Z_2 = Z_3 = \infty$, $Z_1 = 100$ K Ω, $Z_F = 1$ M Ω. Find the exact gain, and compare with the gain calculated by the approximate formula (8.32).

Solution: The gain is obtained from

$$\frac{e_{i_1}}{10^5} = -\frac{e_o}{10^6}\left[1 + \frac{10^6}{100}\left(\frac{1}{10^5} + \frac{1}{10^5} + \frac{1}{10^6}\right)\right].$$

Simplifying,

$$e_{i_1} = -\frac{e_o}{10}(1.21) = -0.121\,e_o,$$

$$\frac{e_o}{e_{i_1}} = \text{gain} = -8.25.$$

The gain is -10 by the approximate formula. The approximation is poor because of the low gain, $A = 100$.

PROBLEM 8.12 Repeat the preceding problem for $A = 10^5$.

Solution: Substituting, as before,

$$\frac{e_{i_1}}{10^5} = -\frac{e_o}{10^6}\left[1 + \frac{10^6}{10^5}\left(\frac{1}{10^5} + \frac{1}{10^5} + \frac{1}{10^6}\right)\right].$$

Simplifying,

$$e_{i_1} = -\frac{e_o}{10}(1.00021), \qquad \frac{e_o}{e_{i_1}} = \frac{-10}{1.00021}.$$

The error introduced by using the approximate formula is 0.02%.

Note the applicability of the approximate gain formula to high-gain operational amplifiers. Gain is almost entirely dependent on the summing and feedback resistors. Stable resistors mean correspondingly stable gain.

PROBLEM 8.13 Refer to Fig. 8.12, with $Z_1 = 100$ K Ω, $Z_2 = 1$ M Ω, $Z_3 = 10$ K Ω, $Z_F = 10^6$. Let A be essentially infinite so that we may use (8.32). Find e_o in terms of e_{i_1}, e_{i_2}, and e_{i_3}.

Solution: The following is the required expression:

$$\frac{e_{i_1}}{10^5} + \frac{e_{i_2}}{10^6} + \frac{e_{i_3}}{10^4} = -\frac{e_o}{10^6}.$$

Simplifying,

$$-e_o = 10\,e_{i_1} + e_{i_2} + 100\,e_{i_3}.$$

The voltage e_o is the sum of the inputs, each input with an appropriate scale factor. The arrangement of input resistors is called a *summing network*.

PROBLEM 8.14 In the circuit of Fig. 8.10, $Z_F = 1/(j\omega C_F)$, where C_F is a feedback capacitor, $Z_1 = 1$ M Ω, $Z_2 = Z_3 = \infty$. Assume A is essentially infinite. Find the gain.

Solution: Substituting in (8.32),

$$\frac{e_i}{10^6} = -\frac{e_o}{\dfrac{1}{j\omega C_F}} = j\omega C_F\, e_o \; ,$$

$$\frac{e_o}{e_i} = \frac{j}{\omega C_F} \times 10^{-6}.$$

The gain varies inversely with the frequency of the input. This is a characteristic of an *integrator*. Output represents the *integral* of input. This circuit is widely used in analog computers to carry out the critical integration function.

8.6 Supplementary Problems

PROBLEM 8.15   What type of feedback produces low input impedance and low output impedance?

PROBLEM 8.16   What type of feedback produces high input impedance?

PROBLEM 8.17   What type of feedback is commonly used in operational amplifiers? (Cf., Fig. 8.12.)

PROBLEM 8.18   Discuss the advantages of negative feedback.

PROBLEM 8.19   If the voltage gain of an amplifier is $A_v = \dfrac{100(1000 + j\omega)}{1 + 0.1j\omega}$, find (a) the d-c gain, and   (b) the gain at 1 MHz.

PROBLEM 8.20   Using the block diagram of Fig. 8.3, let $A_1 = \dfrac{1000}{j\omega + 1}$, $A_2 = \dfrac{0.15 + 1}{0.015 + 1}$, and $\beta = 0.1$. Calculate   (a) $\dfrac{e_o}{e_d}(\omega)$, and   (b) $\dfrac{e_o}{e_i}$ at 1 Hz.

PROBLEM 8.21   Using the block diagram of Fig. 8.3, let $A_1 = \dfrac{500}{j\omega + 1}$, $A_2 = \dfrac{0.15 + 1}{0.015 + 1}$, and $\beta = 0.1$. Calculate   (a) $\dfrac{e_o}{e_i}$ at 1 Hz, and   (b) $\dfrac{e_o}{e_d}(\omega)$.

PROBLEM 8.22   Using the system of Prob. 8.20, determine the   (a) forward gain at 1 Hz,   (b) zero-frequency forward gain,   (c) feedback gain at 1 Hz, (d) zero-frequency open-loop gain,   (e) closed-loop gain at 1 Hz,   (f) zero-frequency closed-loop gain, and   (g) frequency at which the closed-loop has dropped 3 db below its initial value at zero-frequency.

PROBLEM 8.23   For the circuit of Fig. 8.9b, determine   (a) the closed-loop gain at $\omega = 200$,   (b) the change in the closed-loop gain at $\omega = 200$ if the stage gain increases from 10 to 20, and   (c) what happens if the stage gain is reduced to 7.

Fig. 8.13 The circuit of Prob. 8.24.

PROBLEM 8.24   For the transistor Q_1 in the circuit of Fig. 8.13 the parameters are $\beta = 100$, $r_e = 10\,\Omega$, $r_b = 0\,\Omega$, and $r_c = \infty$.   Determine   (a) the nature of the feedback used,   (b) $A_v = e_o/e_i$, and   (c) Z_{in} and Z_o.

TRANSISTOR CHARACTERISTICS

<div style="text-align: right">

A
APPENDIX

</div>

A.1 Types 2N929, 2N930 *n-p-n* Planar Silicon Transistors*

FOR EXTREMELY LOW-LEVEL, LOW-NOISE, HIGH-GAIN, SMALL-SIGNAL AMPLIFIER APPLICATIONS

- Guaranteed h_{FE} at 10 μa, $T_A = -55°C$ and 25°C
- Guaranteed Low-Noise Characteristics at 10 μa
- Usable at Collector Currents as Low as 1 μa
- Very High Reliability
- 2N929 and 2N930 Also Are Available to MIL-S-19500/253 (Sig C)

THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE

ALL JEDEC TO-18 DIMENSIONS AND NOTES ARE APPLICABLE

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
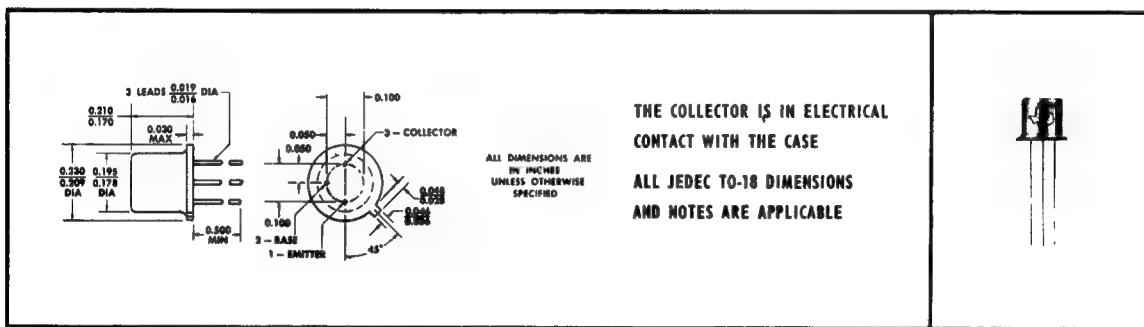
Fig. A.1 JEDEC registered mechanical data.

TABLE A.1   JEDEC registered absolute maximum ratings at 25°C free-air temperature (unless otherwise noted).

Collector-Base Voltage	45 v
Collector-Emitter Voltage (See Note 1)	45 v
Emitter-Base Voltage	5 v
Collector Current	30 ma
Total Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	300 mw
Total Device Dissipation at (or below) 25°C Case Temperature (See Note 3)	600 mw
Operating Collector Junction Temperature	175°C
Storage Temperature Range	−65°C to +300°C

[1] This value applies when the base-emitter diode is open circuited.
[2] Derate linearly to 175°C free-air temperature at the rate of 2.0 mw/C°.
[3] Derate linearly to 175°C case temperature at the rate of 4.0 mw/C°.

* TEXAS INSTRUMENTS Incorporated.

TABLE A.2   JEDEC registered electrical characteristics at 25°C free-air temperature (unless otherwise noted).

PARAMETER		TEST CONDITIONS	2N929		2N930		UNIT
			MIN	MAX	MIN	MAX	
BV$_{CEO}$	Collector-Emitter Breakdown Voltage	I$_C$ = 10 ma, I$_B$ = 0, (See Note 1)	45		45		v
BV$_{EBO}$	Emitter-Base Breakdown Voltage	I$_E$ = 10 na I$_C$ = 0	5		5		v
I$_{CBO}$	Collector Cutoff Current	V$_{CB}$ = 45 v, I$_E$ = 0		10		10	na
I$_{CES}$	Collector Cutoff Current (See Note 2)	V$_{CE}$ = 45 v, V$_{BE}$ = 0		10		10	na
		V$_{CE}$ = 45 v, V$_{BE}$ = 0, T$_A$ = 170°C		10		10	μa
I$_{CEO}$	Collector Cutoff Current	V$_{CE}$ = 5 v, I$_B$ = 0		2		2	na
I$_{EBO}$	Emitter Cutoff Current	V$_{EB}$ = 5 v, I$_C$ = 0		10		10	na
h$_{FE}$	Static Forward Current Transfer Ratio	V$_{CE}$ = 5 v, I$_C$ = 10 μa	40	120	100	300	
		V$_{CE}$ = 5 v, I$_C$ = 10 μa, T$_A$ = —55°C	10		20		
		V$_{CE}$ = 5 v, I$_C$ = 500 μa	60		150		
		V$_{CE}$ = 5 v, I$_C$ = 10 ma, (See Note 1)		350		600	
V$_{BE}$	Base-Emitter Voltage	I$_B$ = 0.5 ma, I$_C$ = 10 ma, (See Note 1)	0.6	1.0	0.6	1.0	v
V$_{CE(sat)}$	Collector-Emitter Saturation Voltage	I$_B$ = 0.5 ma, I$_C$ = 10 ma, (See Note 1)		1.0		1.0	v
h$_{ib}$	Small-Signal Common-Base Input Impedance	V$_{CB}$ = 5 v, I$_E$ = —1 ma, f = 1 kc	25	32	25	32	ohm
h$_{rb}$	Small-Signal Common-Base Reverse Voltage Transfer Ratio	V$_{CB}$ = 5 v, I$_E$ = —1 ma, f = 1 kc	0	6.0 x 10^{-4}	0	6.0 x 10^{-4}	
h$_{ob}$	Small-Signal Common-Base Output Admittance	V$_{CB}$ = 5 v, I$_E$ = —1 ma, f = 1 kc	0	1.0	0	1.0	μmho
h$_{fe}$	Small-Signal Common-Emitter Forward Current Transfer Ratio	V$_{CE}$ = 5 v, I$_C$ = 1 ma, f = 1 kc	60	350	150	600	
|h$_{fe}$|	Small-Signal Common-Emitter Forward Current Transfer Ratio	V$_{CE}$ = 5 v, I$_C$ = 500 μa, f = 30 mc	1.0		1.0		
C$_{ob}$	Common-Base Open-Circuit Output Capacitance	V$_{CB}$ = 5 v, I$_E$ = 0, f = 1 mc		8		8	pf

[1] These parameters must be measured using pulse techniques, PW = 300 μsec, Duty Cycle ≤ 2%.
[2] I$_{CES}$ may be used in place of I$_{CBO}$ for circuit stability calculations.

TABLE A.3   JEDEC registered operating characteristics at 25°C free-air temperature.

PARAMETER		TEST CONDITIONS	2N929	2N930	UNIT
			MAX	MAX	
$\overline{NF}$	Average Noise Figure	V$_{CE}$ = 5 v, I$_C$ = 10 μa, R$_G$ = 10 kΩ Noise Bandwidth 10 cps to 15.7 kc	4.0	3.0	db

A.1a Typical Characteristics
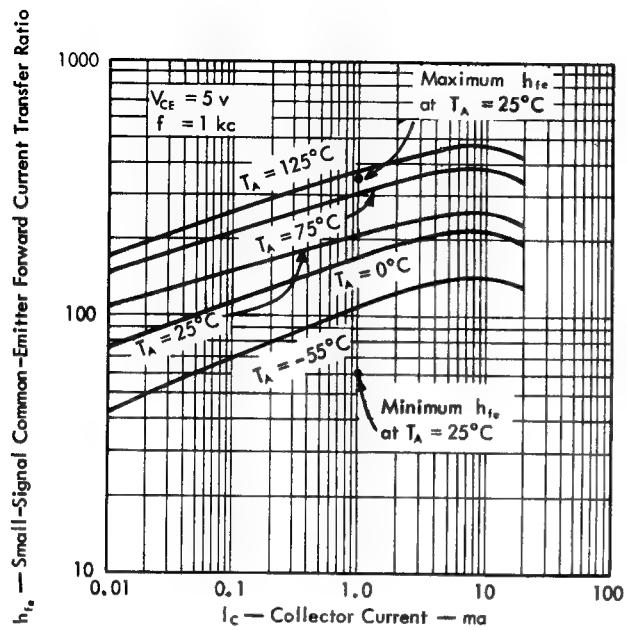
Fig. A.2 2N929 transistor: small-signal common-emitter forward current transfer ratio vs. collector current.
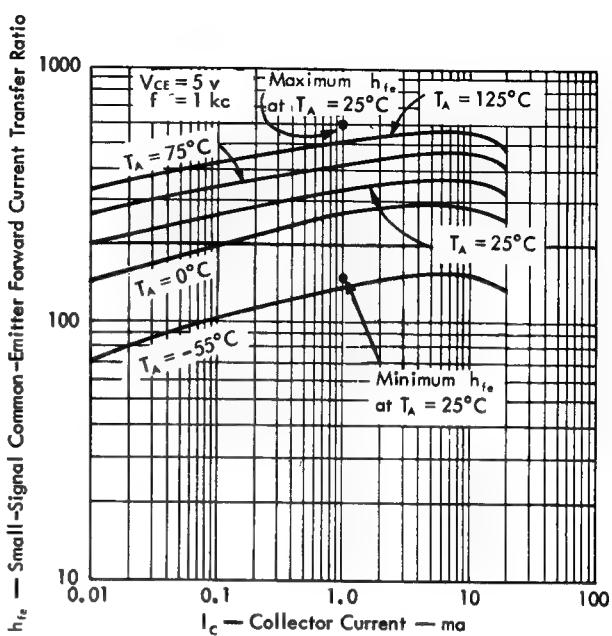
Fig. A.3 2N930 transistor: small-signal common-emitter forward current transfer ratio vs. collector current.
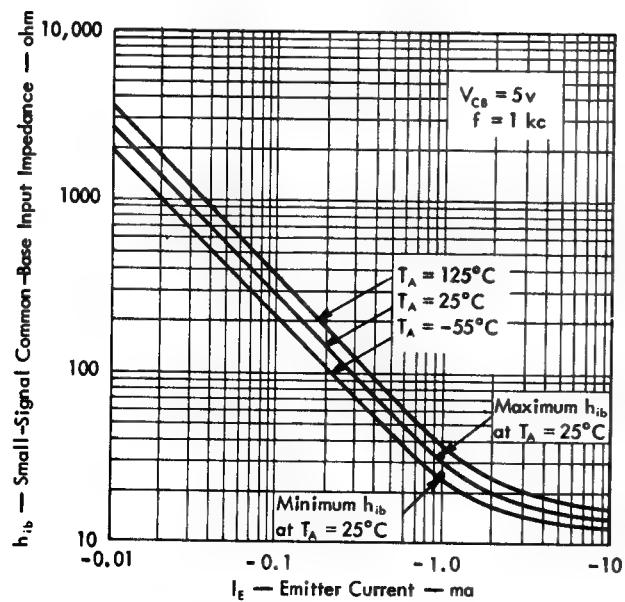
Fig. A.4 2N929 and 2N930 transistors: small-signal common-base input impedance vs. emitter current.
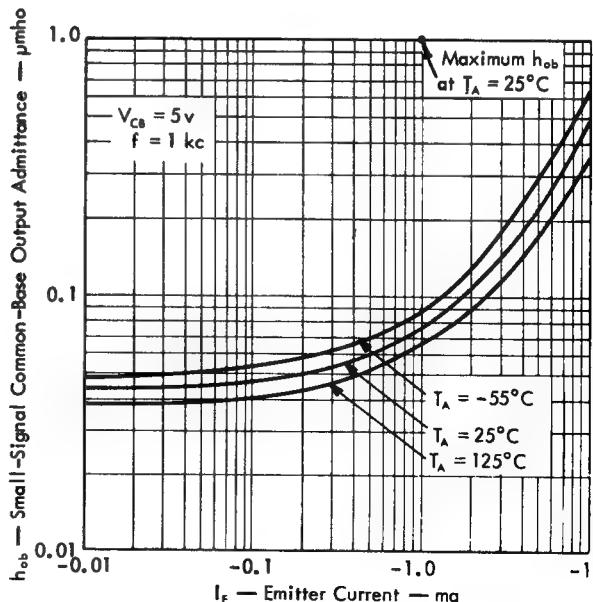
Fig. A.5 2N929 and 2N930 transistors: small-signal common-base output admittance vs. emitter current.
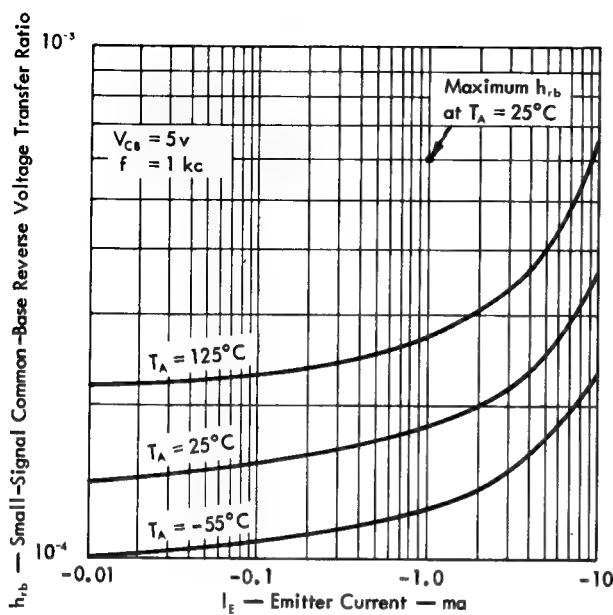
Fig. A.6 Small-signal common-base reverse voltage transfer ratio vs. emitter current.
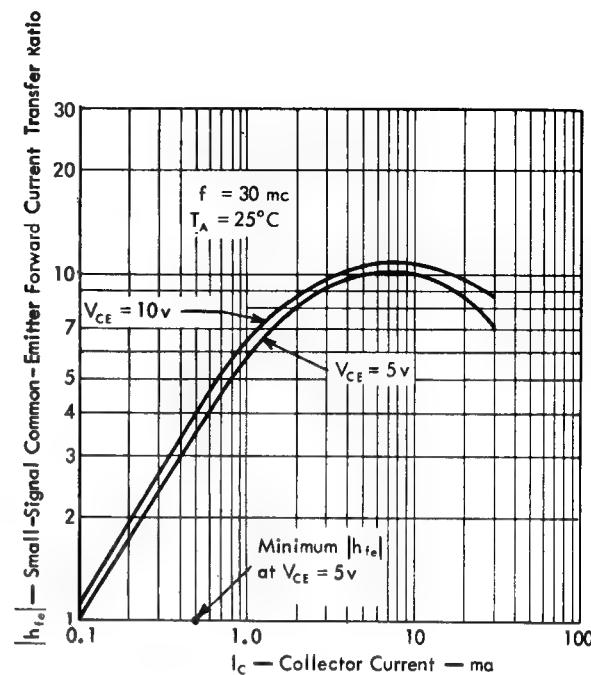
Fig. A.7 Small-signal common-emitter forward current transfer ratio vs. collector current.
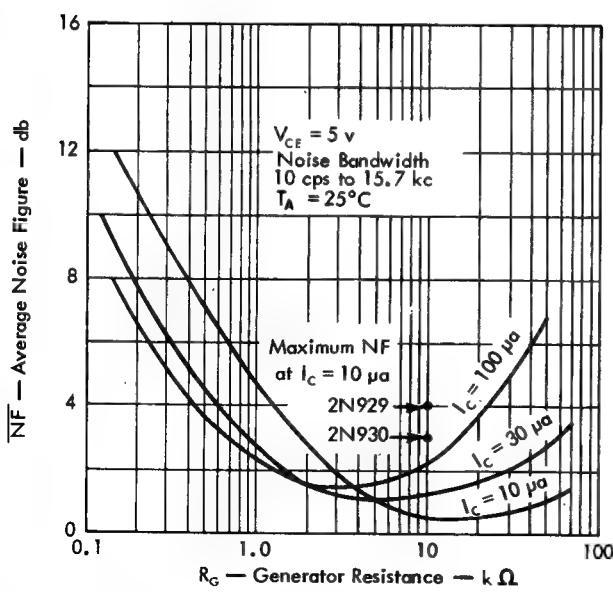
Fig. A.8 Average noise figure vs. generator resistance.
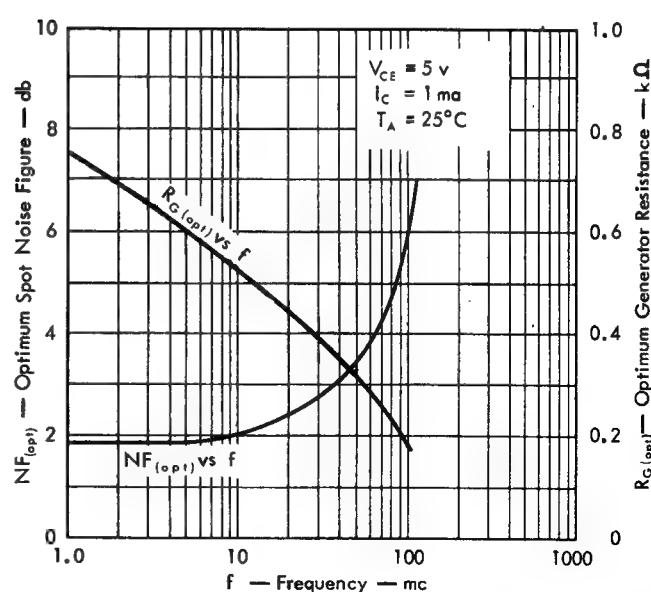
Fig. A.9 Optimum spot noise figure and optimum generator resistance vs. frequency.
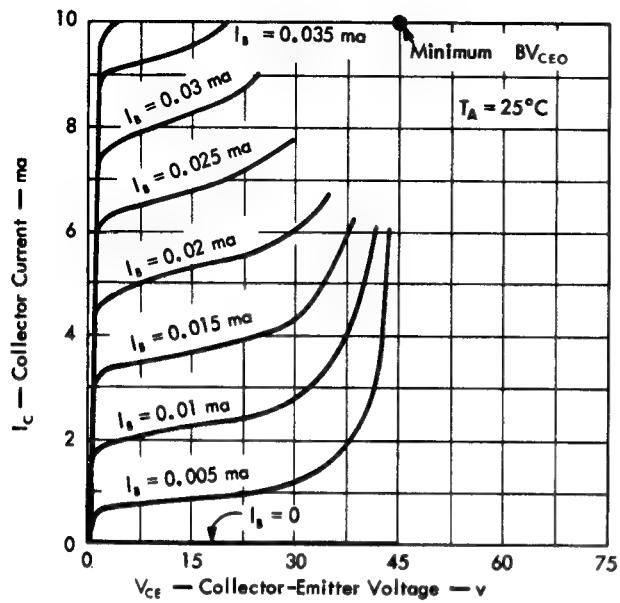
Fig. A.10   2N929 transistor: common-emitter
collector characteristics.
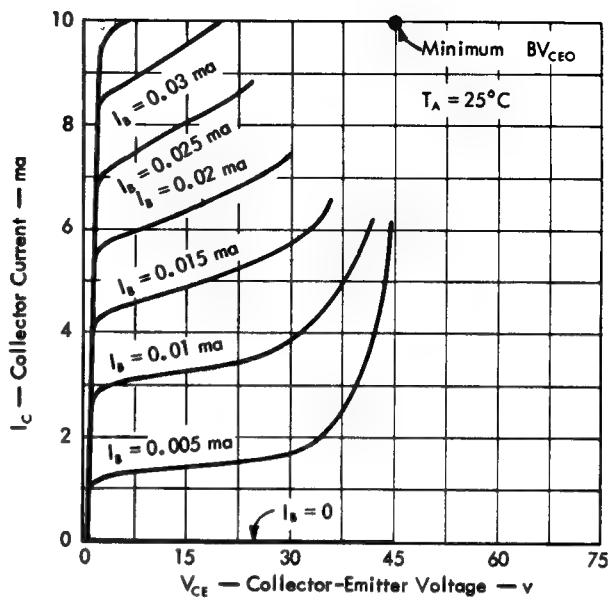
Fig. A.11   2N930 transistor: common-emitter
collector characteristics.
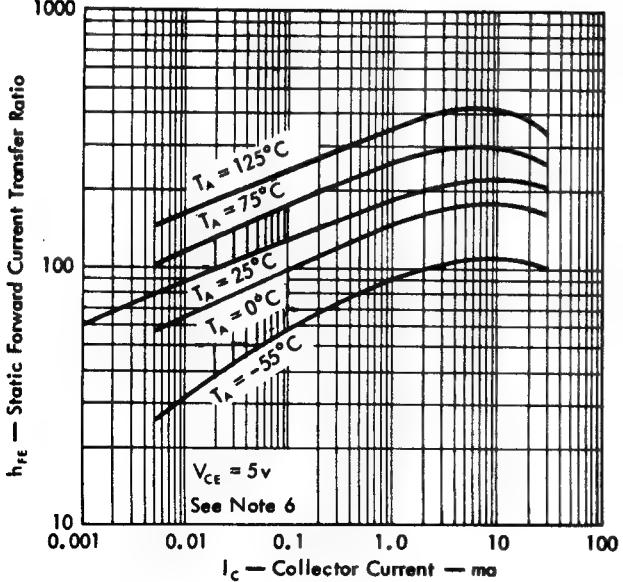
Fig. A.12   2N929 transistor: static forward current
transfer ratio vs. collector current. Note that these
parameters were measured using pulse techniques,
PW = 300 μsec, Duty Cycle $\leq$ 2%.
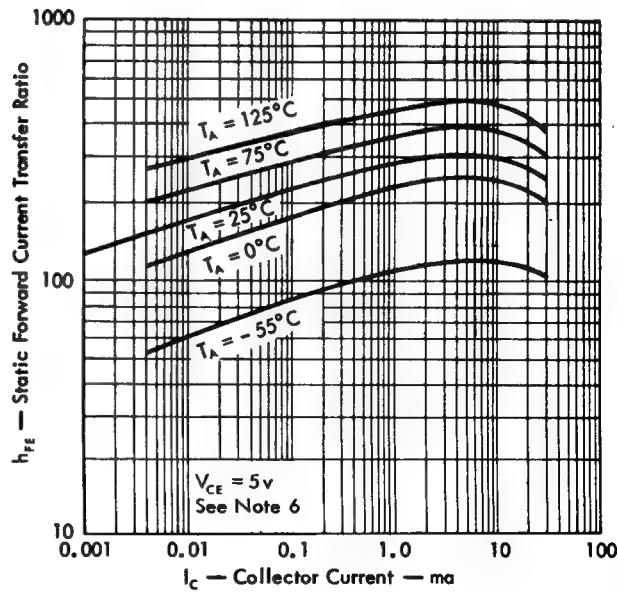
Fig. A.13   2N930 transistor: static forward current
transfer ratio vs. collector current. Note that these
parameters were measured using pulse techniques,
PW = 300 μsec, Duty Cycle $\leq$ 2%.
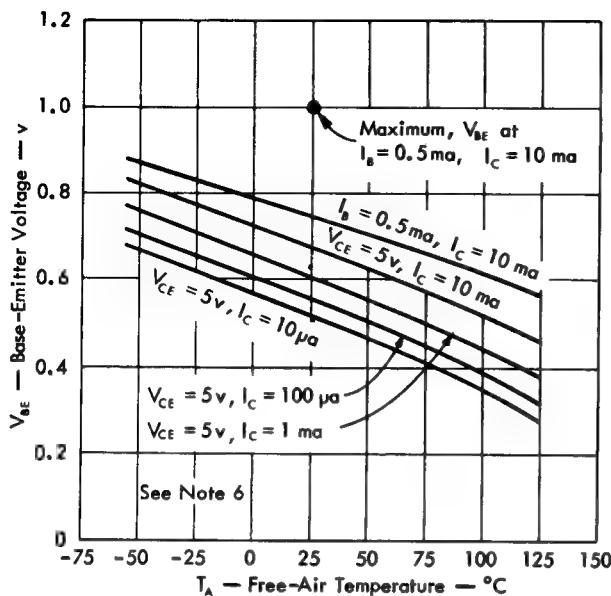
Fig. A.14 2N929 transistor: base-emitter voltage
vs. free-air temperature.
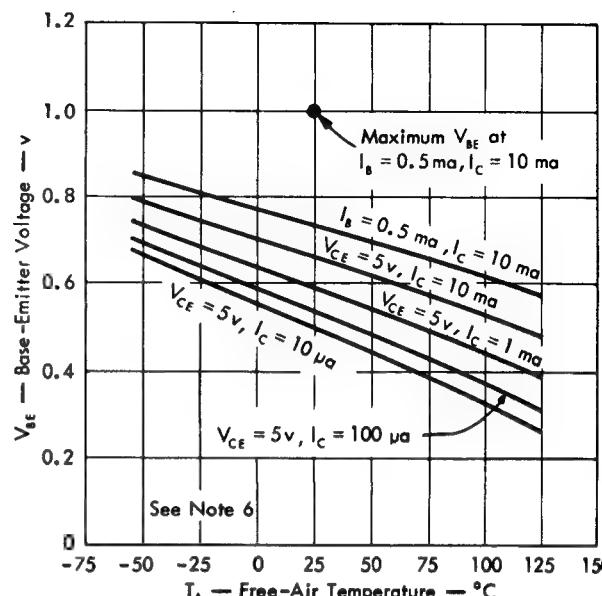
Fig. A.15 2N930 transistor: base-emitter voltage
vs. free-air temperature.
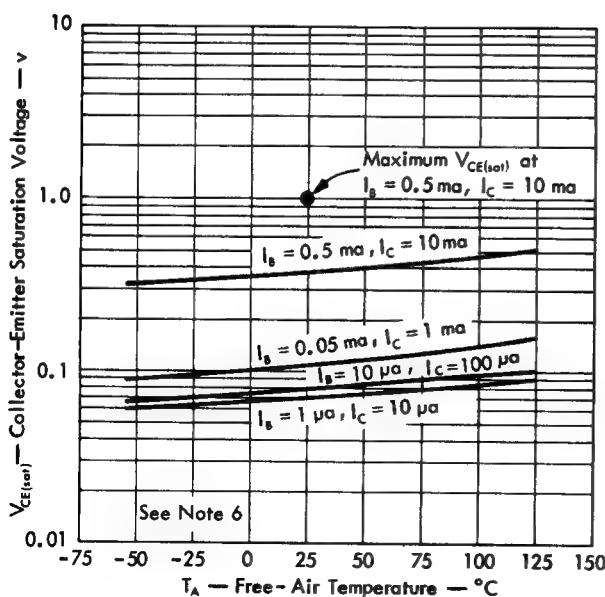
Fig. A.16 2N929 transistor: collector-emitter satu-
ration voltage vs. free-air temperature. Note that
these parameters were measured using pulse tech-
niques, PW = 300 μsec, Duty Cycle $\leq$ 2%.
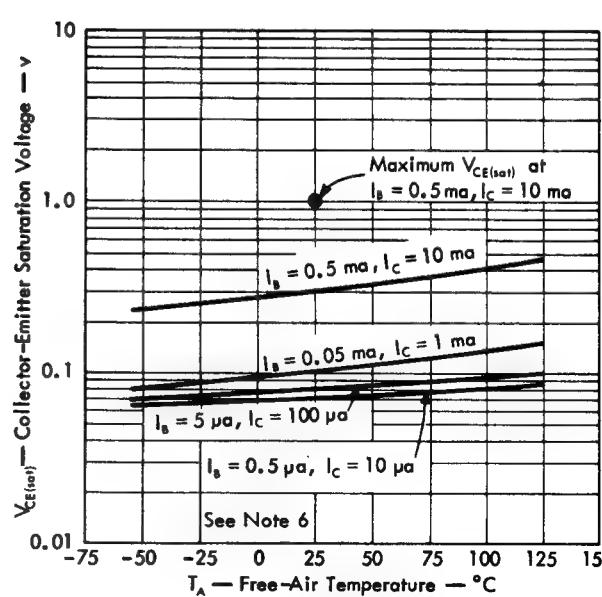
Fig. A.17 2N930 transistor: collector-emitter satu-
ration voltage vs. free-air temperature. Note that
these parameters were measured using pulse tech-
niques, PW = 300 μsec, Duty Cycle $\leq$ 2%.

A.2   Types 2N1162 thru 2N1167 Transistors*

TABLE A.4 Electrical characteristics, general. (At case temperature of 25°C ± 3° except where noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector Cutoff Current	I_{CBO}				
$\quad V_{CB} = BV_{CBO}$ (max), $I_E = 0$		—	3	15	mA
$\quad V_{CB} = 2V$, $I_E = 0$		—	125	225	μA
$\quad V_{CB} = 15V$, $I_E = 0$, $T_C = 90°C$ (2N1162, 2N1163)		—	10	20	mA
$\quad V_{CB} = 30V$, $I_E = 0$, $T_C = 90°C$ (2N1164 through 2N1167)		—	10	20	mA
Collector-Emitter Breakdown Voltage	BV_{CES}				
$\quad I_C = 500mA$, $V_{EB} = 0$ (2N1162, 2N1163)		35	—	—	Vdc
$\quad$ (2N1164, 2N1165)		60	—	—	Vdc
$\quad$ (2N1166, 2N1167)		75	—	—	Vdc
Emitter Cutoff Current	I_{EBO}				
$\quad V_{BE} = 12V$, $I_C = 0$		—	0.5	1.2	mA
Collector – Emitter Saturation Voltage	$V_{CE(SAT)}$				
$\quad I_C = 25A$, $I_B = 1.6A$		—	0.3	1.0	Vdc
Base - Emitter Drive Voltage (at Saturation)	V_{BE}				
$\quad I_C = 25A$, $I_B = 1.6A$		—	0.7	1.7	Vdc

TABLE A.5 Electrical characteristics, common emitter.

Characteristic	Symbol	Min	Typ	Max	Unit
DC Forward Current Gain	h_{FE}				
$\quad V_{CE} = 2V$, $I_C = 5A$		—	65	125	—
$\quad V_{CE} = 1V$, $I_C = 25A$		15	25	65	—
Frequency Cutoff					
$\quad V_{CE} = -2V$, $I_C = 2A$	f_{ae}	—	4	—	kc
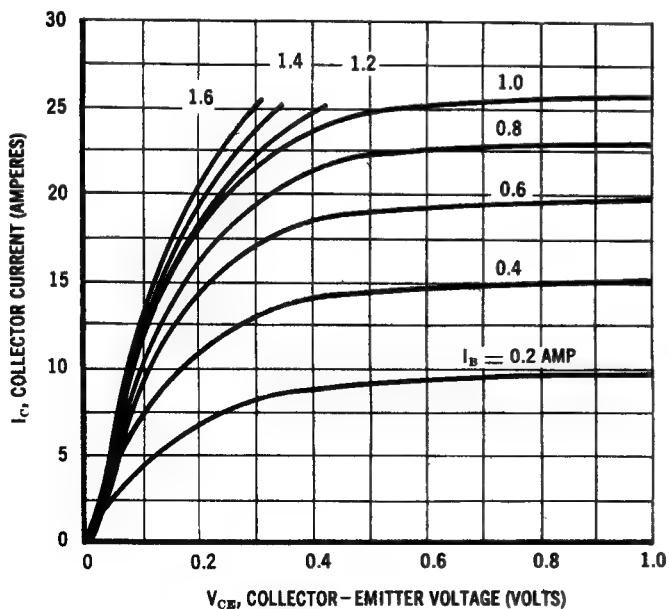
Fig. A.18 Saturation region, common emitter
(constant base current).
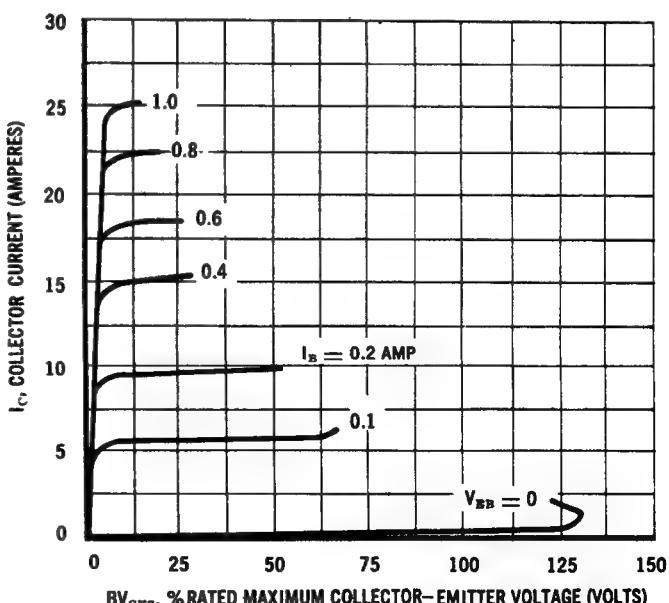
Fig. A.19 Collector characteristics, common emitter.

*MOTOROLA Inc., Semiconductor Products Division.
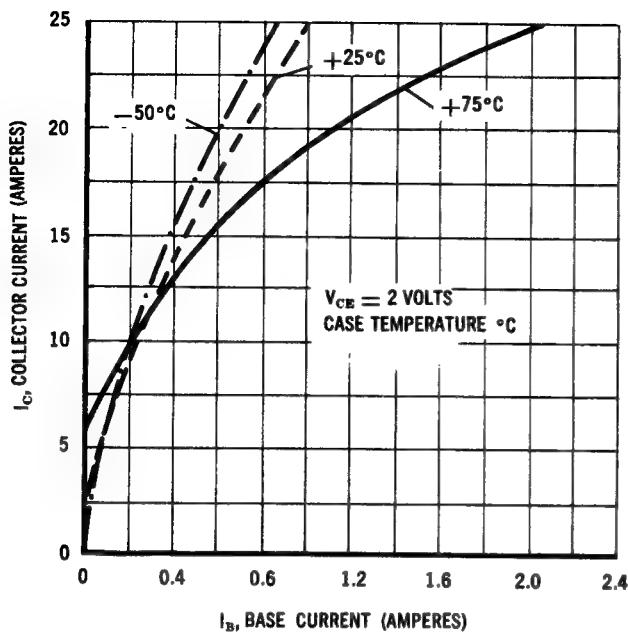
Fig. A.20 Collector current vs. base current.
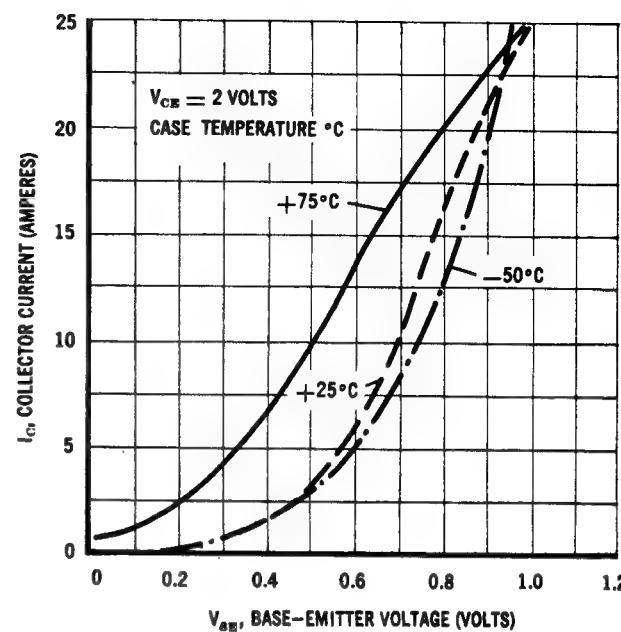

Fig. A.21 Output current vs. emitter-drive voltage.
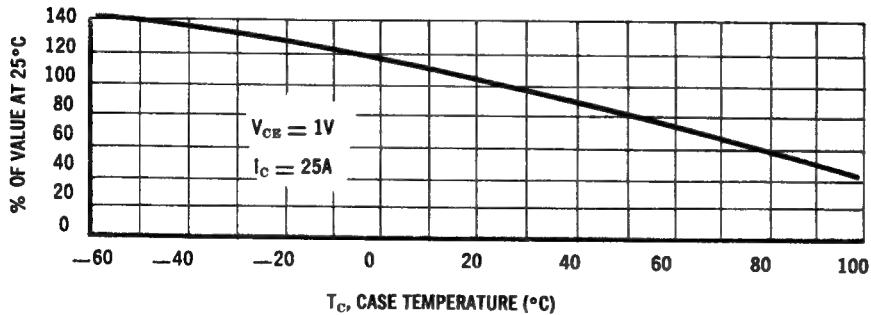

Fig. A.22 h_{FE} vs. temperature.
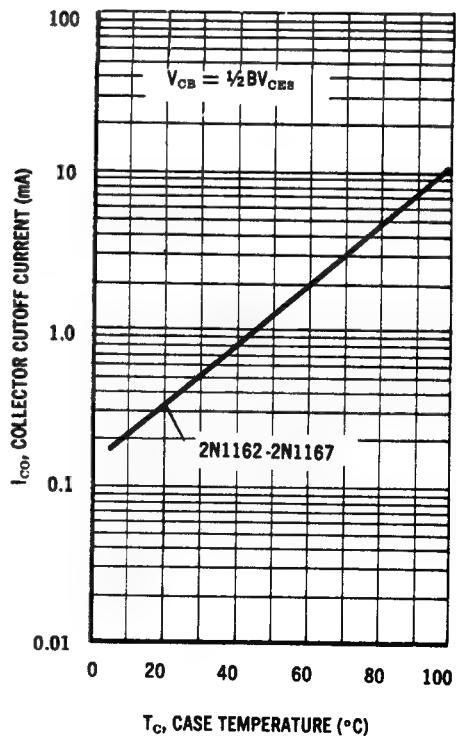

Fig. A.23 I_{CO} vs. temperature.
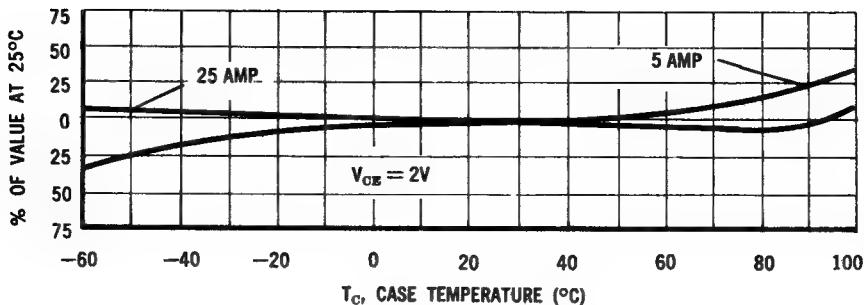
Fig. A.24 g_{FE} vs. temperature.

A.2a Peak Power Derating

The peak allowable power is:

$$P_P = \frac{(T_J - T_A - \theta_{JA} P_{ss})}{\theta_{JC} \left(\dfrac{1}{C_P}\right) + \theta_{CA} (t_1/t)}$$

C_P is a coefficient of power as obtained from the chart. T_J is junction temperature in °C; T_A is ambient temperature in °C; θ_{JC} is junction to case thermal resistance in °C/W; θ_{CA} is case to ambient thermal resistance in °C/W; θ_{JA} is the sum of $\theta_{JC} + \theta_{CA}$; t_1 is pulse width; t is the pulse period; (t_1/t) is the duty cycle; P_{ss} is a constant power dissipation and P_P is the additional allowable pulse power dissipation above the amount of P_{ss}.

The above equation is usable when a heat sink is used which has thermal capacity very much larger than the transistors thermal capacity.

The chart is normalized with respect to the thermal time constant, which is on the order of 50 milliseconds for these power transistors. (Fig. A.25.)
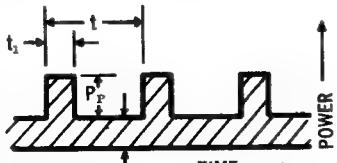
EXAMPLE
Given:

$P_{ss} = 10W$ $T_A = 40°C$
Pulse width $(t_1) = 1$ msec
Duty Cycle $= 20\%$
$\theta_{CA} = 3°C/W$
$\theta_{JC} = 0.8°C/W$ $T_{J\,max} = 100°C$

Solution: Enter the graph at $t_1/\tau = 1$ msec/50msec, and Duty Cycle 20%. Find $C_P = 5$. Solve equation

$$P_P = \frac{100 - 40 - (3 + 0.8)\,10}{\dfrac{0.8 + 3 \times 0.2}{5}}$$

$P_P = 29$ watts in addition to the steady 10 watts resulting in 39 watts peak.
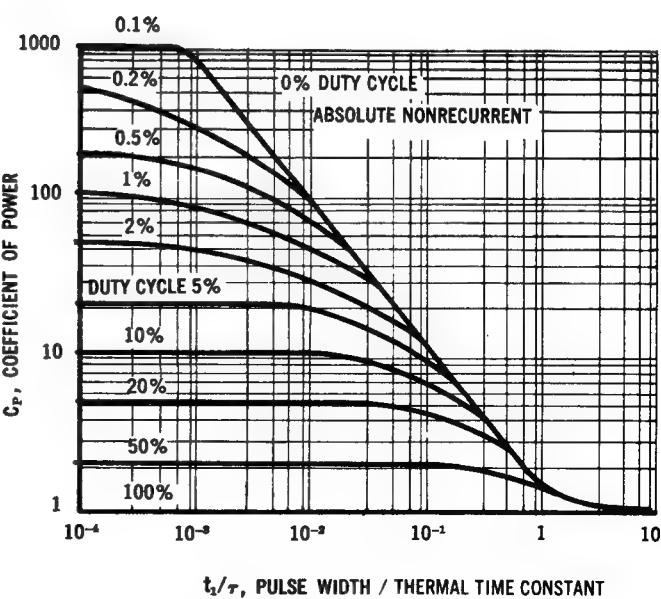
Fig. A.25 Normalized peak allowable power.

A.3 Types 2N1302, 2N1304, 2N1306, and 2N1308
n-p-n Alloy-Junction Germanium Transistors▲

TABLE A.6 JEDEC registered electrical characteristics at 25°C free-air temperature.

PARAMETER		TEST CONDITIONS	2N1302			2N1304			2N1306			2N1308			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
BV_{CBO}	Collector-Base Breakdown Voltage	$I_E = 100\ \mu a$, $I_E = 0$	25	—	—	25	—	—	25	—	—	25	—	—	v
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = 100\ \mu a$, $I_C = 0$	25	—	—	25	—	—	25	—	—	25	—	—	v
*V_{PT}	Punch Through Voltage†	$V_{EBfl} = 1$ v	25	—	—	20	—	—	15	—	—	15	—	—	v
*I_{CBO}	Collector Cutoff Current	$V_{CB} = 25$ v, $I_E = 0$	—	3	6	—	3	6	—	3	6	—	3	6	μa
*I_{EBO}	Emitter Cutoff Current	$V_{EB} = 25$ v, $I_C = 0$	—	2	6	—	2	6	—	2	6	—	2	6	μa
*h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 1$ v, $I_C = 10$ ma	20	100	—	40	115	200	60	130	300	80	160	—	—
		$V_{CE} = 0.35$ v, $I_C = 200$ ma	10	100	—	15	110	—	20	125	—	20	140	—	—
*V_{BE}	Base-Emitter Voltage	$I_B = 0.5$ ma, $I_C = 10$ ma	0.15	0.22	0.40	0.15	0.22	0.35	0.15	0.22	0.35	0.15	0.22	0.35	v
*$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = 0.5$ ma, $I_C = 10$ ma	—	0.07	0.20	—	—	—	—	—	—	—	—	—	v
		$I_B = 0.25$ ma, $I_C = 10$ ma	—	—	—	—	0.07	0.20	—	—	—	—	—	—	v
		$I_B = 0.17$ ma, $I_C = 10$ ma	—	—	—	—	—	—	—	0.07	0.20	—	—	—	v
		$I_B = 0.13$ ma, $I_C = 10$ ma	—	—	—	—	—	—	—	—	—	—	0.07	0.20	v
h_{ib}	Small-Signal Common-Base Input Impedance	$V_{CB} = 5$ v, $I_E = -1$ ma $f = 1$ kc	—	28	—	—	28	—	—	28	—	—	28	—	ohm
h_{rb}	Small-Signal Common-Base Reverse Voltage Transfer Ratio	$V_{CB} = 5$ v, $I_E = -1$ ma $f = 1$ kc	—	5×10^{-4}	—	—	5×10^{-4}	—	—	5×10^{-4}	—	—	5×10^{-4}	—	—
h_{ob}	Small-Signal Common-Base Output Admittance	$V_{CB} = 5$ v, $I_E = -1$ ma $f = 1$ kc	—	0.34	—	—	0.34	—	—	0.34	—	—	0.34	—	μmho
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = 5$ v, $I_C = 1$ ma $f = 1$ kc	—	105	—	—	120	—	—	135	—	—	170	—	—
*f_{hfb}	Common-Base Alpha-Cutoff Frequency	$V_{CB} = 5$ v, $I_E = -1$ ma	3	12	—	5	14	—	10	16	—	15	20	—	mc
*C_{ob}	Common-Base Open Circuit Output Capacitance	$V_{CB} = 5$ v, $I_E = 0$ $f = 1$ mc	—	14	20	—	14	20	—	14	20	—	14	20	pf
C_{ib}	Common-Base Open-Circuit Input Capacitance	$V_{EB} = 5$ v, $I_C = 0$ $f = 1$ mc	—	13	—	—	13	—	—	13	—	—	13	—	pf

†V_{PT} is determined by measuring the emitter-base floating potential V_{EBfl}. The collector-base voltage, V_{CB}, is increased until $V_{EBfl} = 1$ volt; this value of $V_{CB} = (V_{PT} + 1$ v).

TABLE A.7 JEDEC registered switching characteristics at 25°C free-air temperature.

PARAMETER		TEST CONDITIONS††	2N1302			2N1304			2N1306			2N1308			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_d	Delay Time	$I_C = 10$ ma, $I_{B(1)} = 1.3$ ma	—	0.07	—	—	0.07	—	—	0.06	—	—	0.06	—	μsec
t_r	Rise Time	$I_{B(2)} = -0.7$ ma, $V_{BE\ (off)} = -0.8$ v	—	0.20	—	—	0.20	—	—	0.18	—	—	0.15	—	μsec
t_s	Storage Time	$R_L = 1$ kΩ (See Fig. 1)	—	0.70	—	—	0.70	—	—	0.64	—	—	0.64	—	μsec
t_f	Fall Time		—	0.40	—	—	0.40	—	—	0.36	—	—	0.34	—	μsec
Q_{sb}	Stored Base Charge	$I_{B(1)} = 1$ ma, $I_C = 10$ ma (See Fig. 2)	—	800	—	—	760	—	—	720	—	—	680	—	pcb

††Voltage and current values shown are nominal; exact values vary slightly with device parameters.

TABLE A.8 JEDEC registered operating characteristics at 25°C free-air temperature.

PARAMETER		TEST CONDITIONS	2N1302			2N1304			2N1306			2N1308			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
NF	Spot Noise Figure	$V_{CB} = 5$ v $I_E = -1$ ma $f = 1$ kc, $R_G = 1$ kΩ	—	4	—	—	4	—	—	3	—	—	3	—	db

*Indicates JEDEC registered data (typical values excluded).

▲ TEXAS INSTRUMENTS Incorporated.

A.3a Typical Characteristics
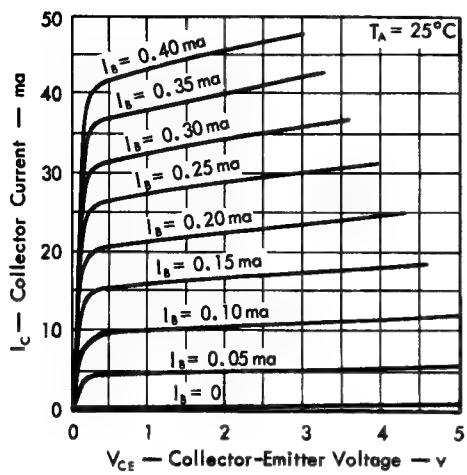

Fig. A.26 2N1302 transistor.
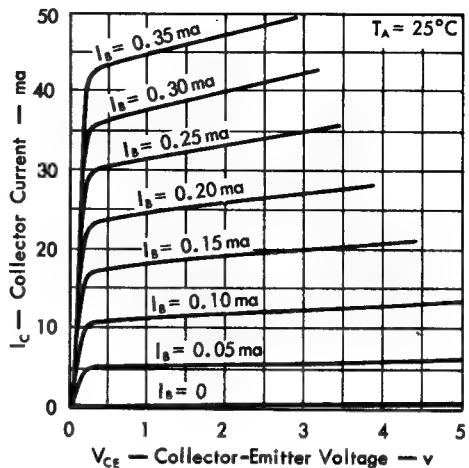

Fig. A.27 2N1304 transistor.
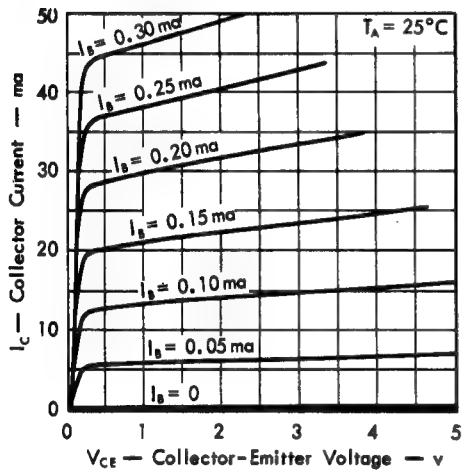

Fig. A.28 2N1306 transistor.
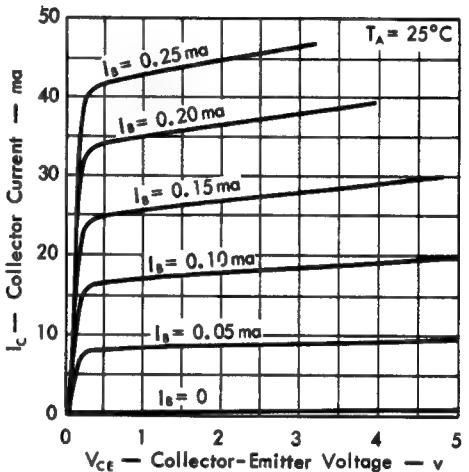

Fig. A.29 2N1308 transistor.
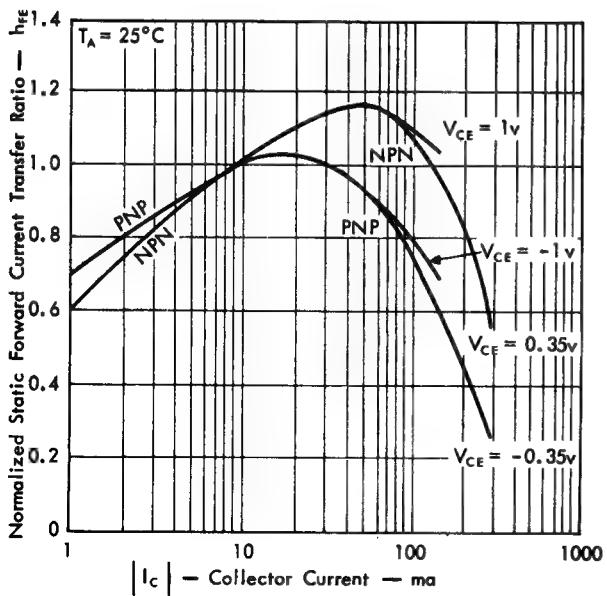
Fig. A.30 Normalized static forward current transfer ratio vs. collector current.
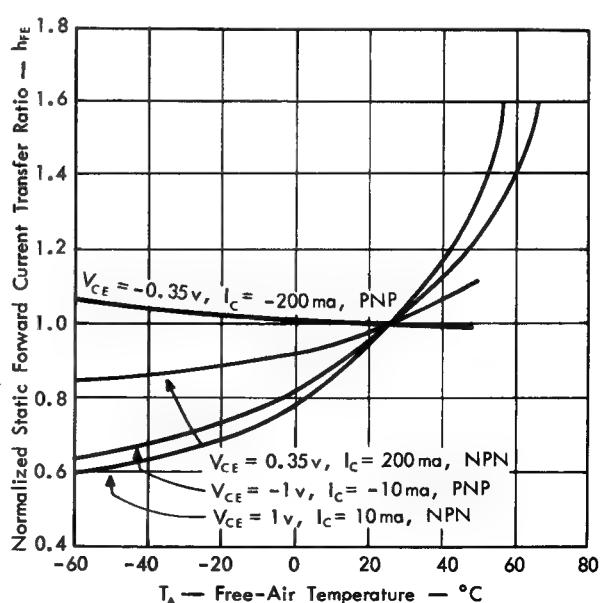
Fig. A.31 Normalized static forward current transfer ratio vs. free-air temperature.
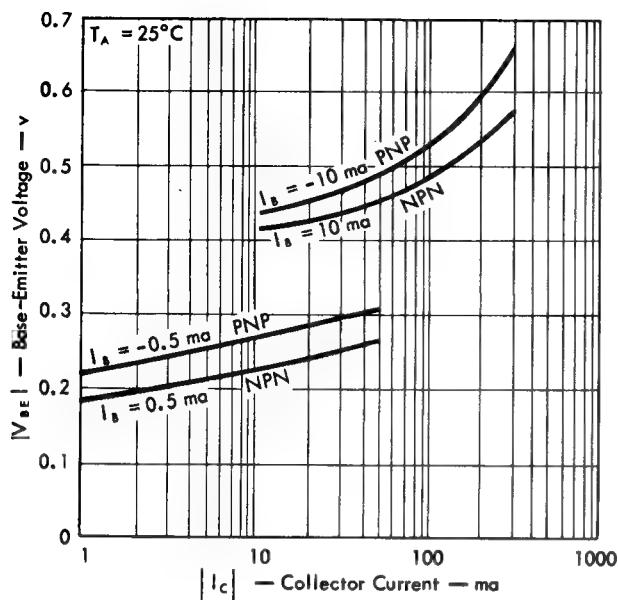
Fig. A.32 Base-emitter voltage vs. collector current.
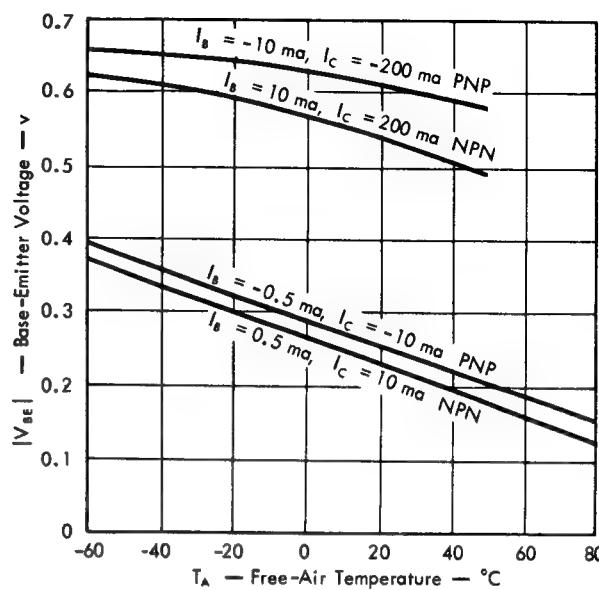
Fig. A.33 Base-emitter voltage vs. free-air temperature.
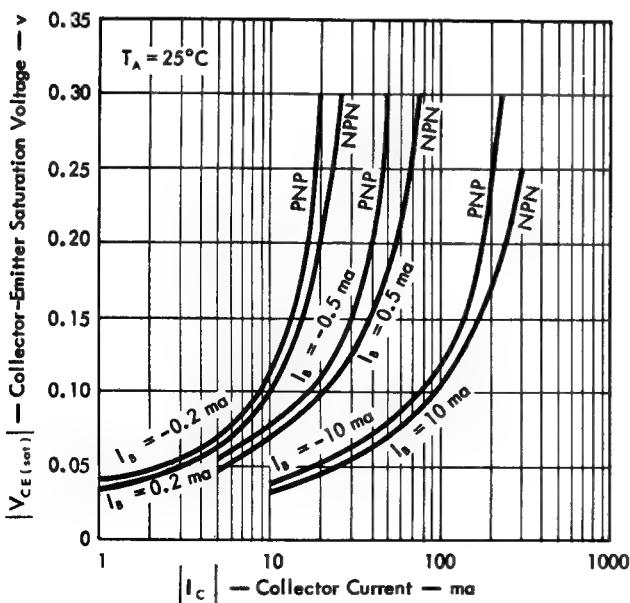
Fig. A.34 Collector-emitter saturation voltage vs. collector current.
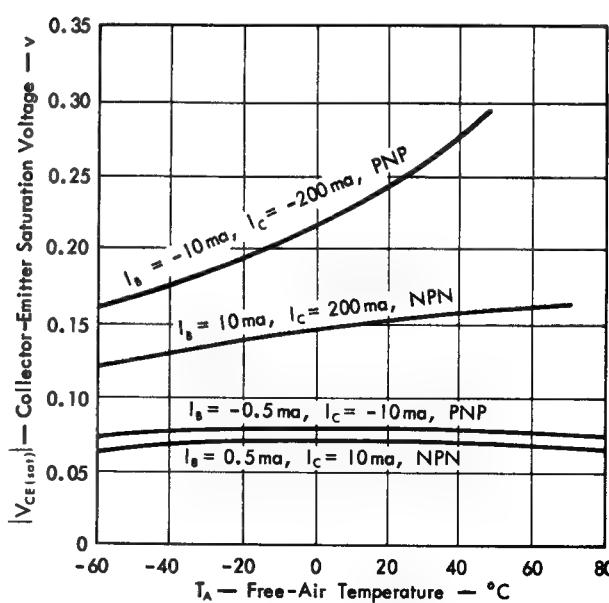
Fig. A.35 Collector-emitter saturation voltage vs. free-air temperature.
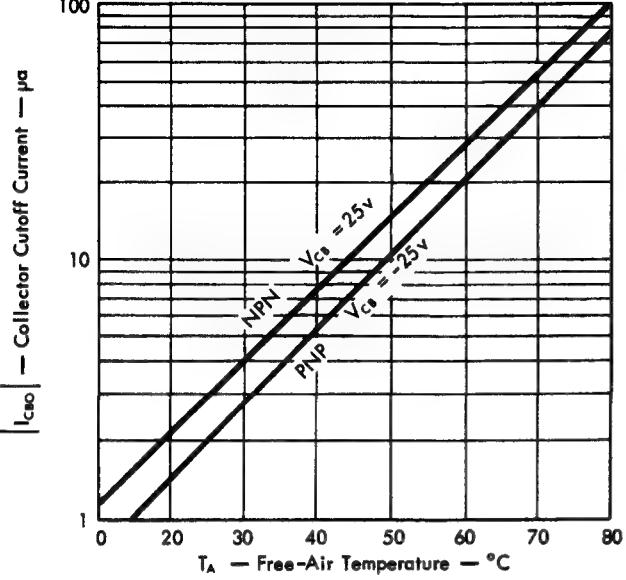
Fig. A.36 Collector cutoff current vs. free-air temperature.
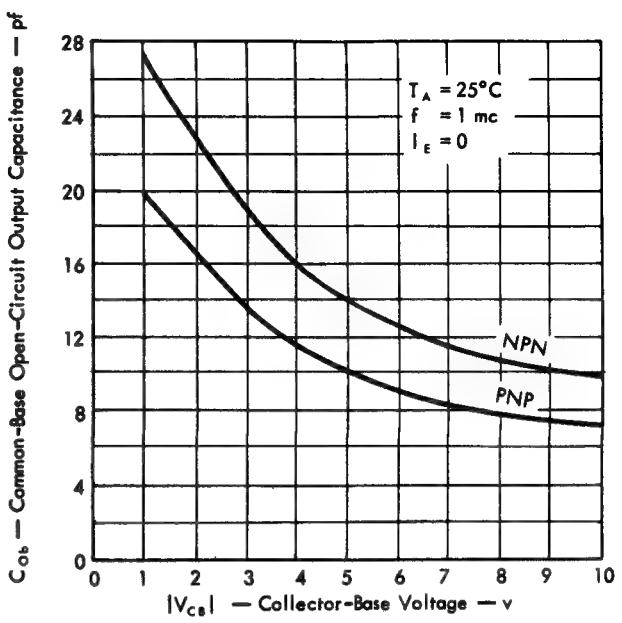
Fig. A.37 Common-base open-circuit output capacitance vs. collector-base voltage.
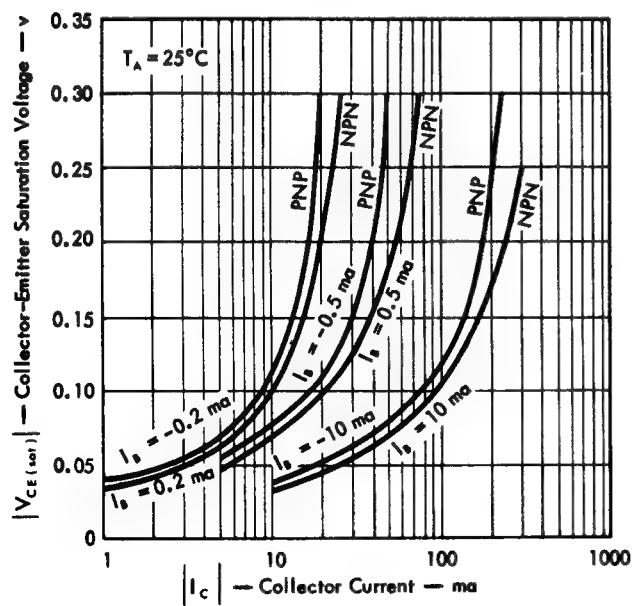
Fig. A.38 Collector-emitter saturation voltage vs. collector current.
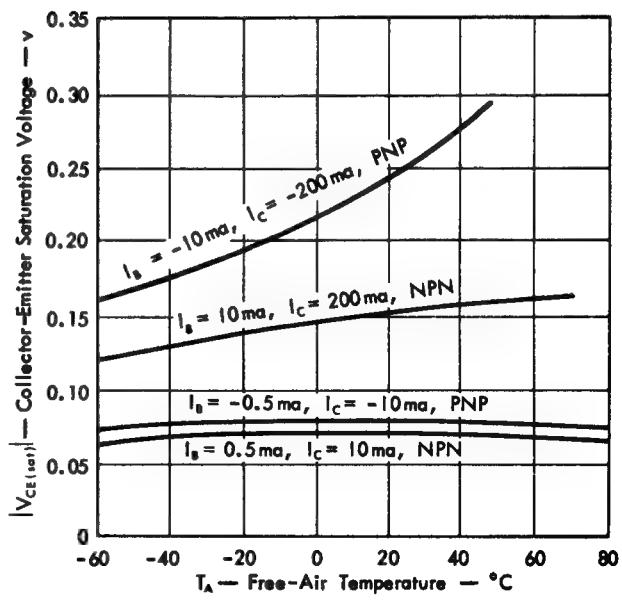
Fig. A.39 Collector-emitter saturation voltage vs. free-air temperature.

A.4 Types 2N1529A thru 2N1532A, 2N1534A thru 2N1537A and 2N1529 thru 2N1538 Transistors▲

TABLE A.9 Electrical characteristics. (At 25°C case temperature unless otherwise specified.) AQL and inspectio levels apply to "MEG-A-LIFE" series (2N1529A thru 2N1532A and 2N1534A thru 2N1537A) only. Thermal resistance, θ_{JC} ½ 0.6°C/W typical, 0.8°C/W maximum.

| Parameter	Symbol			Min	Max	Unit
Collector-Base Cutoff Current	I_{CBO1}					mA
(V_{CB} = 25V) 2N1529A, 2N1534A*				—	2.0	
(V_{CB} = 40V) 2N1530A, 2N1535A*				—	2.0	
(V_{CB} = 55V) 2N1531A, 2N1536A*				—	2.0	
(V_{CB} = 65V) 2N1532A, 2N1537A*				—	2.0	
(V_{CB} = 80V) 2N1533, 2N1538				—	2.0	
Collector-Base Cutoff Current	I_{CBO}					mA
(VCB = 2V) All Types				—	0.2	
(V_{CB} = 1/2 BV_{CES} rating; All Types T_C = +90°C)					20	
Emitter-Base Cutoff Current	I_{EBO}					mA
(V_{EB} = 12V) All Types				—	0.5	
Collector-Emitter Breakdown Voltage	BV_{CES}					volts
(I_C = 500 mA, V_{EB} = 0)						
2N1529A, 2N1534A*				30	—	
2N1530A, 2N1535A*				45	—	
2N1531A, 2N1536A*				60	—	
2N1532A, 2N1537A*				75	—	
2N1533, 2N1538				90	—	
Collector-Emitter Leakage Current	I_{CEX}					mA
(V_{BE} = 1V; V_{CE} @ rated BV_{CBO}) All Types				—	20	
Collector-Emitter Breakdown Voltage	BV_{CEO}					volts
(I_C = 500 mA, I_B = 0)						
2N1529A, 2N1534A*				20	—	
2N1530A, 2N1535A*				30	—	
2N1531A, 2N1536A*				40	—	
2N1532A, 2N1537A*				50	—	
2N1533, 2N1538				60	—	
Collector-Base Breakdown Voltage	BV_{CBO}					volts
(I_C = 20 mA)						
2N1529A, 2N1534A*				40	—	
2N1530A, 2N1535A*				60	—	
2N1531A, 2N1536A*				80	—	
2N1532A, 2N1537A*				100	—	
2N1533, 2N1538				120	—	
Current-Gain	h_{FE1}					—
(V_{CE} = 2V, I_C = 3A)						
2N1529A - 2N1532A				20	40	
2N1534A - 2N1537A				35	70	
2N1529 - 2N1533				20	40	
2N1534 - 2N1538				35	70	
Base-Emitter Drive Voltage	V_{BE}					volts
(I_C = 3A, I_B = 300 mA)						
2N1529A - 2N1532A				—	1.7	
2N1534A - 2N1537A				—	1.5	
2N1529 - 2N1533				—	1.7	
2N1534 - 2N1538				—	1.5	
Collector Saturation Voltage	$V_{CE(sat)}$					volts
(I_C = 3A, I_B = 300 mA)						
2N1529A - 2N1532A				—	1.5	
2N1534A - 2N1537A				—	1.2	
2N1529 - 2N1533				—	1.5	
2N1534 - 2N1538				—	1.2	
Transconductance	g_{FE}					mhos
(V_{CE} = 2V, I_C = 3A)						
2N1529A - 2N1532A				1.2	—	
2N1534A - 2N1537A				1.5	—	
2N1529 - 2N1533				1.2	—	
2N1534 - 2N1538				1.5	—	

*   Characteristics apply also to corresponding, non-A type numbers
** Each parameter of the "MEG-A-LIFE" series only is guaranteed to an individual AQL of 0.65%, inspection level II

▲MOTOROLA Inc., Semiconductor Products Division.

Fig. A.40 Power-temperature derating curve. The maximum continuous power is related to maximum junction temperature, by the thermal resistance factor. For d-c or frequencies below 25 cps the transistor must be operated within the constant $P_d = V_c \times I_c$ hyperbolic curve. This curve has a value of 90 watts at case temperatures of 25°C and is 0 watts at 100°C with a linear relation between the two temperatures such that allowable

$$P_d = \frac{100^{\circ} - T_c}{0.8}.$$

A.4a Collector Characteristics at 25°C: Types 2N1529A thru 2N1532A and 2N1529 thru 2N1533 Transistors
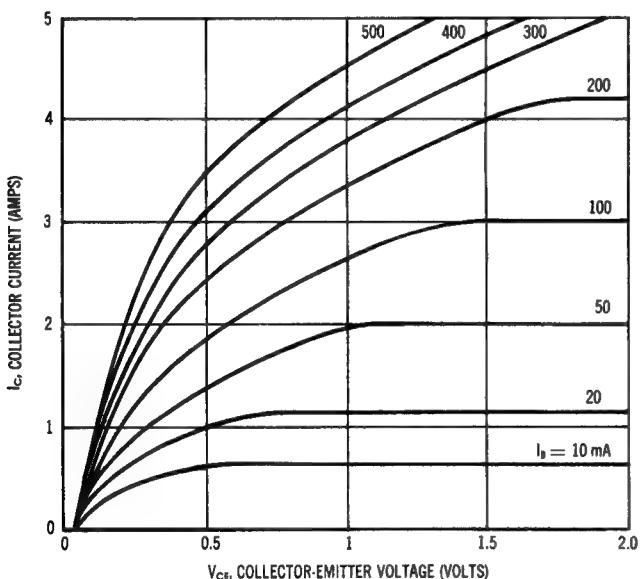
Fig. A.41 Saturation region, common emitter, constant base current.

Fig. A.42 Collector characteristics, common emitter.

Fig. A.43 Saturation region, common emitter, constant base current.
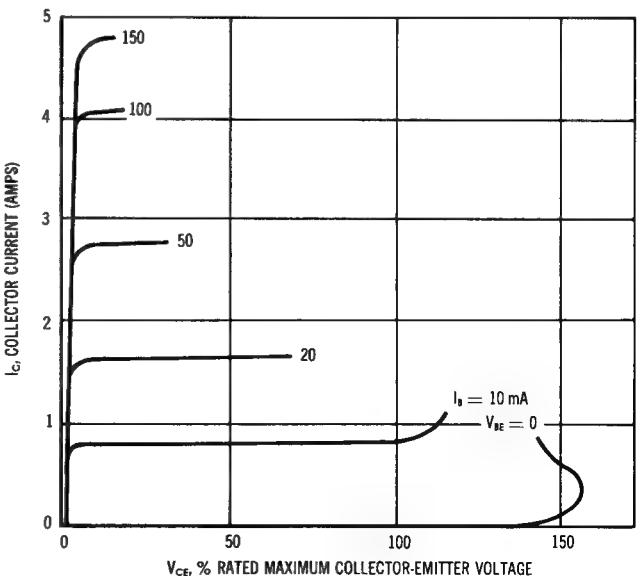
Fig. A.44 Collector characteristics, common emitter.
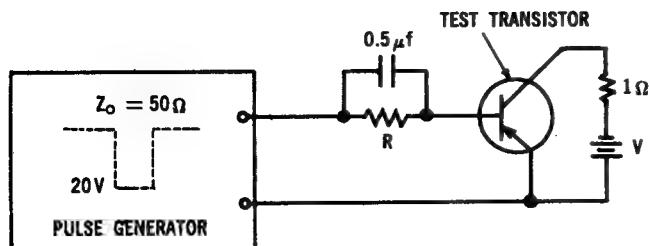
Fig. A.45 Switching time measuring circuit.
Also see Table A.10.

	I_C (Amps)	V (Volts)	I_{ON} (mA)	R (ohms)	$t_d + t_r$ (μsec)	t_s (μsec)	t_f (μsec)
2N1529A-32A 2N1529-33	3	3	300	65	10	2	5
2N1534A-37A 2N1534-38	3	3	200	100	8	3	5
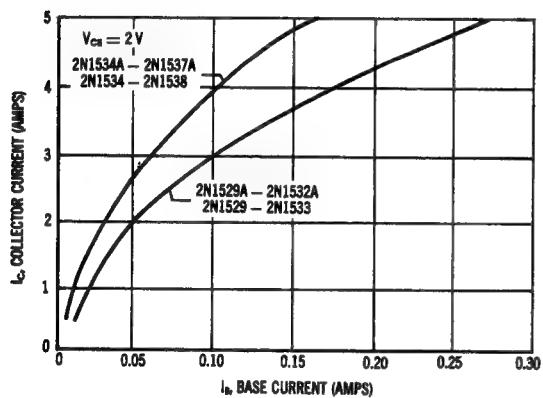
Fig. A.46 Collector current vs. base current.
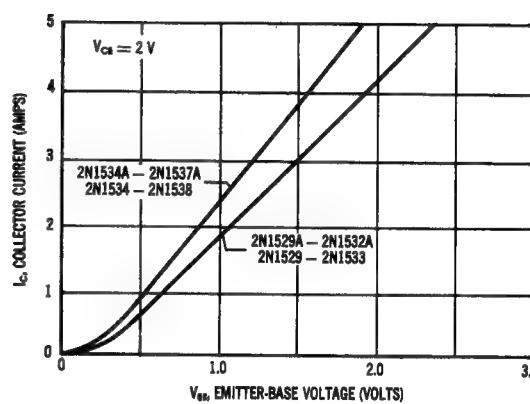

Fig. A.47 Collector current vs. emitter base voltage.
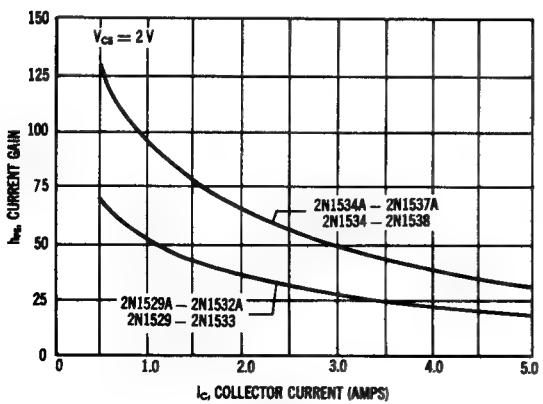

Fig. A.48 D-c current gain vs. collector current.
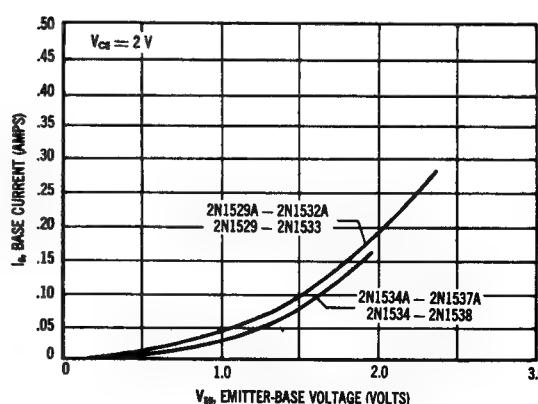
Fig. A.49 Base current vs. emitter base voltage.
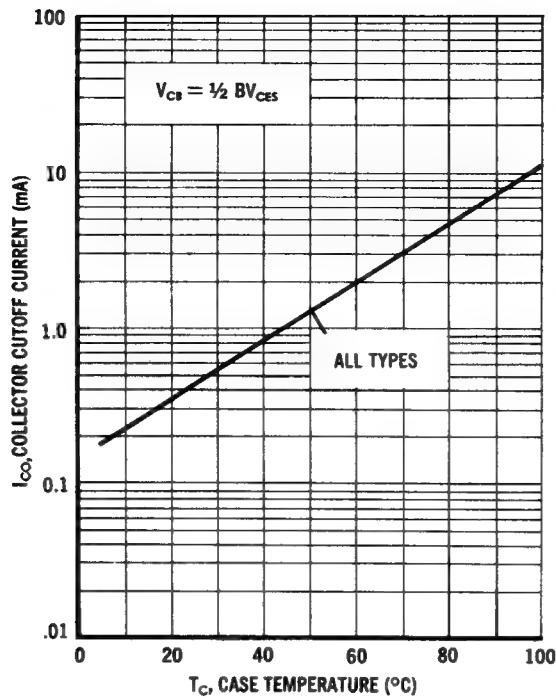
Fig. A.50 I_{CO} vs. temperature.
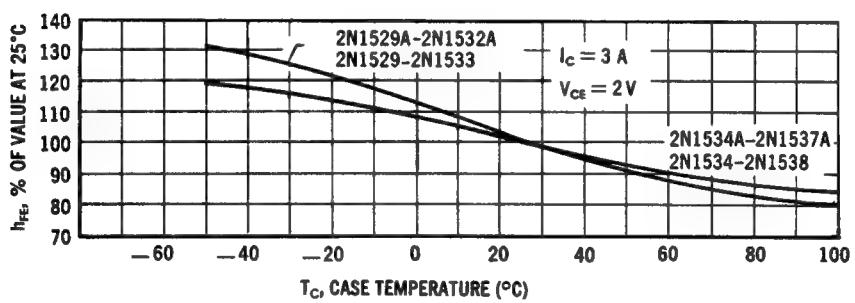
Fig. A.51 h_{FE} vs. temperature.
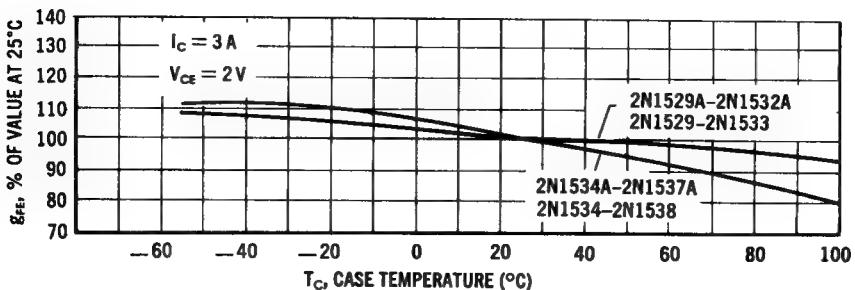
Fig. A.52 g_{FE} vs. temperature.

A.4b Determination of Allowable Peak Power

When a heat sink is used for increased heat transfer and greater thermal capacity, the following equation can be used to determine the allowable pulse power dissipation, designated as P_P. The allowable pulse power plus the steady state power, P_{SS}, gives the peak allowable power dissipation. Allowable pulse power is related by the following equation:

$$P_P = \frac{T_J - T_A - \theta_{JA} P_{SS}}{\theta_{JC}(1/C_P) + \theta_{CA}(t_1/t)}$$

where
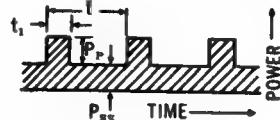
C_P = Coefficient of Power (from peak power derating curve),
T_J = Junction Temperature (°C),
T_A = Ambient Temperature (°C),
θ_{JC} = Junction-to-Case Thermal Resistance (°C/W),
θ_{CA} = Case-to-Ambient Thermal Resistance (°C/W),
$\theta_{JA} = \theta_{JC} + \theta_{CA}$,
(t_1/t) = Duty Cycle = Pulse Width / Pulse Period,
P_{SS} = Steady State Power Dissipation, and
P_P = Allowable Pulse Power Dissipation Above P_{SS}.
τ = Thermal Time Constant ≈ 50 msec

The peak power derating curve is normalized with respect to the thermal time constant, τ. The following example shows the application of this equation in conjunction with the peak power derating curve.

EXAMPLE:
Given:

$P_{SS} = 10$ W, $T_A = 40°C$, $t_1 = 1$ msec,
$(t_1/t) = 20\%$, $\theta_{CA} = 3°C/W$, $\theta_{JC} = 0.8°C/W$,
T_J max $= 100°C$

Solution:

Enter the derating graph at $t_1/\tau = 1$ msec/50 msec, and duty cycle of 20%. Find $C_P = 5$. Substitute this value and the given parameters into the peak pulse power equation. This gives $P_P = 29$ watts. Thus the peak allowable power is $P_P + P_{SS}$, or 39 watts.
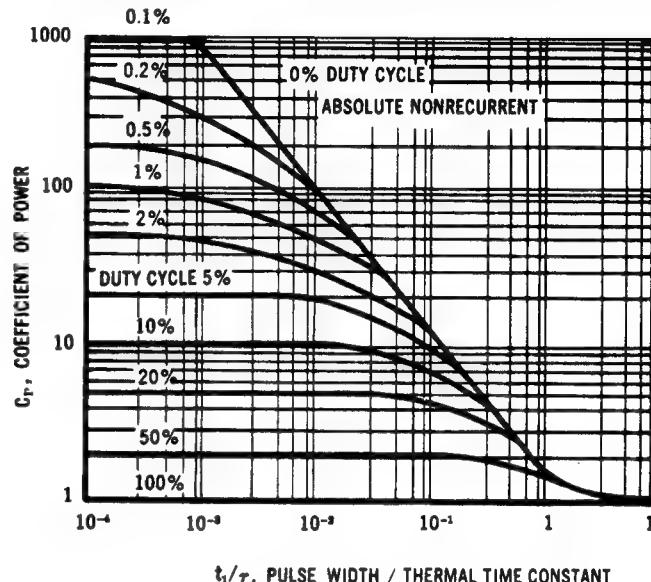

Fig. A.53 Pulse power derating curve. Caution: In all cases the peak pulse power should stay within the Safe Operating Area.

SUMMARY CHARTS

TABLE 3.1 Conversion from hybrid to hybrid-π parameters.

$$g_m = \frac{h_{fe}}{h_{ie} - r_{bb'}} \qquad [3.56]$$

$$r_{b'c} = \frac{h_{ie} - r_{bb'}}{h_{re}} \qquad [3.60]$$

$$r_{b'e} = \frac{h_{ie} - r_{bb'}}{1 - h_{re}} \cong h_{ie} - r_{bb'} \qquad [3.61]$$

$$\frac{1}{r_{ce}} = h_{oe} - h_{re} \frac{1 + h_{fe} - h_{re}}{h_{ie} - r_{bb'}} \cong h_{oe} \qquad [3.63]$$

(a) Common-emitter configuration.

(b) Hybrid equivalent circuit.

Hybrid	Common-base	Common-collector	Tee-equivalent
h_{ie}	$\dfrac{h_{ib}}{1 + h_{fb}}$	h_{ic}	$r_b + \dfrac{r_e}{1 - \alpha}$
h_{re}	$\dfrac{h_{ib}h_{ob}}{1 + h_{fb}} - h_{rb}$	$1 - h_{rc}$	$\dfrac{r_e}{(1 - \alpha)r_c}$
h_{fe}	$\dfrac{-h_{fb}}{1 + h_{fb}}$	$-(1 + h_{fc})$	$\dfrac{\alpha}{1 - \alpha}$
h_{oe}	$\dfrac{h_{ob}}{1 + h_{fb}}$	h_{oc}	$\dfrac{1}{(1 - \alpha)r_c}$

(c) Approximate parameter conversion formulae.

$$h_{ie} = 2200 \ \Omega$$
$$h_{re} = 2 \times 10^{-4}$$
$$h_{fe} = 290$$
$$h_{oe} = 30 \times 10^{-6} \ \text{mhos}$$

(d) Typical values for type 2N929 transistor at $I_C = 4$ ma, $V_{CE} = 12$ v.

Fig. 3.24 Conversion to common-emitter h-parameters.

* For convenience in reference, the original table numbers have been retained in this Appendix.

(a) Common-base configuration.

(b) Hybrid equivalent circuit.

Hybrid	Common-emitter	Common-collector	Tee-equivalent
h_{ib}	$\dfrac{h_{ie}}{1+h_{fe}}$	$-\dfrac{h_{ic}}{h_{fc}}$	$r_e + (1-\alpha)r_b$
h_{rb}	$\dfrac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$	$h_{rc} - 1 - \dfrac{h_{ic}h_{oc}}{h_{fc}}$	$\dfrac{r_b}{r_c}$
h_{fb}	$-\dfrac{h_{fe}}{1+h_{fe}}$	$-\dfrac{1+h_{fc}}{h_{fc}}$	$-\alpha$
h_{ob}	$\dfrac{h_{oe}}{1+h_{fe}}$	$-\dfrac{h_{oc}}{h_{fc}}$	$\dfrac{1}{r_c}$

(c) Approximate parameter conversion formulae.

$$h_{ib} = 7.57\ \Omega$$
$$h_{rb} = 0.268 \times 10^{-4}$$
$$h_{fb} = -0.996$$
$$h_{ob} = 0.103 \times 10^{-6}\ \text{mhos}$$

(d) Typical values for type 2N929 transistor.

Fig. 3.25 Conversion to common-base h-parameters.

(a) Common-collector configuration.

(b) Hybrid equivalent circuit.

Hybrid	Common-emitter	Common-base	Tee-equivalent
h_{ic}	h_{ie}	$\dfrac{h_{ib}}{1+h_{fb}}$	$r_b + \dfrac{r_e}{1-\alpha}$
h_{rc}	$1-h_{re} \cong 1$	$1-h_{rb} - \dfrac{h_{ib}h_{ob}}{1+h_{fb}} \cong 1$	$1 - \dfrac{r_e}{(1-\alpha)r_c} \cong 1$
h_{fc}	$-(1+h_{fe})$	$-\dfrac{1}{1+h_{fb}}$	$\dfrac{-1}{1-\alpha}$
h_{oc}	h_{oe}	$\dfrac{h_{ob}}{1+h_{fb}}$	$\dfrac{1}{(1-\alpha)r_c}$

(c) Approximate parameter conversion formulae.

$$h_{ic} = 2200\ \Omega$$
$$h_{rc} = 0.9999 \cong 1.0$$
$$h_{fc} = -291$$
$$h_{oc} = 30 \times 10^{-6}\ \text{mhos}$$

(d) Typical values for type 2N929 transistor.

Fig. 3.26 Conversion to common-collector h-parameters.

(a) Tee-equivalent circuit, common-base.

Circuit labels: αi_e, i_e, i_c, E, C, r_e, r_c, r_b, i_b, B

(b) Tee-equivalent circuit, common-emitter.

Circuit labels: $\frac{\alpha}{1-\alpha}i_b=\beta i_b$, i_b, r_b, i_c, B, C, r_e, $r_d=r_c(1-\alpha)=\frac{r_c}{1+\beta}$, i_e, E

Tee-parameter	Common-emitter	Common-base	Common-collector
α	$\dfrac{h_{fe}}{1+h_{fe}}$	$-h_{fb}$	$\dfrac{1+h_{fc}}{h_{fc}}$
r_c	$\dfrac{h_{fe}+1}{h_{oe}}$	$\dfrac{1-h_{rb}}{h_{ob}}$	$-\dfrac{h_{fc}}{h_{oc}}$
r_e	$\dfrac{h_{re}}{h_{oe}}$	$h_{ib}-(1+h_{fb})\dfrac{h_{rb}}{h_{ob}}$	$\dfrac{1-h_{rc}}{h_{oc}}$
r_b	$h_{ie}-\dfrac{h_{re}(1+h_{fe})}{h_{oe}}$	$\dfrac{h_{rb}}{h_{ob}}$	$h_{ic}+\dfrac{h_{fc}(1-h_{rc})}{h_{oc}}$
β	h_{fe}	$-\dfrac{h_{fb}}{1+h_{fb}}$	$-(1+h_{fc})$

(c) Approximate parameter conversion formulae.

$$\alpha = +0.996$$
$$r_c = 9.7\ \text{M}\Omega$$
$$r_e = 6.667\ \Omega$$
$$r_b = 260\ \Omega$$

(d) Typical values for type 2N929 transistor.

Fig. 3.27 Conversion to tee-parameters.

TABLE 5.1 Single-stage amplifier formulae.

	$R_i = \dfrac{v_i}{i_i}$	$R_o = \dfrac{v_o}{i_o}$	$A_i = \dfrac{i_o}{i_i}$	$A_v = \dfrac{v_o}{v_i}$
h-parameters (Second subscript omitted)	$h_i - \dfrac{h_f h_r}{\dfrac{1}{R_L}+h_o}$	$\dfrac{1}{h_o - \dfrac{h_f h_r}{h_i+R_g}}$	$\dfrac{h_f}{1+h_o R_L}$	$\dfrac{-R_L h_f}{h_i\left[1+R_L\left(h_o - \dfrac{h_f h_r}{h_i}\right)\right]}$
Common-base tee-equivalent circuit (see Fig. 2.31)	$r_e + r_b(1-\alpha) + r_b\dfrac{\alpha\frac{R_L}{r_c}+(1-\alpha)\frac{r_b}{r_c}}{1+\frac{R_L+r_b}{r_c}}$ $\cong r_e + r_b(1-\alpha)$, $\dfrac{r_b}{r_c}\ll\beta\quad \dfrac{R_L}{r_d}\ll1$	$r_c + r_b - \dfrac{\alpha r_c + r_b}{1+\frac{r_e+R_g}{r_b}}$	$\dfrac{\alpha+\frac{r_b}{r_c}}{1+\frac{r_b+R_L}{r_c}}\cong\alpha$, $\dfrac{r_b+R_L}{r_c}\ll1$	$\dfrac{\left(\alpha+\frac{r_b}{r_c}\right)R_L}{r_c\left(1+\frac{r_b+R_L}{r_c}\right)+r_b\left(1-\alpha+\frac{R_L}{r_c}\right)}$ $\cong\dfrac{\alpha R_L}{r_c+r_b\left(1-\alpha+\frac{R_L}{r_c}\right)}$, $\dfrac{r_b+R_L}{r_c}\ll1$
Common-emitter tee-equivalent circuit (see Fig. 2.31) Note: $r_e^*=r_e+R_E$; R_E = circuit resistance in emitter	$r_b+r_e^*(1+\beta)\dfrac{1+\frac{R_L}{r_d(1+\beta)}}{1+\frac{R_L+r_e^*}{r_d}}$ $\cong r_b+r_e^*(1+\beta)$, $R_L+r_e^*\ll r_d$	$r_d\left[1+\dfrac{r_e^*}{r_d}+\dfrac{\beta-\frac{r_e^*}{r_d}}{1+\frac{R_g+r_b}{r_e^*}}\right]$ $\cong r_d\left[1+\dfrac{\beta}{1+\frac{R_g+r_b}{r_e^*}}\right]$, $\dfrac{r_e^*}{r_d}\ll1$	$\dfrac{\beta-\frac{r_e^*}{r_d}}{1+\frac{R_L+r_e^*}{r_d}}$ $\cong\dfrac{\beta}{1+\frac{R_L}{r_d}}$, $r_e^*\ll r_d$	$\dfrac{R_L}{r_e^*}\times\dfrac{\frac{\beta}{\beta+1}-\frac{r_e^*}{r_d(\beta+1)}}{1+\frac{R_L}{r_d(\beta+1)}+\frac{r_b}{r_e^*(1+\beta)}\left(1+\frac{r_e^*+R_L}{r_d}\right)}$ $\cong-\dfrac{R_L}{r_e^*}$, $r_e^*\ll r_d$, $\beta\gg1$, $R_L\ll r_d$
Common-collector tee-equivalent circuit (see Fig. 2.31)	$r_b+\dfrac{(R_L+r_e)(\beta+1)}{1+\frac{(R_L+r_e)(\beta+1)}{r_c}}$ $\cong r_b+(R_L+r_e)(\beta+1)$, $r_c\gg(R_L+r_e)(\beta+1)$	$r_e+\dfrac{R_g+r_b}{1+\beta}\times\dfrac{1}{1+\frac{R_g+r_b}{r_d(1+\beta)}}$ $\cong r_e+\dfrac{R_g+r_b}{1+\beta}$, $R_g\ll r_c$	$(1+\beta)\dfrac{1}{1+\frac{r_e+R_L}{r_d}}$ $\cong1+\beta$, $r_e+R_L\ll r_d$	$\dfrac{1}{1+\frac{r_b}{r_c}+\left[r_e\left(1+\frac{r_b}{r_c}\right)+\frac{r_b}{1+\beta}\right]\frac{1}{R_L}}$ $\cong\dfrac{1}{1+\left(r_e+\frac{r_b}{1+\beta}\right)\frac{1}{R_L}}=\dfrac{1}{1+\frac{h_{ib}}{R_L}}$, $r_b\ll r_c$

TABLE 6.1 Type No. 2N930.

Electrical Parameters	$I_C = 13\,\mu a$	$I_C = 4$ ma	Unit
$h_{ib}^{\,*}$	2100	17	ohm
$h_{ob}^{\,*}$	0.045×10^{-6}	0.056×10^{-6}	mho
$h_{fe}^{\,*}$	200	370	
$h_{rb}^{\,*}$	1.5×10^{-4}	2.3×10^{-4}	
$h_{ic}^{\,**}$	420,000	6300	ohm
$h_{oc}^{\,**}$	9×10^{-6}	20.8×10^{-6}	mho
$h_{fc}^{\,**}$	-201	-371	
$h_{rc}^{\,**}$	1	1	

* Published data
** Derived data using conversion formulae of Chap. 3

TABLE 6.2 Type No. 2N930.

Electrical Parameters	$I_C = 1$ ma		$I_C = 2$ ma		$I_C = 3$ ma		Unit
	25°C	100°C	25°C	100°C	25°C	100°C	
h_{fe}	320	460	340	480	360	500	
h_{ib}	30	36	20	24	16	20	ohm
h_{ob}	0.076×10^{-6}	0.086×10^{-6}	0.11×10^{-6}	0.13×10^{-6}	0.15×10^{-6}	0.18×10^{-6}	mho
h_{rb}	1.8×10^{-4}	2.5×10^{-4}	2.0×10^{-4}	2.8×10^{-4}	2.2×10^{-4}	3.0×10^{-4}	
$r_c = 1/h_{ob}$	13.2×10^{6}	11.6×10^{6}	9.1×10^{6}	7.7×10^{6}	6.7×10^{6}	5.57×10^{6}	ohm
$h_{ic} = h_{ib}(1 + h_{fe})$	9630	16,650	6820	11,600	5780	10,000	ohm
$h_{oc} = h_{ob}(1 + h_{fe})$	24.4×10^{-6}	39.6×10^{-6}	37.4×10^{-6}	62.5×10^{-6}	54×10^{-6}	90.5×10^{-6}	mho
$h_{re} = h_{ib}h_{ob}(1 + h_{fe}) - h_{rb}$	5.5×10^{-4}	11.7×10^{-4}	5.5×10^{-4}	12.2×10^{-4}	6.4×10^{-4}	15×10^{-4}	
$r_b = h_{ie} - r_e(1 + h_{fe})$	2230	2750	1710	2450	1330	1500	ohm
$r_e = h_{re}/h_{oe}$	23	30	15	19	12	17	ohm

TABLE 7.1 Class A amplifier design formulae.*

Item	Formula $(R_T \neq 0)$	Formula $(R_T = 0)$	
$P_{o_{max}}$	$\dfrac{BV_{max} I_Q}{4} - \dfrac{R_T I_Q^2}{2}$	$\dfrac{P_C}{2}$	(7.10a)
$P_{CE_{max}}$	$V_{CC} I_Q = P_C$	P_C	(7.10b)
V_{CC}	$\dfrac{BV_{max} + 2R_T I_Q}{2}$	$\dfrac{BV_{max}}{2}$	(7.10c)
η_{max}	$0.5\,\dfrac{R_L'}{R_L' + 2R_T}$	0.5	(7.10d)
R_L'	$\dfrac{BV_{max}}{2I_Q} - R_T$	$\dfrac{BV_{max}^2}{4P_C}$	(7.10e)
$\dfrac{P_{o_{max}}}{P_{CE_{max}}}$		0.5	(7.10f)
$I_{Q\,(opt)}$	$\dfrac{BV_{max}}{4R_T}\left[\sqrt{1 + \dfrac{16 P_C R_T}{BV_{max}^2}} - 1\right]$	$I_Q = \dfrac{2P_C}{BV_{max}}$	(7.10g)
$P_{cc_{max}}$	$V_{CC} I_Q = P_C$	$V_{CC} I_Q = P_C$	(7.10h)
I_{max}	$2I_Q$	$2I_Q$	(7.10i)

*Transformer coupling to load assumed.

TABLE 7.3 Measured parameters on a 2N930 transistor.

$I_{C\,(ma)}$	$T_J = 175°C$		$T_J = 25°C$	$T_J = 175°C$
	h_{fe}	$I_{B\,(\mu a)}$	V_{BE} (v)	V_{BE} (v)
1	460	2.2	0.515	0.215
2	490	4.1	0.54	0.24
5	500	10	0.56	0.26
10	490	20	0.58	0.28
20	425	47	0.61	0.31
30	380	79	0.635	0.335
40	335	120	0.655	0.355
50	310	161	0.67	0.370
60	290	206	0.68	0.38
70	250	240	0.695	0.395

TABLE 7.2 Class B push-pull amplifier, design formulae.

Item	Formula $(R_T \neq 0)$	Formula $(R_T = 0)$	
$P_{o_{max}}$	$\dfrac{V_{CC}^2 R_L'}{4(R_T + R_L')^2}$	$\dfrac{V_{CC}^2}{4R_L'}$	(7.12a)
$P_{CE_{max}}$	$\dfrac{V_{CC}^2}{\pi^2 R_L'}$	$\dfrac{V_{CC}^2}{\pi^2 R_L'}$	(7.12b)
η_{max}	$\dfrac{\pi}{4} \dfrac{R_L'}{R_T + R_L'}$	0.785	(7.12c)
R_L'	$\dfrac{V_{CC}^2}{\pi^2 P_C}$	$\dfrac{V_{CC}^2}{\pi^2 P_C}$	(7.12d)
$\dfrac{P_{o_{max}}}{P_{CE_{max}}}$	$\dfrac{\pi^2}{4}\left(\dfrac{R_L'}{R_T + R_L'}\right)^2$	$\dfrac{\pi^2}{4} = 2.466$	(7.12e)
V_{CC}	$2V_{CC}^3 - BV_{max}V_{CC}^2 + \pi^2 P_C R_T V_{CC}$ $= BV_{max} P_C R_T \pi^2$	$V_{CC} = \dfrac{BV_{max}}{2}$	(7.12f)
$P_{CC_{max}}$	$\dfrac{V_{CC}^2}{\pi(R_T + R_L')}$	$\dfrac{V_{CC}^2}{\pi R_L'}$	(7.12g)
For $I_C = kI_{C_{max}}$, $k < 1$			
P_{CC}		$\dfrac{kV_{CC}^2}{\pi R_L'}$ (per transistor)	(7.12h)
η		$\dfrac{k\pi}{4}$	(7.12i)
P_o		$\dfrac{k^2 V_{CC}^2}{4R_L'}$ (per transistor)	(7.12j)
I_{max}	$\dfrac{V_{CC}}{R_T + R_L'}$	$\dfrac{V_{CC}}{R_L'}$	(7.12k)

FREQUENCY RESPONSE PLOTTING

C | APPENDIX

C.1 Introduction

The frequency response of networks used in transistor amplifiers can be represented by the product of a constant term, and frequency sensitive terms of the form listed below:

$$j\omega T, \qquad \frac{1}{j\omega T},$$

$$1 + j\omega T, \qquad \frac{1}{1 + j\omega T},$$

$$\omega^2 T^2 + 2j\zeta\omega T + 1, \qquad \frac{1}{\omega^2 T^2 + 2j\zeta\omega T + 1}.$$

This limitation on the realizable form of practical transfer functions leads to a quick method of plotting those transfer functions. The key is to use logarithmic coordinates, i.e., logarithm of gain vs. logarithm of frequency. On these coordinates, the transfer functions are very accurately described by straight line asymptotes. Phase angle in linear coordinates is normally plotted versus the same log frequency as the gain function.

C.2 The Asymptotic Plot

The utility of logarithmic coordinates is based on the elementary fact that the logarithm of a product of terms is the sum of the logarithms of the individual terms. Thus, the logarithm of the gain of a complex transfer function is the sum of the logarithms of the component terms. Since the variety of component terms is very limited, as listed in C.1, the basis for rapid sketching of the gain function is established.

The logarithmic gain is conventionally expressed in db, where

$$\text{gain (db)} = 20 \log_{10} (\text{gain}).$$

Thus, a gain of 2 corresponds to 6 db; a gain of 10 corresponds to 20 db. Attenuation is expressed as negative db. For example, an attenuation of $\frac{1}{2}$ is expressed as −6 db.

The asymptotic plotting technique is based on the surprisingly excellent correspondence between limiting asymptotes and the actual frequency response curve when plotted on logarithmic coordinates.

Elaboration on the actual plotting techniques is carried out by means of a series of problems, gradually increasing in complexity. Asymptotic gain is plotted

on logarithmic coordinates, while phase shift is plotted on *linear* coordinates versus log frequency.

Note how asymptotes are determined in the following examples, by taking the simplified forms of the transfer functions for extreme conditions.

PROBLEM C.1   Plot the following transfer function on logarithmic coordinates:

$$G(j\omega) = \frac{10}{j\omega(1 + j\omega/10)} .$$ (C.1)

Solution: At very low frequency,

$$|G(j\omega)| \approx \left| \frac{10}{j\omega} \right| .$$

Express gain in decibels for the low frequency region:

$$db = 20 \log_{10} \frac{10}{\omega} = 20[\log_{10} 10 - \log_{10} \omega]$$

$$= 20 [1 - \log_{10} \omega] .$$ (C.2)

Note that if db is plotted versus $\log_{10} \omega$, the resulting curve will be a *straight line* as in Fig. C.1a (dashed line).   This line crosses the zero db axis at $\omega = 10$, since at that point, (C.2) = 0.   The line is an approximation to the actual frequency-response curve only at very low frequencies.
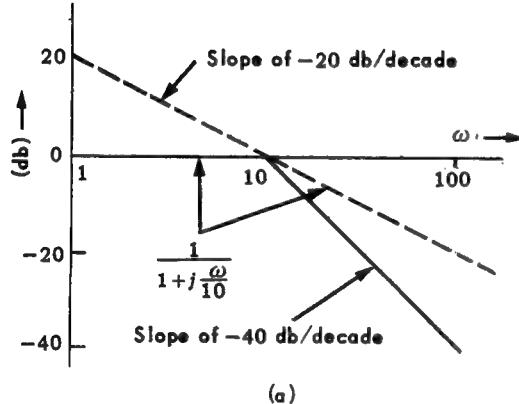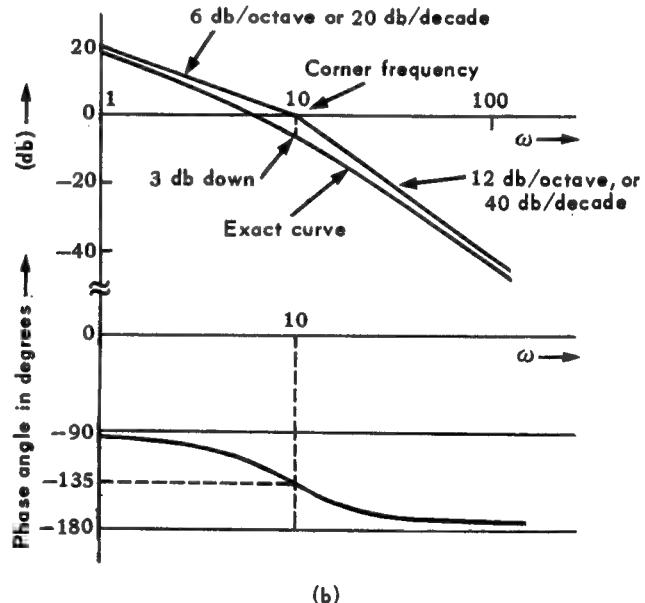
Fig. C.1 (a) Separate Bode components which are combined to obtain the resultant diagram of Fig. C.1(b).
(b) Bode plot of the transfer function $G(j\omega) = \dfrac{10}{j\omega \left(1 + j \dfrac{\omega}{10} \right)} .$

Now consider the very high frequency region where $\dfrac{\omega}{10} \gg 1.$ In this region,

$$|G(j\omega)| \approx \left| \frac{10}{(j\omega)^2 \left(\dfrac{1}{10} \right)} \right| = \frac{100}{\omega^2} .$$ (C.3)

Express gain in decibels:

$$db = 20 \log_{10} \frac{100}{\omega^2} = 20 \left[\log_{10} 100 - \log_{10} \omega^2 \right]$$

$$= 20 \left[2 - 2 \log_{10} \omega \right]$$

$$= 40 \left[1 - \log_{10} \omega \right] . \tag{C.4}$$

This is again a straight line; i.e., db is a linear function of $\log_{10} \omega$. This line crosses the zero db axis where $\log_{10} \omega = 1$, or at $\omega = 10$, by coincidence, at the same point where the low-frequency approximation curve crosses the zero db axis. Note that the slope (-40) of (C.4) is twice the slope (-20) of (C.2).

Figure C.1b shows the superposition of the straight line approximations to the very low- and very high-frequency regions of the $|G(j\omega)|$ curve, as well as the actual curve. As frequency reduces or increases indefinitely, the curve $|G(j\omega)|$ approaches the straight lines asymptotically. Hence, this type of diagram is often called an *asymptotic diagram*. Practically, the degree of approximation represented by the two asymptotic portions to the left and right of their common intersection point, is remarkably good. The excellence of the straight line approximation to the actual curve is the key reason for the widespread use of this type of diagram. Figure C.1b also shows the plot of the phase angle plotted on the same frequency scale.

PROBLEM C.2 For the transfer function of Prob. C.1 with generalized gain and time constant, calculate the gain error at the intersection of the two asymptotes.

Solution: Consider the mathematical expression for $|G(j\omega)|$. Use K and T instead of the numerical values of the previous example. We have

$$G(j\omega) = \frac{K}{j\omega(1 + j\omega T)},$$

$$|G(j\omega)| = \frac{K}{\omega \sqrt{1 + \omega^2 T^2}} .$$

When $\omega T \gg 1$ (high frequency) or when $\omega T \ll 1$ (low frequency), the approximation method applies with high accuracy. Where $\omega T = 1$, the approximation is poorest. Here, the asymptotic diagram indicates a value (at the intersection of the two asymptotes) of $20 \log_{10} KT$. The exact value is

$$|G(j\omega)| = \frac{KT}{\omega T \sqrt{1 + (\omega T)^2}} = \frac{KT}{1 \sqrt{1 + 1}} = \frac{KT}{\sqrt{2}}$$

or

$$db = 20 \log_{10} \frac{KT}{\sqrt{2}} = \underbrace{20 \log_{10} KT}_{\substack{\text{approximate} \\ \text{value}}} - \underbrace{20 \log_{10} \sqrt{2}}_{\text{error}} ,$$

so that

$$\text{error (db)} = -20 \log_{10} \sqrt{2} = -10 \log_{10} 2 = -10(0.301) = -3.01 \text{ db}.$$

At this poorest point, the actual curve is very close to 3 db below the value indicated by the asymptotes.

There are other interesting points to note from the asymptotic curve of Fig. C.1b. Observe the slopes of the two straight line sections:

Low-frequency slope = -20

High-frequency slope = -40

Suppose we let frequency $\omega_2 = 2\omega_1$, a one octave range, and determine the change in decibels over this octave for the two slopes. Therefore, the changes at the low- and high-frequency slopes are, respectively,

$$-20 \log_{10} \frac{\omega_2}{\omega_1} = -20 \log_{10} 2 = -6.02 \text{ db},$$

$$-40 \log_{10} \frac{\omega_2}{\omega_1} = -40 \log_{10} 2 = -12.04 \text{ db}.$$

The slopes of the straight line approximations are 6 db/octave and 12 db/octave, respectively, for the low-frequency and high-frequency regions. For a decade band, $\omega_2/\omega_1 = 10$, $\log_{10} \omega_2/\omega_1 = 1$, and the slopes become 20 db/decade and 40 db/decade, respectively.

Therefore,

$$6 \text{ db/octave} = 20 \text{ db/decade}, \tag{C.5}$$

$$12 \text{ db/octave} = 40 \text{ db/decade}. \tag{C.6}$$

Six db/octave means that gain is changed by a factor of two for a doubling of frequency. Twelve db/octave means that gain is changed by a factor of four for a doubling of frequency.

With respect to plotting phase angle, the method is more sophisticated than the one for amplitude. However, it is simple enough for practical purposes. Consider the phase shift at very low frequency of the function of (C.1). The approximate low frequency expression is

$$G(j\omega) = \frac{K}{j\omega},$$

which corresponds to a 90° phase lag. The high-frequency approximation

$$G(j\omega) = \frac{K}{(j\omega)^2 T}$$

indicates a phase lag of 180°. The phase shift versus frequency curve is plotted in Fig. C.1b. At extreme frequencies, actual phase shift approaches these asymptotic values. At $\omega T = 1$, phase shift may be found directly from the transfer function (C.1). Thus,

$$G(j\omega) = \frac{K}{j\omega(1 + j\omega T)} = \frac{KT}{j(1 + j)} = \frac{KT}{1\angle 90° \sqrt{2} \angle 45°}.$$

At $\omega T = 1$, phase lag is 135°, as shown by Fig. C.1b. The phase angle can be estimated directly from the asymptotic gain diagram by applying the following rules:

When asymptotic slope is 0 db/octave, phase angle approaches 0°.
When asymptotic slope is ± 6 db/octave, phase angle approaches ±90°.
When asymptotic slope is ± 12 db/octave, phase angle approaches ±180°.
When asymptotic slope is ± 6n db/octave, phase angle approaches ± $n\pi/2$, where $n = 1, 2, 3, 4, \ldots$.

By means of these rules, combined with an actual calculation of phase angle at certain critical points, phase angle curves are easily plotted.

PROBLEM C.3 Plot the gain and phase characteristic of $\dfrac{K}{1 + j\omega T}$ where $K = 10$.

Solution: Refer to Fig. C.2. At low frequency, the asymptote is simply K, a horizontal line whose ordinate is given as

$$db = 20 \log_{10} K.$$

At high frequency, $|G(j\omega)| = K/\omega T$, which intersects the low–frequency asymptote at $\omega T = 1$, or $\omega = 1/T$. The slope at high frequency falls off at 20 db/decade, since the high-frequency slope has ω to the first power only in the denominator. The low-frequency phase shift is approximately zero, approaching a 90° lag at very high-frequency. At $\omega T = 1$, phase lag may be calculated from

$$G(j\omega) = \frac{K}{1 + j} \; ;$$

hence, phase lag $= 45°$.
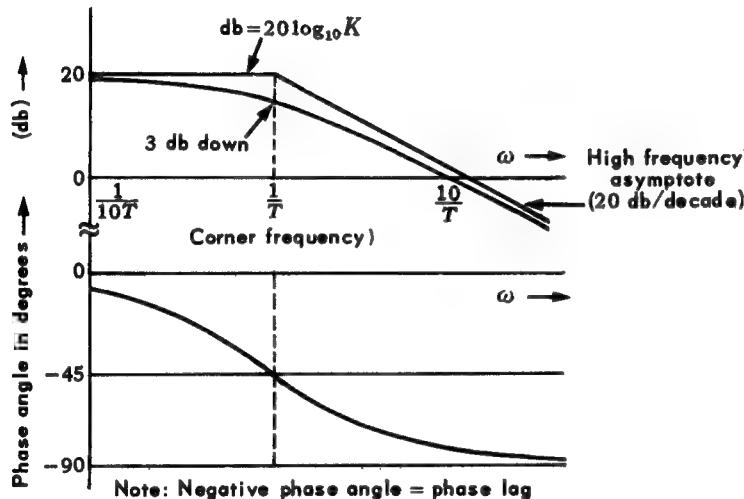
Fig. C.2 Plot on Bode coordinates.
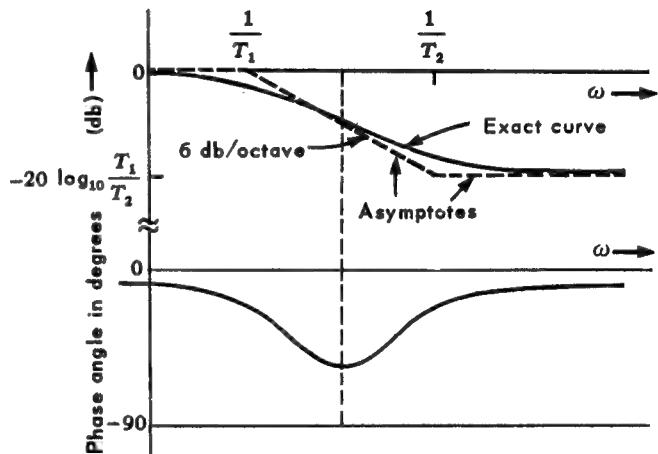
Fig. C.3 Bode plot of transfer function. Note that the phase moves toward $-90°$ and then returns to its $0°$ asymptote.

PROBLEM C.4 Sketch the asymptotic diagram and the approximate phase characteristic of the following transfer function:

$$G(j\omega) = \frac{1 + j\omega T_2}{1 + j\omega T_1} , \qquad T_1 > T_2 .$$

Solution: Refer to Fig. C.3.

PROBLEM C.5 Sketch the asymptotic diagram and the approximate phase characteristic of the following transfer function:

$$G(j\omega) = \frac{1 + j\omega T_1}{1 + j\omega T_2} , \qquad T_1 > T_2 .$$

Solution: Refer to Fig. C.4.
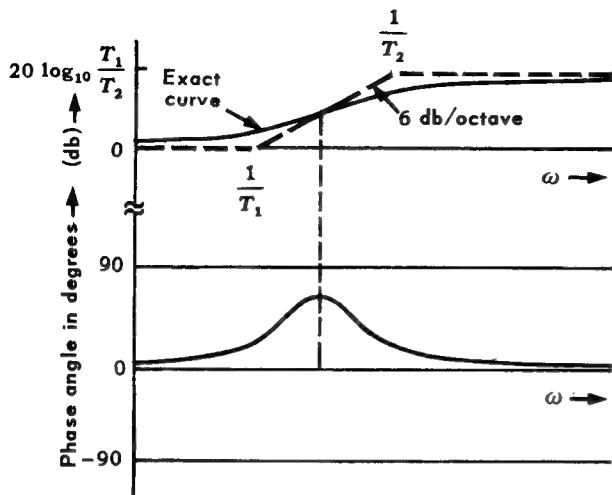
Fig. C.4 Bode plot of transfer function. Note that the phase moves toward $+90°$ and then returns to its $0°$ asymptote.
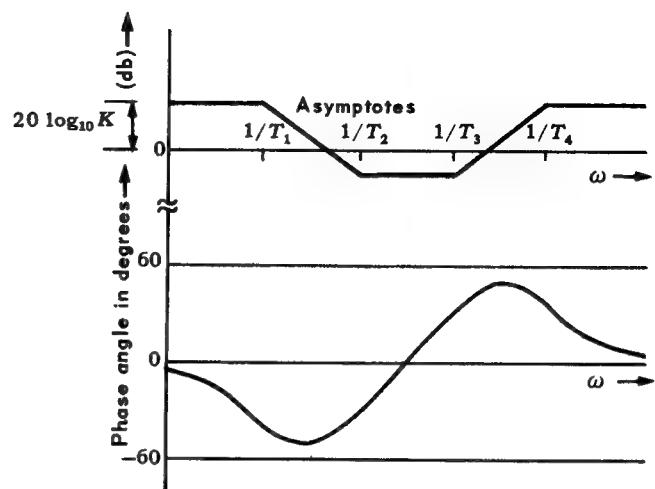
Fig. C.5 Bode plot of transfer function. Note relative complexity of phase diagram.

PROBLEM C.6   Sketch the asymptotic diagram and the approximate phase characteristic of the following transfer function:

$$G(j\omega) = K\ \frac{(1 + j\omega T_2)(1 + j\omega T_3)}{(1 + j\omega T_1)(1 + j\omega T_4)}\ ,\qquad T_1 > T_2 > T_3 > T_4\ .$$

Solution: Refer to Fig. C.5.

PROBLEM C.7   Sketch the asymptotic diagram and the approximate phase characteristic of the following transfer function:

$$G(j\omega) = \frac{K}{(1 + j\omega T_1)(1 + j\omega T_2)}\ ,\qquad T_1 > T_2\ .$$

Solution: Refer to Fig. C.6.
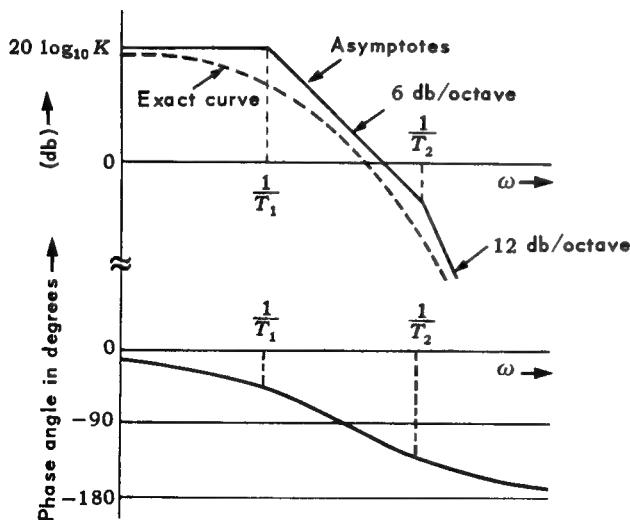
Fig. C.6 Bode plot of transfer function.
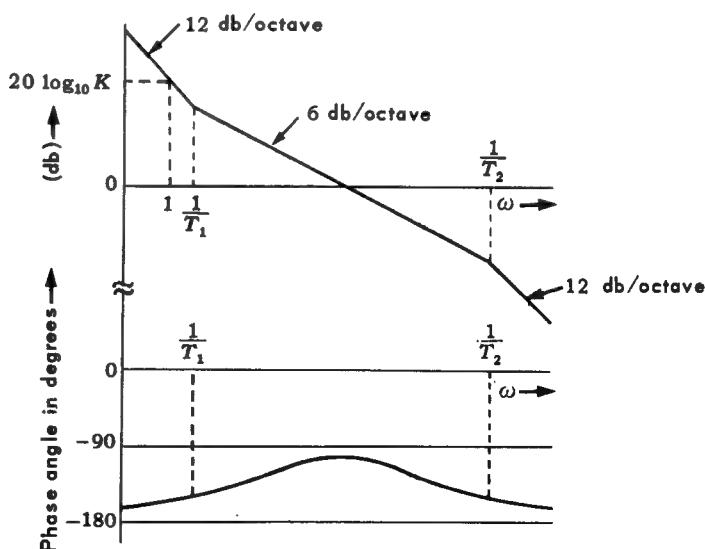
Fig. C.7 Bode plot of transfer function.

PROBLEM C.8   Sketch the asymptotic diagram and the approximate phase char-

acteristic of the following transfer function:

$$G(j\omega) = \frac{K(1 + j\omega T_1)}{(j\omega)^2(1 + j\omega T_2)}, \qquad T_1 > T_2 .$$

Solution: Refer to Fig. C.7.

C.3 More Complex Frequency-Response Functions

The most general frequency-response functions encountered in elementary servomechanisms may be represented by proper fractions of the form

$$G(j\omega) = \frac{KA(j\omega)}{(j\omega)^n B(j\omega)} .$$

The $A(j\omega)$ and $B(j\omega)$ are polynomials with real coefficients which may be factored into the product of linear and quadratic expressions of the following forms:

Linear factors, $1 + j\omega T$;

Quadratic factors, $-\omega^2 T^2 + 2\zeta j\omega T + 1$.

The quadratic factors have complex zeros. The values of ζ and T are dependent on the numerical values of the parameters. In general, transfer functions consist of combinations of terms of these types, with the degree of the denominator exceeding the degree of the numerator. Typical forms taken by these functions are listed below:

$$G_1(j\omega) = \frac{1 + j\omega T_2}{(1 + j\omega T_1)(1 + j\omega T_3)}, \qquad G_2(j\omega) = \frac{(1 + j\omega T_1)}{j\omega(1 + j\omega T_2)(1 + j\omega T_3)}$$

$$G_3(j\omega) = \frac{1}{(-\omega^2 T^2 + 1) + j2\zeta\omega T_3}, \qquad G_4(j\omega) = \frac{1 + j\omega T_1}{-\omega^2(1 + j\omega T_2)}$$

$$G_5(j\omega) = \frac{(1 + j\omega T_1)}{[(-\omega^2 T^2 + 1) + j2\zeta T\omega][1 + j\omega T_2]}, \qquad G_6(j\omega) = \frac{(1 + j\omega T_1)(1 + j\omega T_4)}{(1 + j\omega T_2)(1 + j\omega T_3)}.$$

PROBLEM C.9 Plot the Bode diagram of a quadratic function, using the standard expression

$$G(j\omega) = \frac{1}{-\omega^2 T^2 + 2\zeta j\omega T + 1} . \tag{C.7}$$

Solution: As before, determine asymptotes for low and high frequencies. At low frequency, $|G(j\omega)| = 1$ with zero phase shift. This corresponds to

$$db = 20 \log_{10} 1 = 0 .$$

The low frequency gain is thus zero db. At very high frequency,

$$|G(j\omega)| = \left|\frac{1}{-\omega^2 T^2}\right| \quad \text{with } 180° \text{ phase shift} .$$

Converting gain at high frequency to db,

$$db = -20 \log_{10} \omega^2 T^2 = -40 \log_{10} \omega T .$$

This expression, plotted on suitable coordinates, is a straight line with a negative slope of 40 db/decade (corresponding to 12 db/octave), with phase shift
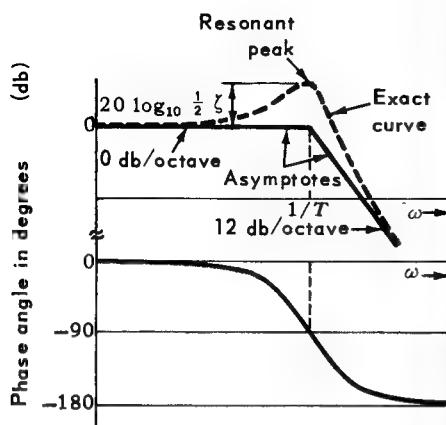
Fig. C.8 Bode plot of quadratic function.

approaching 180° at very high frequencies. This straight line asymptote intersects the zero db axis where $-40 \log_{10} \omega T = 0$, or $\omega T = 1$. Thus, a quadratic expression of the form of (C.7) has two asymptotes, the same as for a linear expression, except that at the intersection point of the asymptotes (the corner frequency), the slope of the asymptotes changes by 40 db/decade.

Consider now the region in the vicinity of the corner frequency, where the asymptotic approximation is apt to be least accurate. In (C.7), let $\omega T = 1$. Then

$$G(j\omega) = \frac{1}{2\zeta j\omega T} = \frac{1}{2\zeta j}. \qquad (C.8)$$

This expression indicates a gain of $1/2\zeta$ and a phase lag of 90°. Plotting the high and low frequency asymptotes, the exact corner frequency point, and sketching in phase shift, the approximate gain curve of Fig. C.8 is quickly drawn. The damping factor ζ for the quadratic expression is exactly the same as the one for the simple second order servo whose characteristic equation is also a quadratic. A zero damping factor means infinite amplitude at the corner or "resonant" frequency. Heavy damping eliminates the resonant peak. A damping factor greater than unity means that the quadratic expression may be factored into two linear expressions which can be plotted by methods previously described. Amplitude and gain functions of the quadratic plotted versus dimensionless frequency ωT as a function of the parameter ζ, are shown by Figs. C.9 and C.10, respectively.
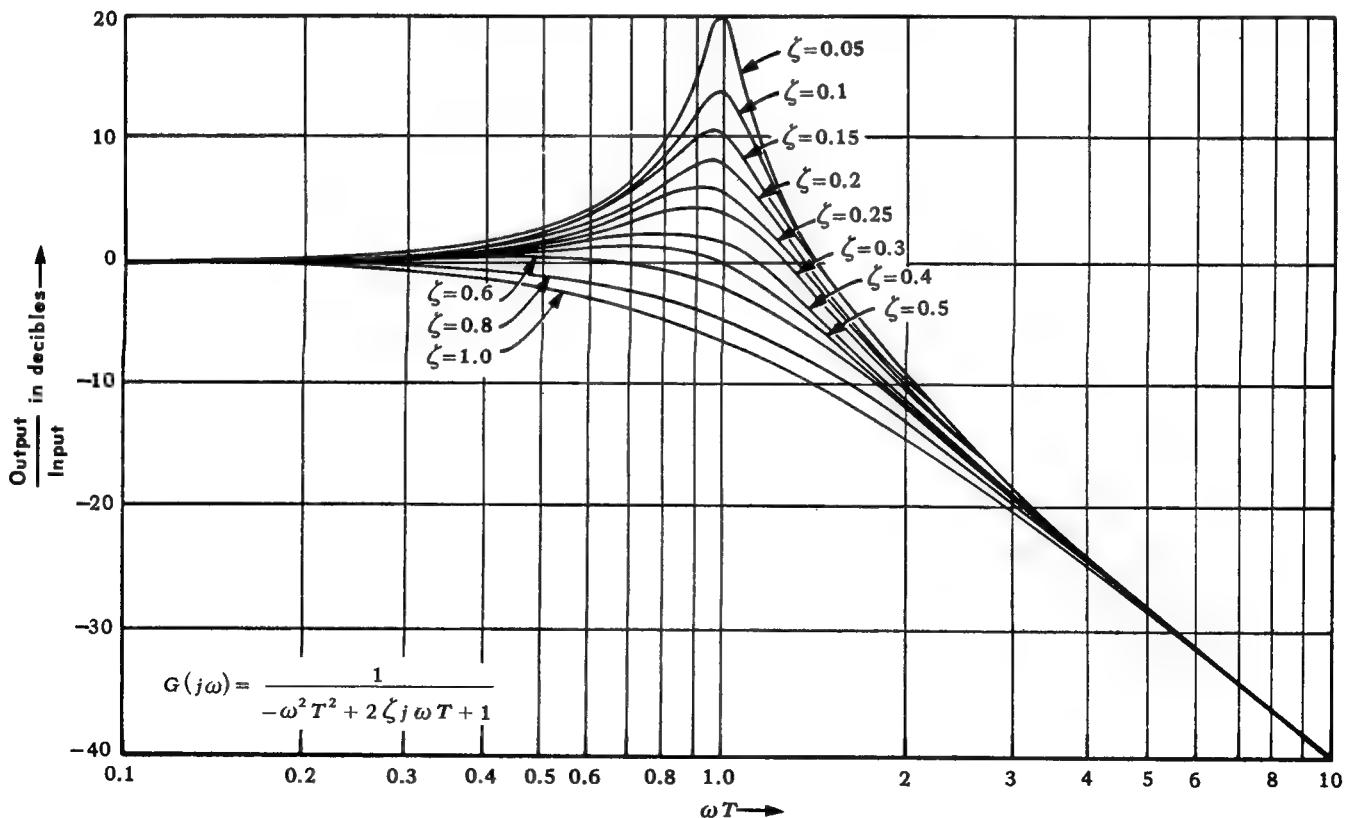
Fig. C.9 Magnitude of output/input versus dimensionless frequency ωT for various values of ζ.
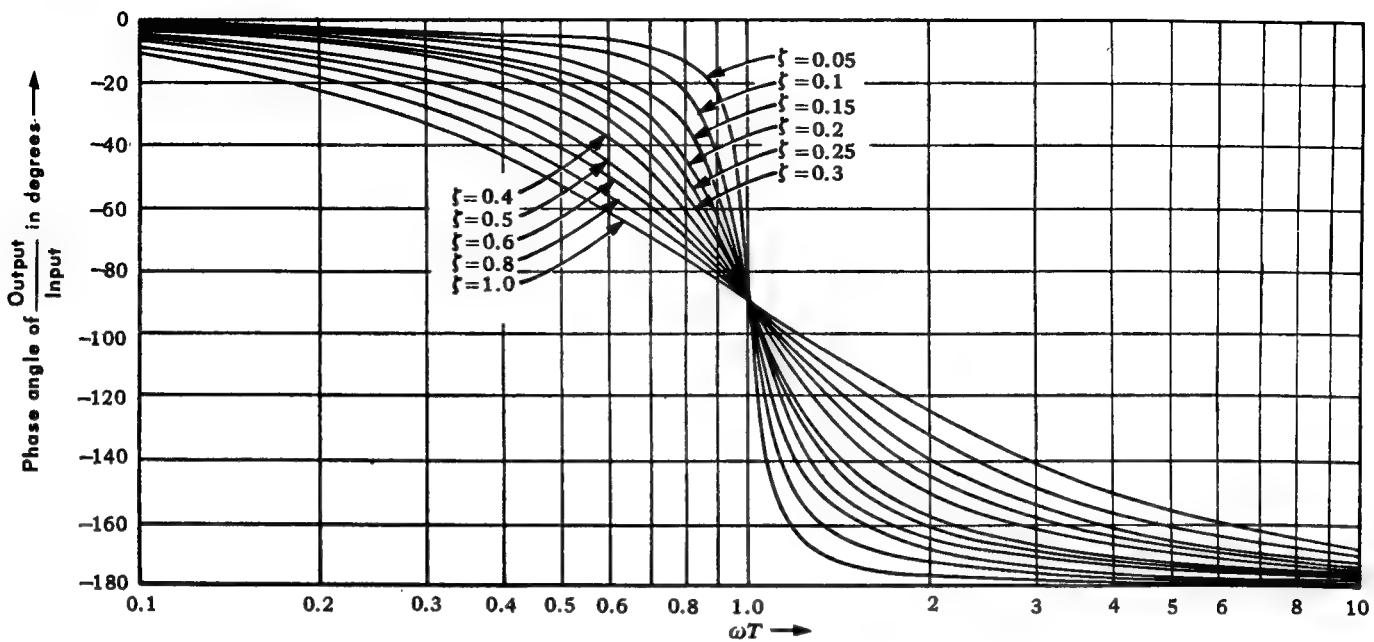
Fig. C.10 Phase shift of output/input versus dimensionless frequency ωT for various values of ζ.

PROBLEM C.10   Sketch the Bode diagram of the expression

$$G(j\omega) = \frac{1}{-\omega^2 T^2 + j\omega T + 1} \ . \qquad (C.9)$$

Solution: Compare the middle term of the denominator with the standard form $2\zeta j\omega T$, $2\zeta = 1$ or $\zeta = \frac{1}{2}$.   Refer to the $\zeta = \frac{1}{2}$ of Fig. C.9.   Note that gain is 0 db at $\omega T = 1$ for this damping factor.   Figure C.10 shows the companion phase shift curve.

Consider now the plotting of transfer functions containing linear and quadratic factors.   This may be carried out in a routine manner by remembering that the contributions of each factor of the gain function may be added, since a multiplying factor becomes an additive term when using logarithmic (decibel) units. Phase shifts are, of course, directly additive.

PROBLEM C.11   Plot the gain and phase characteristics on Bode coordinates of the transfer function

$$G(j\omega) = \frac{K}{(1 + j\omega T_1)(1 + j\omega T_2)} \ , \qquad T_1 > T_2 \ . \qquad (C.10)$$

Solution: Proceeding as before to determine the gain characteristic,

$$|G(j\omega)| = \frac{K}{|1 + j\omega T_1||1 + j\omega T_2|} \ .$$

Expressed in db:

$$db = 20 \log_{10} \left(\frac{K}{|1 + j\omega T_1||1 + j\omega T_2|} \right)$$

$$= 20 (\log_{10} K - \log_{10} |1 + j\omega T_1| - \log_{10} |1 + j\omega T_2|) . \qquad (C.11)$$

Note that each factor in the transfer function makes its separate contribution to

the decibels of attenuation, and in plotting the asymptotic diagram, each term may be considered separately. Thus, as shown by Fig. C.11a, the separate asymptotic contributions of each term are drawn to provide an asymptotic or straight line approximation to the entire curve of Fig. C.11b. This approximation is at its best in regions far from the corner frequencies. Similarly, each term of the transfer function contributes its phase shift component, which may be added, as shown by Fig. C.11c.
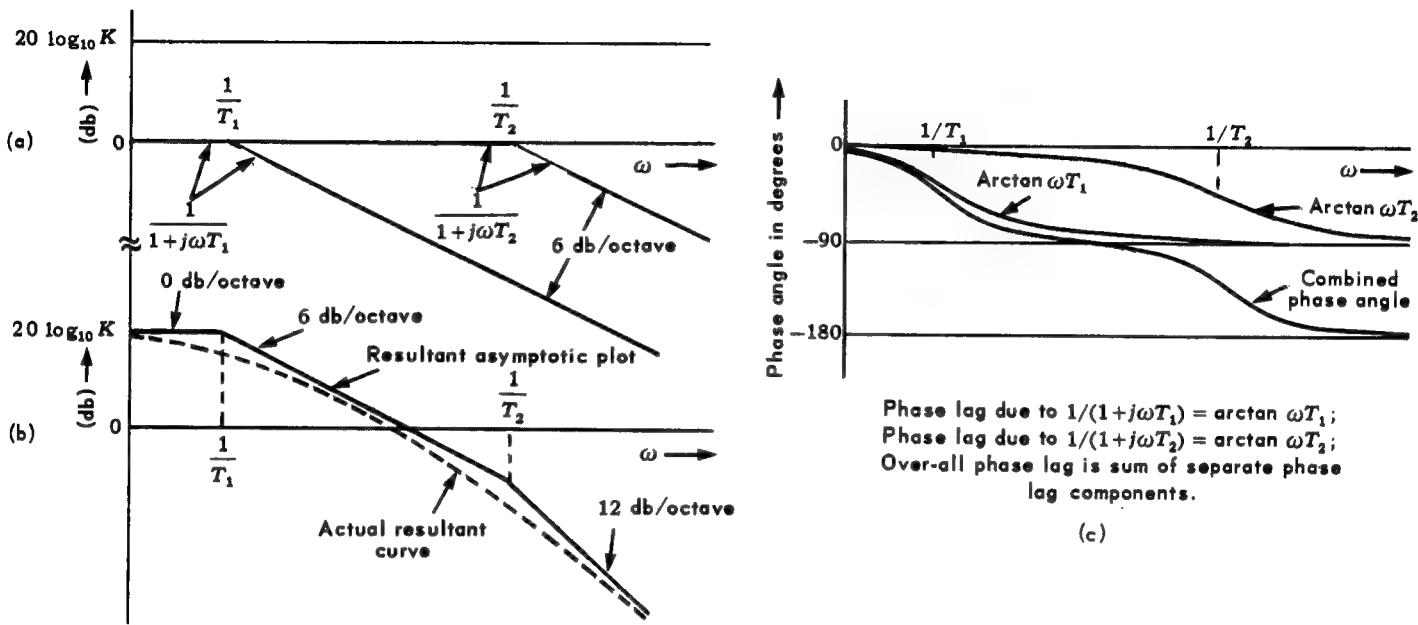
Fig. C.11 (a-b) Bode plot showing how components of asymptotic diagram are added to develop over-all diagram.
(c) Bode plot showing how separate phase lags of transfer function are added together.

Note in Figs. C.11a-c that corner frequencies for the resultant asymptotic curve occur at $\omega = 1/T_1$, and $\omega = 1/T_2$. Note further that each successive corner frequency marks the point where the corresponding term of the denominator starts to increase rapidly with frequency, resulting in a sharper slope of the asymptotic line following the corner point. The phase shift curve tends toward the values corresponding to the gain asymptote slopes; i.e., 90° for 6 db/octave, 180° for 12 db/octave, etc. The phase shift curves tend toward these values only when corner frequencies are widely separated. When the corners are less than a few octaves apart, the limiting phase shift values constitute only a crude guide. A more accurate plot would require calculating the exact phase shift at a few well chosen points. Since the corner frequencies represent points of poorest approximation, it is particularly convenient to calculate phase shift at these corners. In practical cases, phase shift is important in limited regions where exact calculations may be made once the approximate phase curve is known.

PROBLEM C.12   Plot the Bode curves for the function

$$G(j\omega) = \frac{K(1 + j\omega T_1)}{j\omega\,(1 + j\omega T_2)}\;, \qquad T_1 > T_2\;. \tag{C.12}$$

Solution: Refer to Fig. C.12. At very low frequency,

$$G(j\omega) = \frac{K}{j\omega}\;, \qquad |G(j\omega)| = \frac{K}{\omega}\;.$$

This curve, or an extension thereof, crosses the zero db axis at $\omega = K$. At $\omega = 1$, db $= 20 \log_{10} K$. This straight line extends indefinitely to the left (toward $\omega = 0$,

on the logarithmic scale). Phase shift at very low frequency tends toward 90° lagging. At $\omega = 1/T_1$, the term in the numerator starts to increase substantially in magnitude, thereby introducing a leading phase shift component. The increase in ωT_1 starts to balance the increase in the ω of the denominator (ωT_2 still much less than unity), so that the gain curve flattens out. The $(1 + j\omega T_1)$ factor in the numerator creates a positive slope change of 20 db/decade to balance the initial negative slope of 20 db/decade. At $\omega = 1/T_2$, the second denominator factor introduces a second corner frequency, adding a 20 db/decade negative slope to the asymptotic gain curve. Phase shift tends toward the values corresponding to the different slopes between the corner frequencies.
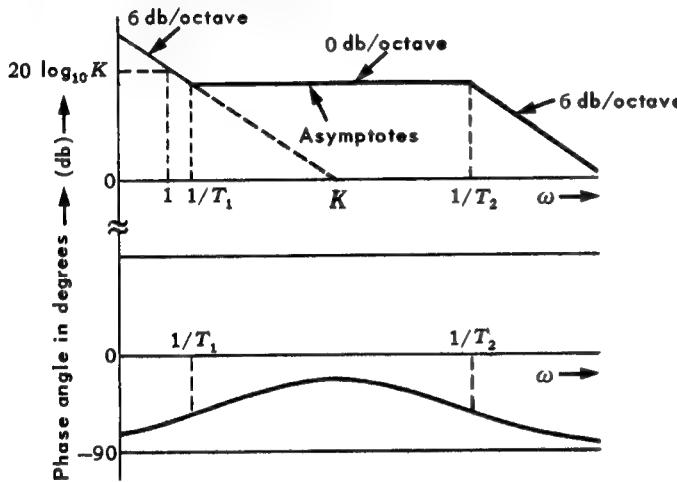
Fig. C.12 Bode plot of transfer function.
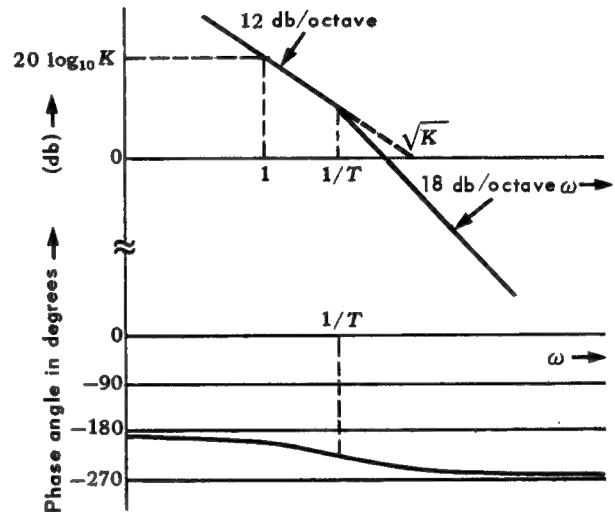
Fig. C.13 Bode plot of transfer function.

PROBLEM C.13 Plot the Bode diagram of the transfer function

$$G(j\omega) = \frac{K}{(j\omega)^2(1 + j\omega T)}.$$ (C.13)

Solution: Refer to Fig. C.13. The gain curve has a single corner frequency at $\omega = 1/T$. The initial slope is 12 db/octave until the corner frequency, at which point the curve falls at 18 db/octave. Phase shift is 180° lagging at low frequencies, approaching 270° at higher frequencies.

PROBLEM C.14 Plot the Bode curves for

$$G(j\omega) = \frac{K}{(j\omega)(0.1j\omega + 1)}$$ (C.14)

Solution: Refer to Fig. C.14. This shows the Bode plots for $K = 1$.
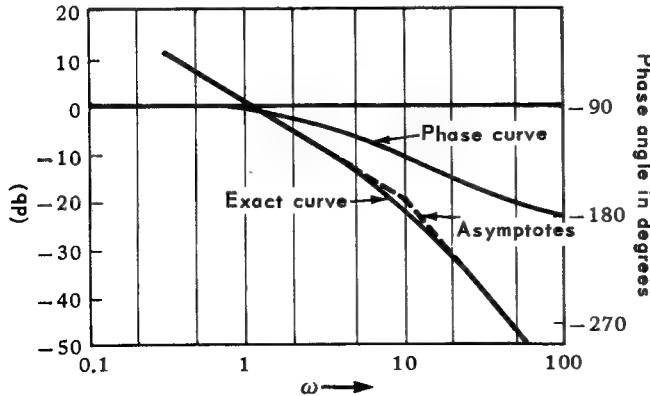
Fig. C.14 Bode diagram, amplitude and phase.

PROBLEM C.15   Plot the Bode curves for

$$G(j\omega) = \frac{K}{(j\omega)(j\omega + 1)\left(j\dfrac{\omega}{2} + 1\right)} \;. \tag{C.15}$$

Solution: Refer to Fig. C.15. This shows the Bode plots for $K = 2$.
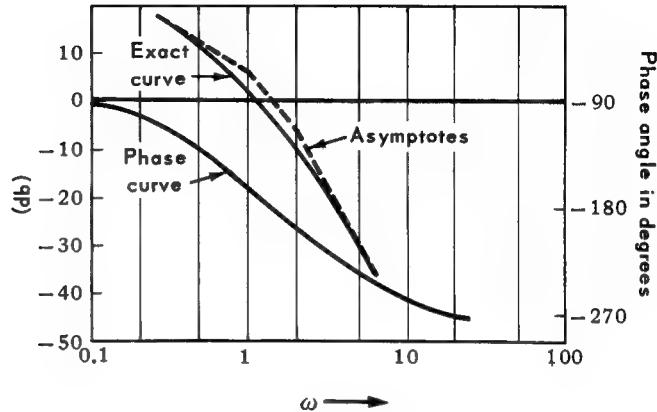
Fig. C.15 Bode diagram, amplitude and phase.

DISTORTION CALCULATION

D.1 Distortion

Distortion is a measure of the degree to which a given periodic waveform departs from non-sinusoidality. Implicit in this definition is the presence of a *fundamental frequency component*, upon which distortion components are superimposed.

An exact analysis of the distortion in a given periodic waveform is routinely carried out using numerical methods based on Fourier series. By this means, it is possible to achieve any degree of accuracy justified by the given waveform data. Furthermore, specific higher harmonics may be investigated where desired.

However, this method of *harmonic analysis* is very tedious, and much too refined for the simpler problem of determining distortion in the output of a power amplifier. The principal distortion components in power amplifier output are second and third harmonic, and frequently, even the third harmonic component may be neglected.

Accordingly, simplified methods of Fourier analysis have been devised to give only the important low-order distortion components. These methods, taking no more than a few minutes to apply to a specific waveform, are summarized in Figs. D.1 and D.2. Figure D.1 applies when *only* second harmonic distortion is present, while Fig. D.2 applies when the distortion includes second and third harmonic components.

Individual distortion components may be designated by the ratios of their individual amplitudes to the fundamental amplitude. *Total distortion* is usually calculated as follows:

$$D_t \ (\%) = \frac{\sqrt{\sum D_i^2}}{D_1} \times 100,$$

where D_i represents the amplitude of the i-th harmonic, while D_1 represents the fundamental amplitude.

Using the formulae of Fig. D.2, the following expressions may be derived for the components denoted by y of a distorted waveform:

$$y_0 = \frac{1}{6} [x_1 + x_2 + 2(x' + x'')], \qquad (D.1a)$$

$$y_1 = \frac{1}{3} [x_1 - x_2 + x' - x''], \qquad (D.1b)$$

$$y_2 = \frac{1}{3} [x_1 + x_2 - x' - x''], \qquad (D.1c)$$

$$y_3 = \frac{1}{6} [x_0 - x_2 - 2x' + 2x'']. \qquad (D.1d)$$

$$D_2 \ (\%) = \frac{x_1 + x_2 - 2x_q}{2(x_2 - x_1)} \times 100$$

x_q = quiescent value of waveform
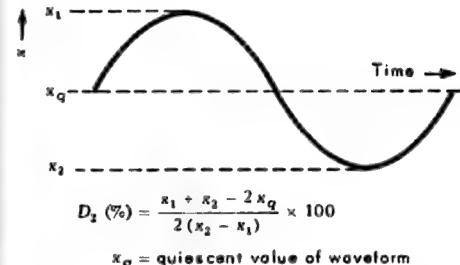
Fig. D.1 Calculation of second harmonic distortion component in an approximately sinusoidal waveform. Higher harmonics are negligible; D = percent distortion.

$$\omega t_0 \qquad \omega_0 t_0 \qquad \omega_0 t_0 \qquad \omega t_0 + \pi$$
$$+ \frac{\pi}{3} \qquad + \frac{2\pi}{3}$$

$$D_2 \ (\%) = \frac{x_1 + x_2 - x' - x''}{x_1 - x_2 + x' - x''} \times 100$$

$$D_3 \ (\%) = \frac{x_1 - x_2 - 2(x' - x'')}{2(x_1 - x_2 + x' - x'')}$$

$$D_t = \sqrt{D_2^2 + D_3^2}$$
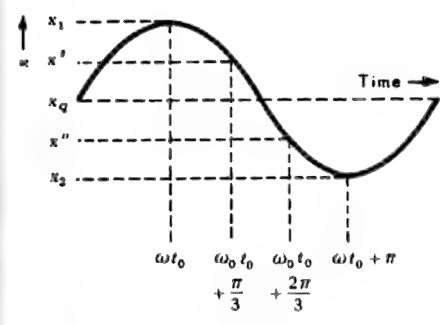
Fig. D.2 Calculation of second and third harmonic distortion components in an approximately sinusoidal waveform. Higher harmonics are negligible; D = percent distortion.

PROBLEM D.1   Refer to Fig. D.2. Analyze the wave described by the following parameters for distortion components: $x_1 = 2$, $x_2 = 0$, $x_q = 1$, $x' = \frac{3}{2}$, $x'' = \frac{1}{2}$. Also use (D.1).

Solution: Using direct substitution, the following results are obtained:

$$D_2(\%) = \frac{2 + 0 - \frac{3}{2} - \frac{1}{2}}{2 + \frac{3}{2} - \frac{1}{2}} = 0,$$

$$D_3(\%) = \frac{2 - 0 - 2\left(\frac{3}{2} - \frac{1}{2}\right)}{2\left(2 - 0 + \frac{3}{2} + \frac{1}{2}\right)} = 0,$$

$$y_0 = \frac{1}{6}\left[2 + 0 + 2(2)\right] = 1,$$

$$y_1 = \frac{1}{3}\left[2 - 0 + \frac{3}{2} - \frac{1}{2}\right] = 1,$$

$$y_2 = \frac{1}{3}\left[2 + 0 - \frac{3}{2} - \frac{1}{2}\right] = 0,$$

$$y_3 = \frac{1}{6}\left[2 - 0 - 3 + 1\right] = 0.$$

The wave exhibits no second or third harmonic distortion components. As a matter of fact, at the points defined in this problem, the wave has the parameters of a pure sinusoid.

Test the formula of Fig. D.1 for second harmonic distortion:

$$D_2(\%) = \frac{2 - 2}{2(0 - 2)} \times 100 = 0.$$

This result is of course necessary for consistency.

LIST OF SYMBOLS

A_I	current gain
A_p	small-signal average power gain
A_v	voltage gain
B	base electrode
BV_{CBO}	breakdown voltage, collector to base, emitter open
BV_{CEO}	breakdown voltage, collector to emitter, base open
BV_{CER}	breakdown voltage, collector to emitter, with specified resistance between base and emitter
BV_{CES}	breakdown voltage, collector to emitter, with base short-circuited to emitter
BV_{EBO}	breakdown voltage, emitter to base, collector open
BV_R	breakdown voltage, reverse
C	collector electrode
C_{ib}	input capacitance (common-base)
C_{ic}	input capacitance (common-collector)
C_{ie}	input capacitance (common-emitter)
C_{ob}	output capacitance (common-base)
C_{oc}	output capacitance (common-collector)
C_{oe}	output capacitance (common-emitter)
E	emitter electrode
f_{hfb}	small-signal short-circuit forward current transfer ratio cut-off frequency (common-base)
f_{hfc}	small-signal short-circuit forward current transfer ratio cut-off frequency (common-collector)
f_{hfe}	small-signal short-circuit forward current transfer ratio cut-off frequency (common-emitter)
h_{FB}	static value of the forward current transfer ratio (common-base)
h_{fb}	small-signal short-circuit forward current transfer ratio (common-base)
h_{FC}	static value of the forward current transfer ratio (common-collector)
h_{fc}	small-signal short-circuit forward current transfer ratio (common-collector)
h_{FE}	static value of the forward current transfer ratio (common-emitter)
h_{fe}	small-signal short-circuit forward current transfer ratio (common-emitter)

h_{IB}	static value of the input resistance (common-base)
h_{ib}	small-signal value of the short-circuit input impedance (common-base)
h_{IC}	static value of the input resistance (common-collector)
h_{ic}	small-signal value of the short-circuit input impedance (common-collector)
h_{IE}	static value of the input resistance (common-emitter)
h_{ie}	small-signal value of the short-circuit input impedance (common-emitter)
h_{OB}	static value of the open-circuit output conductance (common-base)
h_{ob}	small-signal value of the open-circuit output admittance (common-base)
h_{OC}	static value of the open-circuit output conductance (common-collector)
h_{oc}	small-signal value of the open-circuit output admittance (common-collector)
h_{OE}	static value of the open-circuit output conductance (common-emitter)
h_{oe}	small-signal value of the open-circuit output admittance (common-emitter)
h_{rb}	small-signal value of the open-circuit reverse voltage transfer ratio (common-base)
h_{rc}	small-signal value of the open-circuit reverse voltage transfer ratio (common-collector)
h_{re}	small-signal value of the open-circuit reverse voltage transfer ratio (common-emitter)
I_B	base current (d-c)
i_b	base current (instantaneous)
I_C	collector current (d-c)
i_c	collector current (instantaneous)
I_{CBO}	collector cut-off current (d-c), emitter open
I_{CEO}	collector cut-off current (d-c), base open
I_{CER}	collector cut-off current (d-c), with specified resistance between base and emitter
I_{CEX}	collector current (d-c), with specified circuit between base and emitter
I_{CES}	collector cut-off current (d-c), with base short-circuited to emitter

I_E — emitter current (d-c)

i_e — emitter current (instantaneous)

I_{EBO} — emitter cut-off current (d-c), collector open

I_F — forward current (d-c)

i_F — forward current (instantaneous)

I_R — reverse current (d-c)

i_R — reverse current (instantaneous)

I_s — saturation current

n — region of a device where electrons are the majority carriers

p — region of a device where holes are the majority carriers

P_{BE} — total power input (d-c or average) to the base electrode with respect to the emitter electrode

P_C — collector junction dissipation

P_{CB} — total power input (d-c or average) to the collector electrode with respect to the base electrode

P_{CE} — total power input (d-c or average) to the collector electrode with respect to the emitter electrode

P_{EB} — total power input (d-c or average) to the emitter electrode with respect to the base electrode

P_I — large-signal input power

P_i — small-signal input power

P_L — load power

P_O — large-signal output power

P_o — small-signal output power

P_T — total power input (d-c or average) to all electrodes

r_f — small-signal forward resistance

R_B — external base resistance

r_b — base resistance

R_C — external collector resistance

r_c — collector resistance

R_E — external emitter resistance

r_e — emitter resistance

R_s — saturation resistance

R_L — load resistance

T — temperature

T_A — ambient temperature

T_C — case temperature

T_j — junction temperature

θ — thermal resistance

θ_{j-A} — thermal resistance, junction to ambient

θ_{j-C} — thermal resistance, junction to case

V_{BB} — base supply voltage (d-c)

V_{BC} — base to collector voltage (d-c)

v_{bc} — base to collector voltage (instantaneous)

V_{BE} — base to emitter voltage (d-c)

v_{be} — base to emitter voltage (instantaneous)

V_{CB} — collector to base voltage (d-c)

v_{cb} — collector to base voltage (instantaneous)

V_{CC} — collector supply voltage (d-c)

V_{CE} — collector to emitter voltage (d-c)

v_{ce} — collector to emitter voltage (instantaneous)

$V_{CE(sat)}$ — collector to emitter saturation voltage

V_{EB} — emitter to base voltage (d-c)

v_{eb} — emitter to base voltage (instantaneous)

V_{EC} — emitter to collector voltage (d-c)

v_{ec} — emitter to collector voltage (instantaneous)

V_{EE} — emitter supply voltage (d-c)

V_F — forward voltage (d-c)

v_F — forward voltage (instantaneous)

V_{CBF} — d-c open-circuit voltage (floating potential) between the collector and base, with the emitter biased in the reverse direction with respect to the collector.

V_{ECF} — d-c open-circuit voltage (floating potential) between the emitter and collector, with the base biased in the reverse direction with respect to the collector

V_R — reverse voltage (d-c)

v_R — reverse voltage (instantaneous)

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